



**Advanced Power
Electronics Corp.**

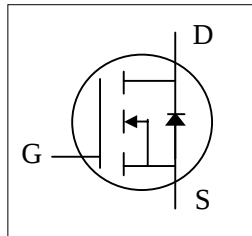
AP2764AI-A-HF

Halogen-Free Product

N-CHANNEL ENHANCEMENT MODE

POWER MOSFET

- ▼ 100% Avalanche Test
- ▼ Fast Switching Characteristic
- ▼ Simple Drive Requirement
- ▼ RoHS Compliant

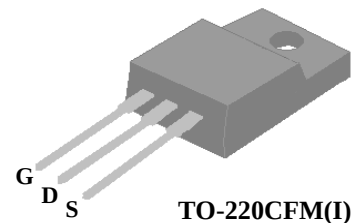


BV_{DSS}	650V
$R_{DS(ON)}$	1.1Ω
I_D	9A

Description

AP2764A series are specially designed as main switching devices for universal 90~265VAC off-line AC/DC converter applications.

TO-220CFM type provide high blocking voltage to overcome voltage surge and sag in the toughest power system with the best combination of fast switching, ruggedized design and cost-effectiveness.



TO-220CFM(I)

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	650	V
V_{GS}	Gate-Source Voltage	± 30	V
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	9	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	6	A
I_{DM}	Pulsed Drain Current ¹	36	A
$P_D @ T_C = 25^\circ\text{C}$	Total Power Dissipation	37	W
E_{AS}	Single Pulse Avalanche Energy ²	32	mJ
I_{AR}	Avalanche Current	8	A
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Value	Units
Rthj-c	Maximum Thermal Resistance, Junction-case	3.4	$^\circ\text{C}/\text{W}$
Rthj-a	Maximum Thermal Resistance, Junction-ambient	65	$^\circ\text{C}/\text{W}$


Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =1mA	650	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ³	V _{GS} =10V, I _D =4A	-	-	1.1	Ω
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	2	-	4	V
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =4A	-	8	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =480V, V _{GS} =0V	-	-	25	uA
	Drain-Source Leakage Current (T _j =125°C)	V _{DS} =480V, V _{GS} =0V	-	-	500	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±30V, V _{DS} =0V	-	-	±100	nA
Q _g	Total Gate Charge ³	I _D =7A	-	66	105	nC
Q _{gs}	Gate-Source Charge	V _{DS} =480V	-	10	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =10V	-	24	-	nC
t _{d(on)}	Turn-on Delay Time ³	V _{DD} =300V	-	36	-	ns
t _r	Rise Time	I _D =7A	-	46	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =50Ω, V _{GS} =10V	-	465	-	ns
t _f	Fall Time	R _D =42.8Ω	-	87	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	2730	4400	pF
C _{oss}	Output Capacitance	V _{DS} =15V	-	470	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	60	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ³	I _S =7A, V _{GS} =0V	-	-	1.5	V
t _{rr}	Reverse Recovery Time ³	I _S =7A, V _{GS} =0V,	-	480	-	ns
Q _{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	7	-	μC

Notes:

- 1.Pulse width limited by max. junction temperature.
- 2.Starting T_j=25°C , V_{DD}=50V , L=1mH , R_G=25Ω
- 3.Pulse test

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

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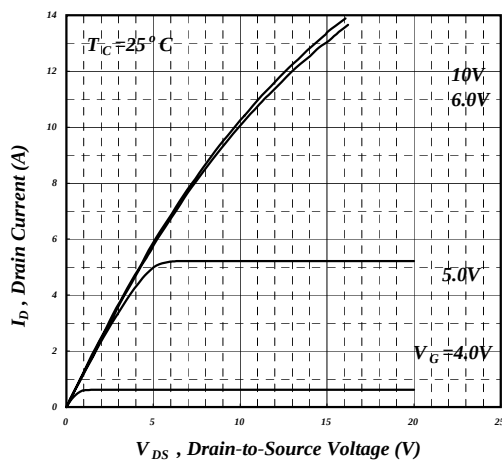


Fig 1. Typical Output Characteristics

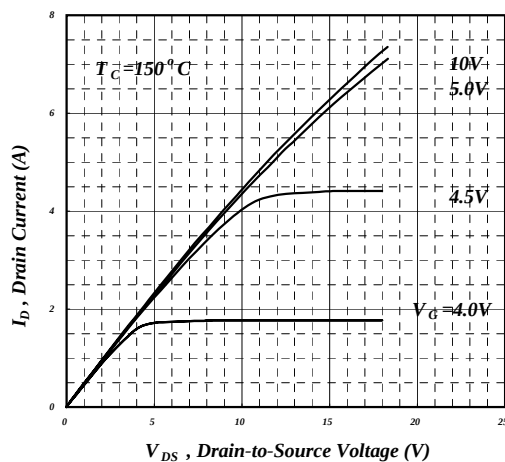


Fig 2. Typical Output Characteristics

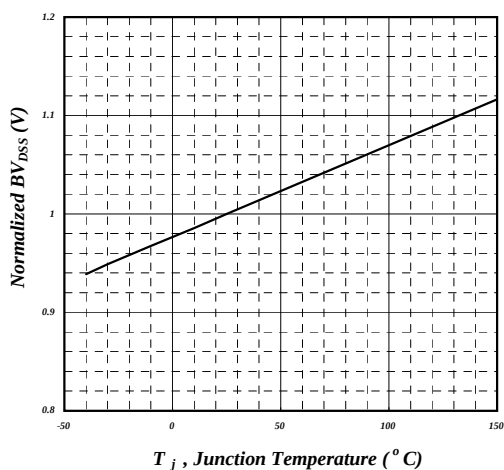


Fig 3. Normalized BV_{DSS} v.s. Junction Temperature

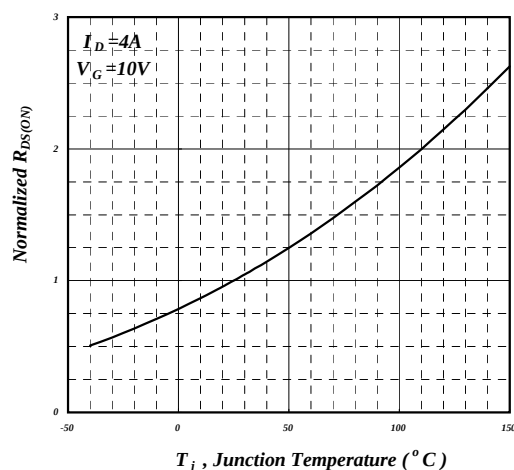


Fig 4. Normalized On-Resistance v.s. Junction Temperature

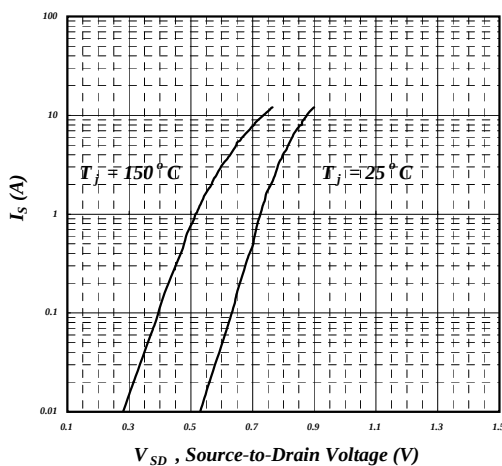


Fig 5. Forward Characteristic of Reverse Diode

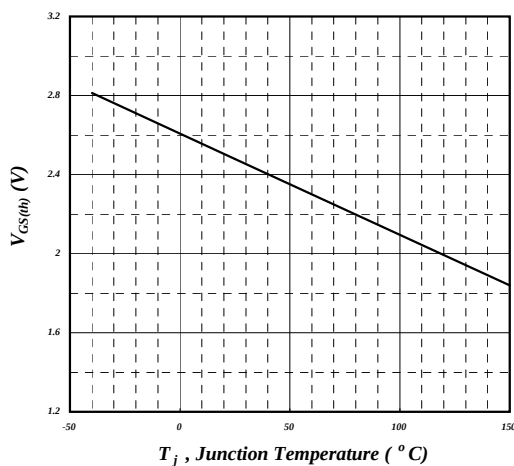


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

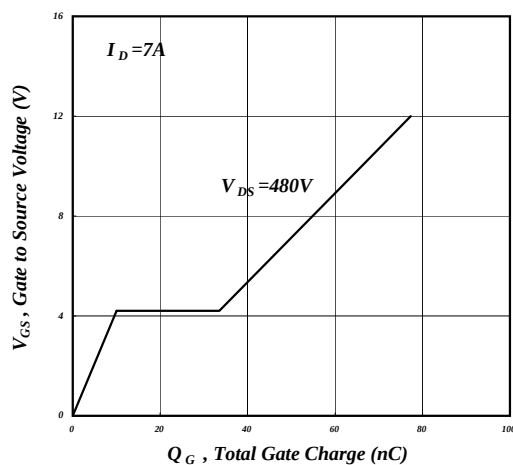


Fig 7. Gate Charge Characteristics

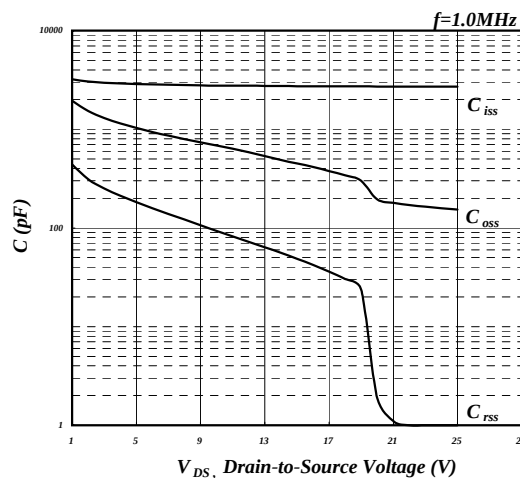


Fig 8. Typical Capacitance Characteristics

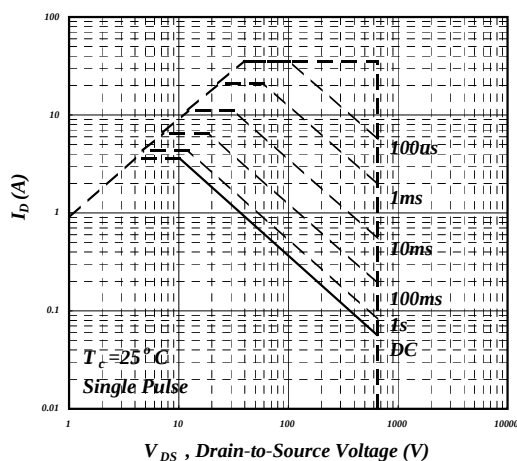


Fig 9. Maximum Safe Operating Area

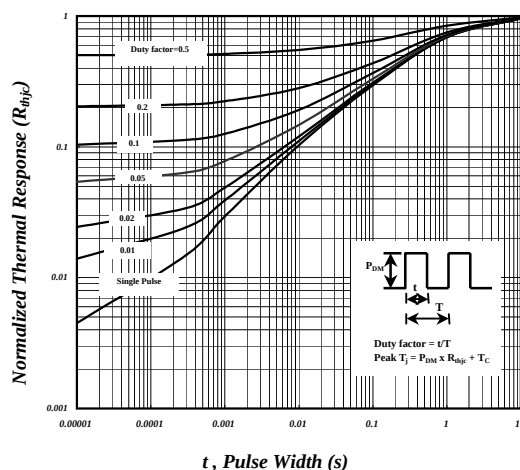


Fig 10. Effective Transient Thermal Impedance

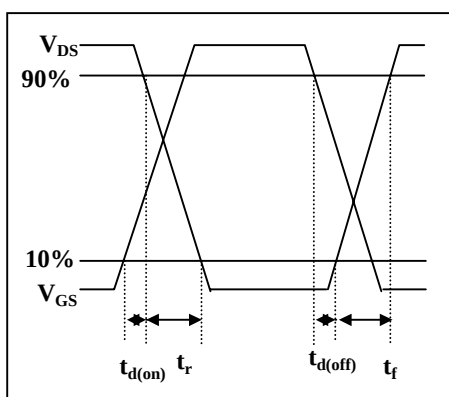


Fig 11. Switching Time Waveform

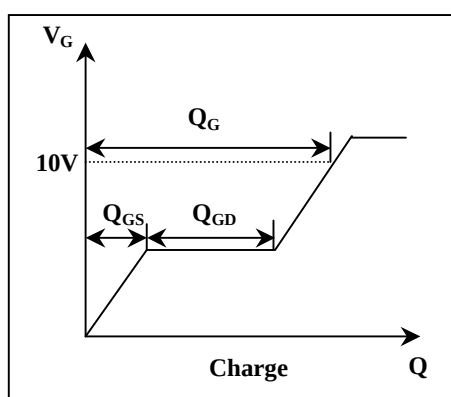


Fig 12. Gate Charge Waveform



Technical drawing of a punch and die set. The drawing includes a top view of the punch and a side view of the die. Dimensions are labeled as follows:

- Punch Dimensions:**
 - E : Total width of the punch head.
 - ϕ : Diameter of the punch tip.
 - L : Total length of the punch.
 - $L3$: Length of the punch head.
 - $b1$: Width of the punch head.
 - b : Width of the punch tip.
 - e : Thickness of the punch tip.
- Die Dimensions:**
 - A : Total width of the die.
 - $A1$: Width of the die head.
 - c : Thickness of the die head.
 - $c2$: Width of the die tip.
 - $L4$: Length of the die head.

SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	4.30	4.70	4.90
A1	2.30	2.65	3.00
b	0.50	0.70	0.90
b1	0.95	1.20	1.50
c	0.45	0.65	0.80
c2	2.30	2.60	2.90
E	9.70	10.00	10.40
L	12.00	---	15.00
L3	2.91	3.41	3.91
L4	14.70	15.40	16.10
ϕ	----	3.20	----
e	----	2.54	----

1.All Dimensions Are in Millimeters.
2.Dimension Does Not Include Mold Protrusions.

Diagram illustrating the marking layout on a component, showing the following fields and their corresponding labels:

- LOGO (indicated by a blue circle with a white 'A')
- Option (indicated by the letter 'A')
- Part Number (indicated by the text '2764AI')
- Package Code (indicated by the text '2764AI')
- Date Code (YWWSSS) (indicated by the text 'YWWSSS')

Legend for Date Code (YWWSSS):

- Y : Last Digit Of The Year
- WW : Week
- SSS : Sequence
- If last "S" is numerical letter : Rohs product
- If last "S" is English letter : HF & Rohs product