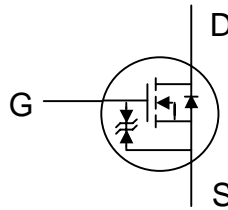




**N-channel Enhancement-mode Power MOSFET**

- Simple Drive Requirement**
- Small Package Outline**
- Surface Mount Device**
- RoHS-compliant, halogen-free**



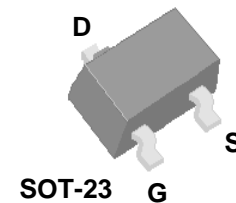
$BV_{DSS}$	60V
$R_{DS(ON)}$	2Ω
$I_D$	450mA

**Description**

Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, low on-resistance and cost-effectiveness.

The AP2N7002K-HF-3 is in the popular SOT-23 small surface-mount package which is widely used in commercial and industrial applications where a small board footprint is required.

This device is well suited for use in medium current applications such as load switches.



**Absolute Maximum Ratings**

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	60	V
$V_{GS}$	Gate-Source Voltage	±20	V
$I_D$ at $T_A=25^{\circ}C$	Continuous Drain Current <sup>3</sup>	450	mA
$I_D$ at $T_A=70^{\circ}C$	Continuous Drain Current <sup>3</sup>	360	mA
$I_{DM}$	Pulsed Drain Current <sup>1,2</sup>	950	mA
$P_D$ at $T_A=25^{\circ}C$	Total Power Dissipation	0.7	W
	Linear Derating Factor	0.005	W/°C
$T_{STG}$	Storage Temperature Range	-55 to 150	°C
$T_J$	Operating Junction Temperature Range	-55 to 150	°C

**Thermal Data**

Symbol	Parameter	Value	Unit
Rthj-a	Maximum Thermal Resistance, Junction-ambient	180	°C/W

**Ordering Information**

**AP2N7002K-HF-3TR** : in RoHS-compliant halogen-free SOT-23, shipped on tape and reel (3000pcs/reel)



**Electrical Specifications at  $T_j=25^\circ\text{C}$  (unless otherwise specified)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	60	-	-	V
$\Delta BV_{DSS}/\Delta T_j$	Breakdown Voltage Temperature Coefficient	Reference to $25^\circ\text{C}, I_D=1\text{mA}$	-	0.06	-	V/ $^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10V, I_D=450\text{mA}$	-	-	2	$\Omega$
		$V_{GS}=4.5V, I_D=200\text{mA}$	-	-	4	$\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1	-	2.5	V
$g_{fs}$	Forward Transconductance	$V_{DS}=10V, I_D=450\text{mA}$	-	400	-	mS
$I_{DSS}$	Drain-Source Leakage Current ( $T_j=25^\circ\text{C}$ )	$V_{DS}=60V, V_{GS}=0V$	-	-	10	$\mu A$
	Drain-Source Leakage Current ( $T_j=70^\circ\text{C}$ )	$V_{DS}=48V, V_{GS}=0V$	-	-	100	$\mu A$
$I_{GSS}$	Gate-Source Leakage	$V_{GS}=\pm 20V$	-	-	$\pm 30$	$\mu A$
$Q_g$	Total Gate Charge <sup>2</sup>	$I_D=450\text{mA}$	-	1	1.6	nC
$Q_{gs}$	Gate-Source Charge	$V_{DS}=50V$	-	0.5	-	nC
$Q_{gd}$	Gate-Drain ("Miller") Charge	$V_{GS}=4.5V$	-	0.5	-	nC
$t_{d(on)}$	Turn-on Delay Time <sup>2</sup>	$V_{DS}=30V$	-	12	-	ns
$t_r$	Rise Time	$I_D=450\text{mA}$	-	10	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=3.3\Omega, V_{GS}=10V$	-	56	-	ns
$t_f$	Fall Time	$R_D=52\Omega$	-	29	-	ns
$C_{iss}$	Input Capacitance	$V_{GS}=0V$	-	32	50	pF
$C_{oss}$	Output Capacitance	$V_{DS}=25V$	-	8	-	pF
$C_{rss}$	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	6	-	pF

**Source-Drain Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{SD}$	Forward On Voltage <sup>2</sup>	$I_S=450\text{mA}, V_{GS}=0V$	-	-	1.2	V

**Notes:**

1. Pulse width limited by maximum junction temperature.
2. Pulse test - pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$
3. Surface mounted on  $1\text{in}^2$  copper pad of FR4 board,  $t \leq 10\text{sec}$ ;  $400^\circ\text{C}/\text{W}$  when mounted on minimum copper pad.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

APEC RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.



Typical Electrical Characteristics

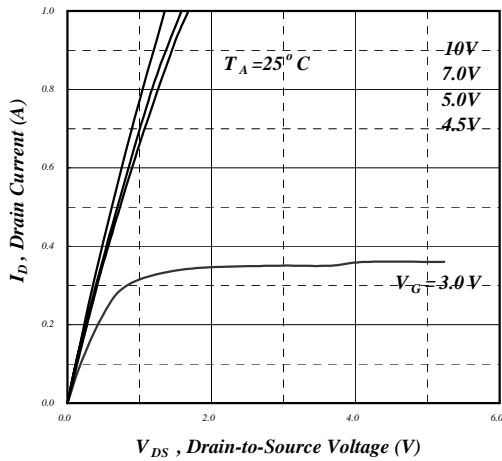


Fig 1. Typical Output Characteristics

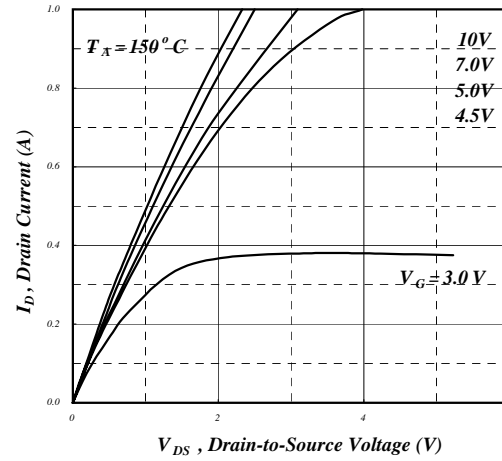


Fig 2. Typical Output Characteristics

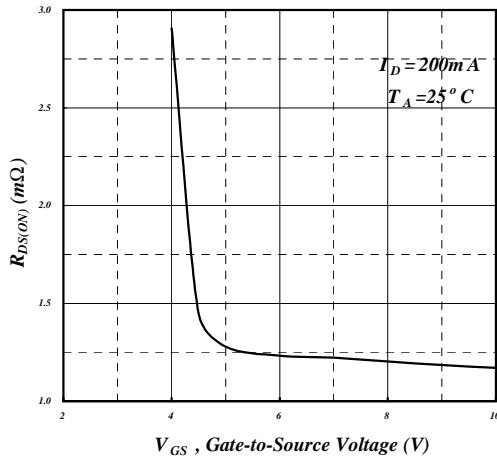


Fig 3. On-Resistance vs. Gate Voltage

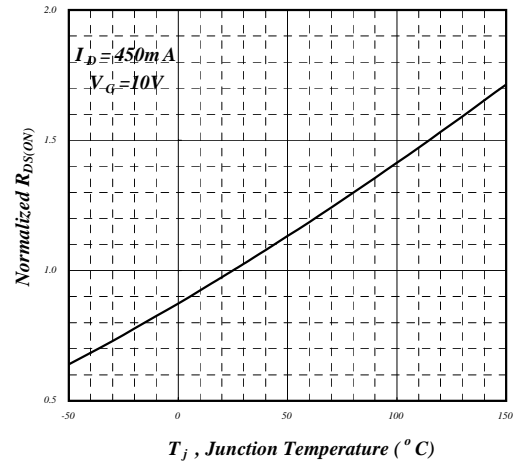


Fig 4. Normalized On-Resistance vs. Junction Temperature

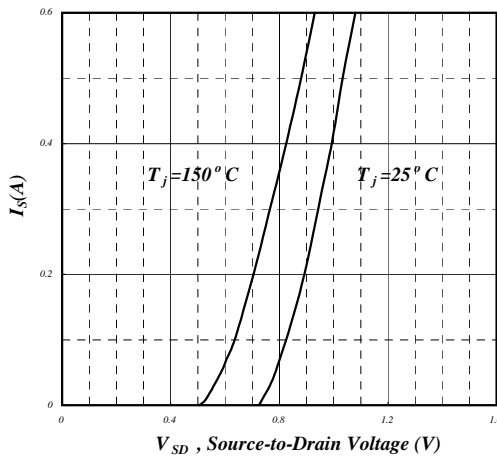


Fig 5. Forward Characteristic of Reverse Diode

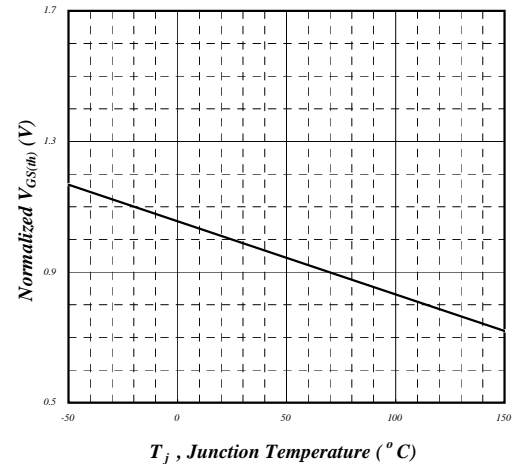


Fig 6. Gate Threshold Voltage vs. Junction Temperature



Typical Electrical Characteristics (cont.)

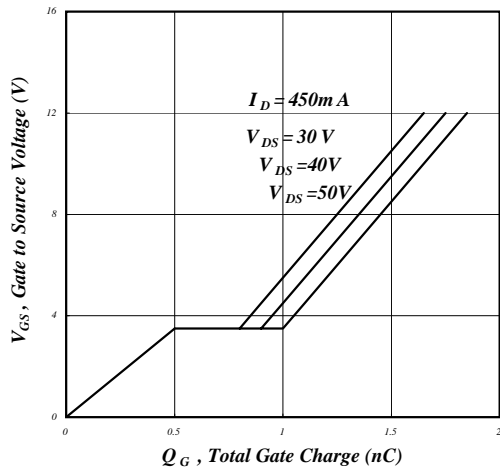


Fig 7. Gate Charge Characteristics

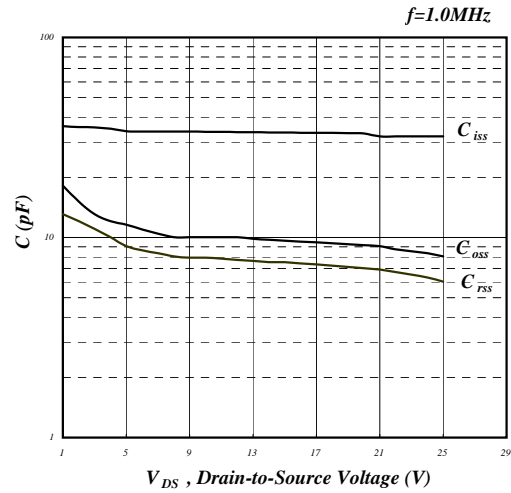


Fig 8. Typical Capacitance Characteristics

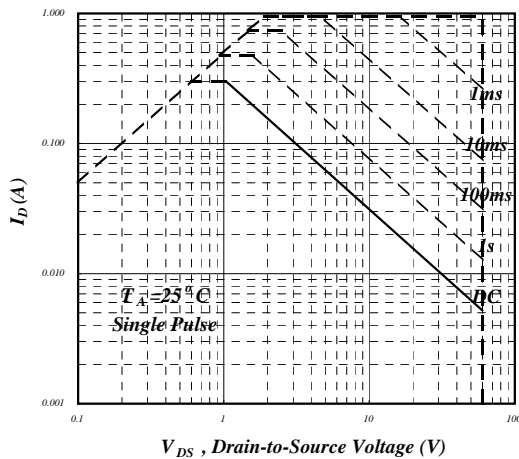


Fig 9. Maximum Safe Operating Area

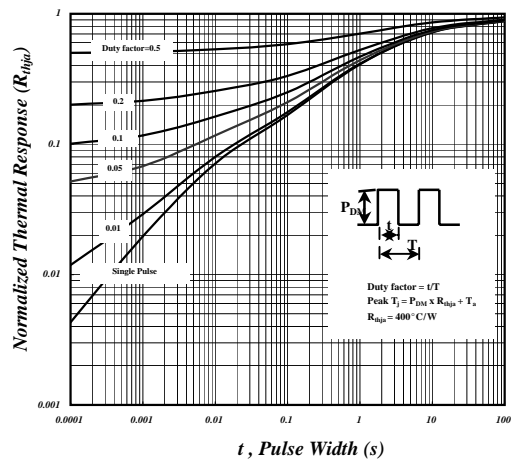


Fig 10. Effective Transient Thermal Impedance

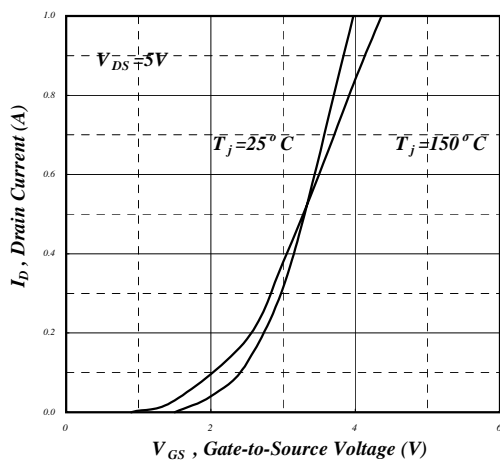


Fig 11. Transfer Waveform

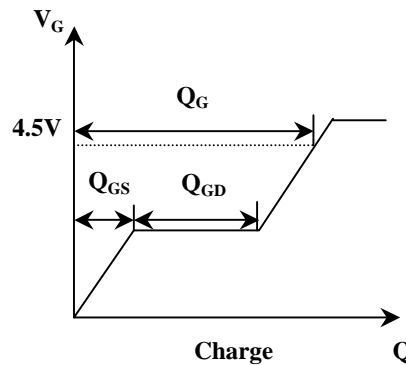
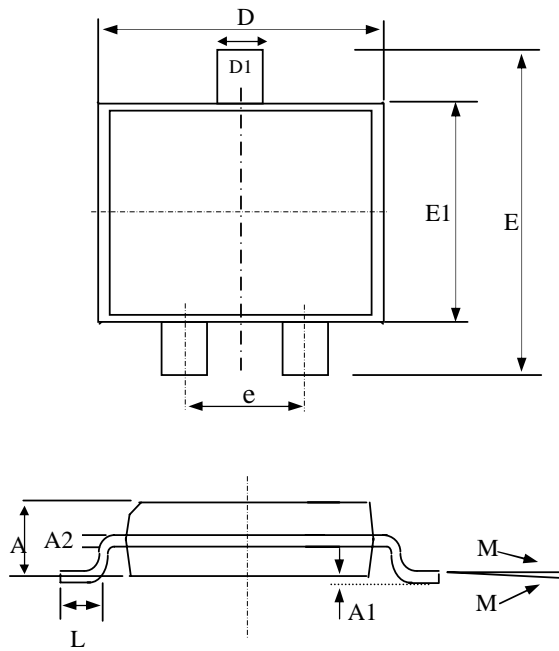


Fig 12. Gate Charge Waveform



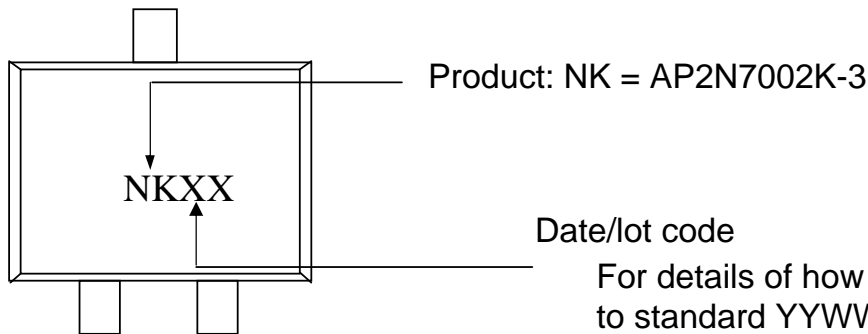
**Package Dimensions: SOT-23**



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	0.88	--	1.30
A1	0.00	--	0.10
A2	0.08	--	0.25
D1	0.30	0.40	0.50
e	1.70	2.00	2.30
D	2.70	2.90	3.10
E	2.20	2.60	3.00
E1	1.20	1.50	1.80
M	0°	--	10°
L	0.30	--	0.60

1. All dimensions are in millimeters.
2. Dimensions do not include mold protrusions.

**Marking Information: SOT-23**



For details of how to convert this to standard YYWW date code format, please contact us directly.