



**Advanced Power
Electronics Corp.**

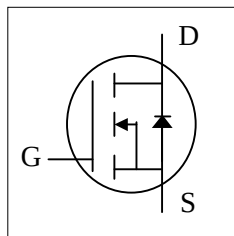
AP2RA04GMT-HF

Halogen-Free Product

N-CHANNEL ENHANCEMENT MODE

POWER MOSFET

- ▼ Simple Drive Requirement
- ▼ SO-8 Compatible with Heatsink
- ▼ Low On-resistance
- ▼ RoHS Compliant & Halogen-Free

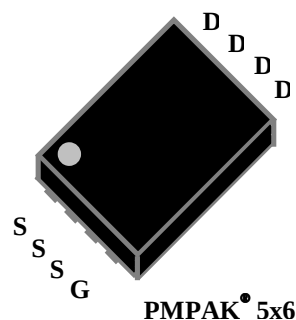


BV_{DSS}	40V
$R_{DS(ON)}$	2.9m Ω
I_D	130A

Description

AP2RA04 series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The PMPAK[®] 5x6 package is special for DC-DC converters application and the foot print is compatible with SO-8 with backside heat sink and lower profile.



Absolute Maximum Ratings@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	40	V
V_{GS}	Gate-Source Voltage	+20	V
$I_D@T_C=25^{\circ}C$	Drain Current (Chip), $V_{GS} @ 10V$	130	A
$I_D@T_A=25^{\circ}C$	Drain Current, $V_{GS} @ 10V^3$	32.5	A
$I_D@T_A=70^{\circ}C$	Drain Current, $V_{GS} @ 10V^3$	26	A
I_{DM}	Pulsed Drain Current ¹	250	A
$P_D@T_C=25^{\circ}C$	Total Power Dissipation	83.3	W
$P_D@T_A=25^{\circ}C$	Total Power Dissipation	5	W
E_{AS}	Single Pulse Avalanche Energy ⁴	28.8	mJ
T_{STG}	Storage Temperature Range	-55 to 150	°C
T_J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Value	Units
Rthj-c	Maximum Thermal Resistance, Junction-case	1.5	°C/W
Rthj-a	Maximum Thermal Resistance, Junction-ambient ³	25	°C/W



AP2RA04GMT-HF

Electrical Characteristics@T_J=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	40	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =20A	-	-	2.9	mΩ
		V _{GS} =4.5V, I _D =20A	-	-	4.6	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	1	-	3	V
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =20A	-	80	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =40V, V _{GS} =0V	-	-	10	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Q _g	Total Gate Charge	I _D =20A	-	26	42	nC
Q _{gs}	Gate-Source Charge	V _{DS} =20V	-	6	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =4.5V	-	14	-	nC
t _{d(on)}	Turn-on Delay Time	V _{DS} =20V	-	10.5	-	ns
t _r	Rise Time	I _D =1A	-	8	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =3.3Ω	-	27	-	ns
t _f	Fall Time	V _{GS} =10V	-	52	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	2800	4500	pF
C _{oss}	Output Capacitance	V _{DS} =25V	-	615	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	190	-	pF
R _g	Gate Resistance	f=1.0MHz	-	1.6	3.2	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ²	I _S =20A, V _{GS} =0V	-	-	1.2	V
t _{rr}	Reverse Recovery Time	I _S =10A, V _{GS} =0V,	-	41	-	ns
Q _{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	49	-	nC

Notes:

1. Pulse width limited by Max. junction temperature
2. Pulse test
3. Surface mounted on 1 in² copper pad of FR4 board, t ≤ 10sec, 60°C/W at steady state.
4. Starting T_J=25°C, V_{DD}=25V, L=0.1mH, R_G=25Ω, I_{AS}=24A.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

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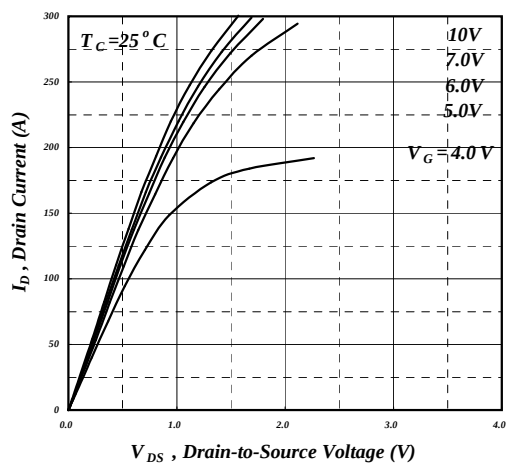


Fig 1. Typical Output Characteristics

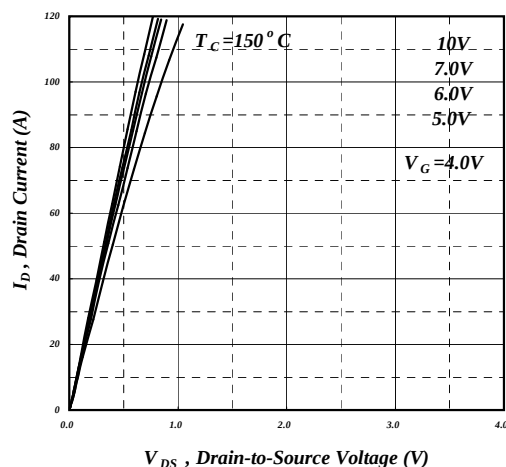


Fig 2. Typical Output Characteristics

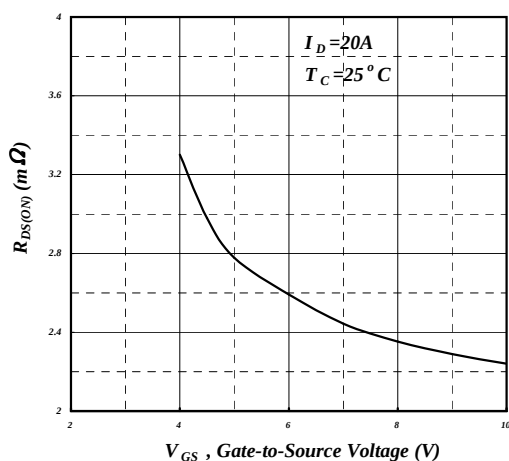


Fig 3. On-Resistance v.s. Gate Voltage

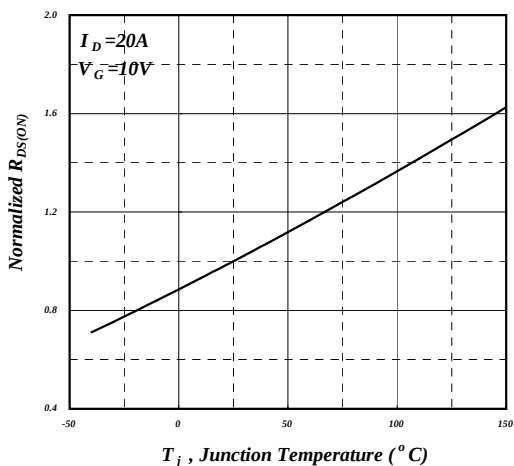


Fig 4. Normalized On-Resistance v.s. Junction Temperature

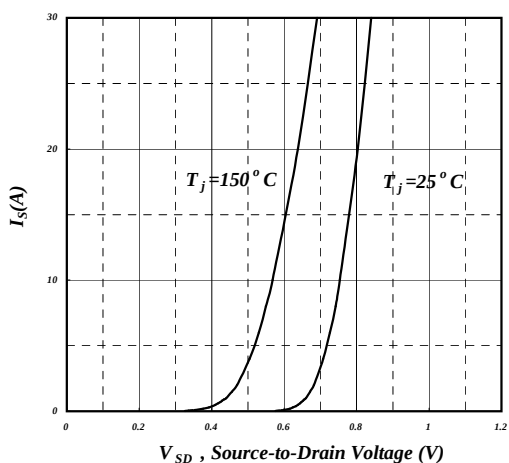


Fig 5. Forward Characteristic of Reverse Diode

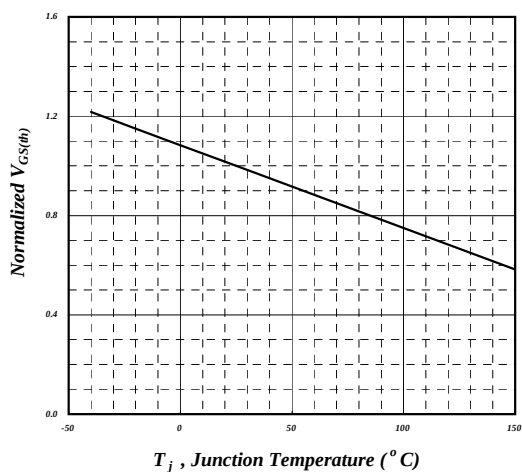


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

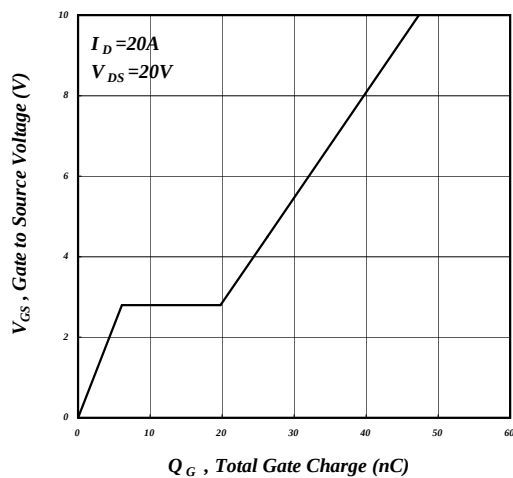


Fig 7. Gate Charge Characteristics

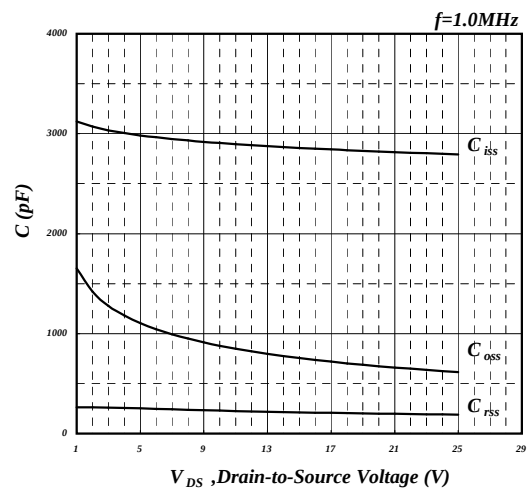


Fig 8. Typical Capacitance Characteristics

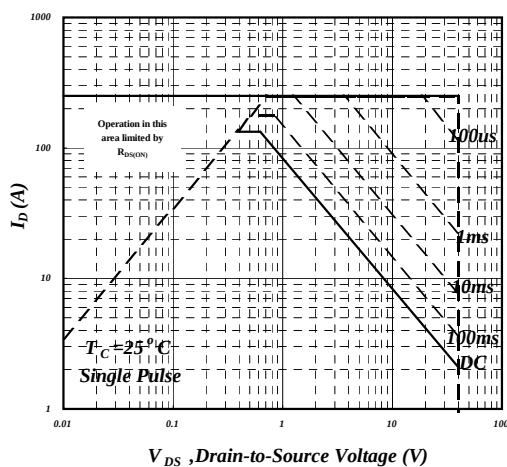


Fig 9. Maximum Safe Operating Area

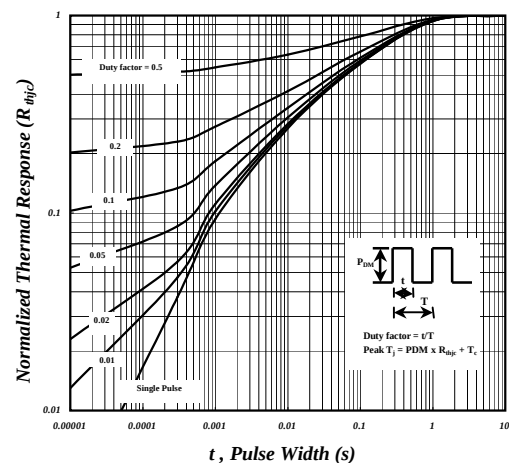


Fig 10. Effective Transient Thermal Impedance

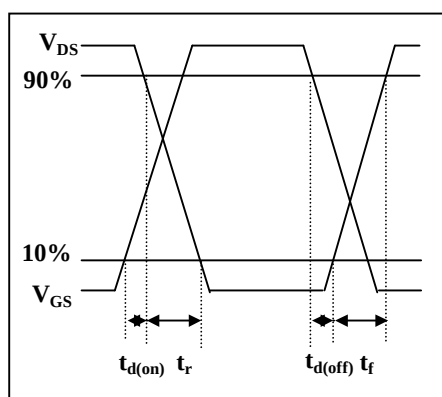


Fig 11. Switching Time Waveform

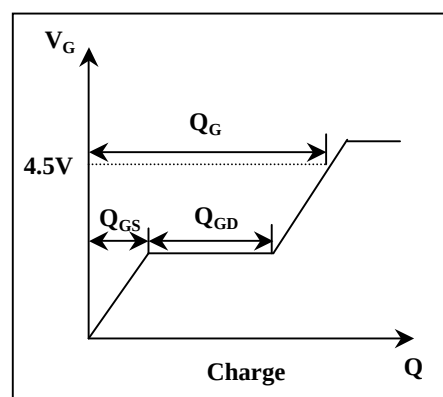


Fig 12. Gate Charge Waveform



MARKING INFORMATION

