

## 40V N+P-Channel Enhancement Mode MOSFET

### Description

The AP30G04NF uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

### General Features

$V_{DS} = 40V$   $I_D = 38A$

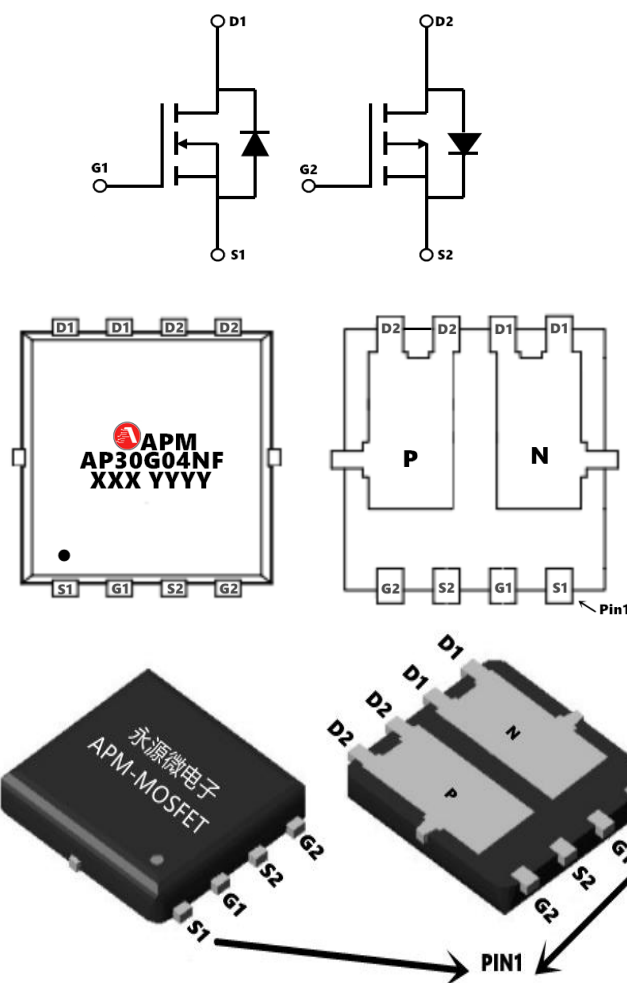
$R_{DS(ON)} < 10m\Omega$  @  $V_{GS}=10V$  (Type: 8.0m $\Omega$ )

$V_{DS} = -40V$   $I_D = -35A$

$R_{DS(ON)} < 18m\Omega$  @  $V_{GS}=-10V$  (Type: 13m $\Omega$ )

### Application

BLDC



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP30G04NF	PDFN5X6-8L	AP30G04NF XXX YYYY	5000

### Absolute Maximum Ratings ( $T_c=25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	N-Ch	P-Ch	Units
$V_{DS}$	Drain-Source Voltage	40	-40	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	$\pm 20$	V
$I_D@T_c=25^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V^1$	38	-35	A
$I_D@T_c=100^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V^1$	31	-29	A
IDM	Pulsed Drain Current <sup>2</sup>	144	-129	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	128	185	mJ
IAS	Avalanche Current	16	-18	A
$P_D@T_c=25^{\circ}C$	Total Power Dissipation <sup>4</sup>	48	51.3	W
TSTG	Storage Temperature Range	-55 to 150		$^{\circ}C$
$T_J$	Operating Junction Temperature Range	-55 to 150		$^{\circ}C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	25		$^{\circ}C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	2.3		$^{\circ}C/W$

**40V N+P-Channel Enhancement Mode MOSFET**
**Electrical Characteristics ( $T_J=25^{\circ}\text{C}$ , unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	40	44	---	V
$\Delta BVDSS/\Delta T_J$	BVDSS Temperature Coefficient	Reference to $25^{\circ}\text{C}$ , $I_D=1mA$	---	0.028	---	$V/^{\circ}\text{C}$
RDS(ON)	Static Drain-Source On-Resistance	$V_{GS}=10V, I_D=30A$	---	8.0	10	m $\Omega$
		$V_{GS}=4.5V, I_D=15A$	---	10	16	
VGS(th)	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.2	1.6	2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-6.16	---	mV/ $^{\circ}\text{C}$
IDSS	Drain-Source Leakage Current	$V_{DS}=40V, V_{GS}=0V, T_J=25^{\circ}\text{C}$	---	---	1	$\mu A$
		$V_{DS}=40V, V_{GS}=0V, T_J=55^{\circ}\text{C}$	---	---	5	
IGSS	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	$\pm 100$	nA
gfs	Forward Transconductance	$V_{DS}=5V, I_D=30A$	---	22	---	S
Rg	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1MHz$	---	1.7	3.4	$\Omega$
Qg	Total Gate Charge (4.5V)	$V_{DS}=20V, V_{GS}=10V, I_D=25A$	---	37	---	nC
Qgs	Gate-Source Charge		---	6	---	
Qgd	Gate-Drain Charge		---	7	---	
Td(on)	Turn-On Delay Time	$V_{DD}=30V, V_{GS}=10V, R_G=1\Omega, I_D=25A$	---	12	---	ns
Tr	Rise Time		---	12	---	
Td(off)	Turn-Off Delay Time		---	38	---	
Tf	Fall Time		---	9	---	
Ciss	Input Capacitance	$V_{DS}=20V, V_{GS}=0V, f=1MHz$	---	2400	---	pF
Coss	Output Capacitance		---	192	---	
Crss	Reverse Transfer Capacitance		---	165	---	
Is	Continuous Source Current <sup>1,5</sup>	$V_G=V_D=0V, \text{Force Current}$	---	---	50	A
ISM	Pulsed Source Current <sup>2,5</sup>		---	---	200	A
VSD	Diode Forward Voltage <sup>2</sup>	$V_{GS}=0V, I_S=1A, T_J=25^{\circ}\text{C}$	---	---	1.2	V
trr	Reverse Recovery Time	$I_F=30A, \text{di/dt}=100A/\mu s, T_J=25^{\circ}\text{C}$	---	22	---	nS
Qrr	Reverse Recovery Charge		---	11	---	nC

**Note :**

- 1、The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.
- 2、The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$
- 3、The EAS data shows Max. rating . The test condition is  $V_{DD}=36V, V_{GS}=10V, L=0.1mH, I_{AS}=16A$
- 4、The power dissipation is limited by  $150^{\circ}\text{C}$  junction temperature
- 5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation

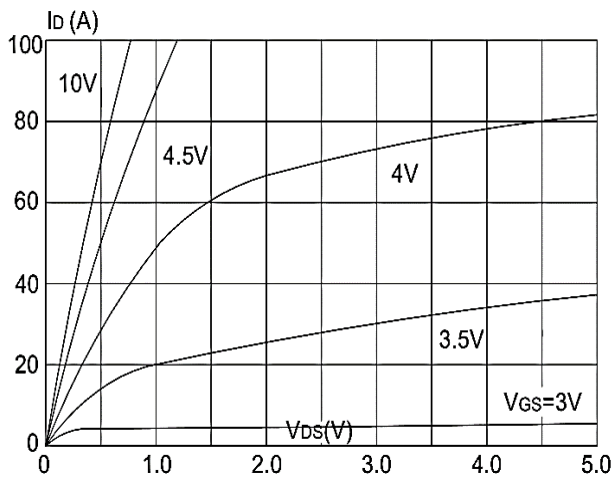
**40V N+P-Channel Enhancement Mode MOSFET**
**Electrical Characteristics ( $T_J=25^{\circ}\text{C}$ , unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V$ , $I_D=-250\mu A$	-40	-44	---	V
$\Delta BV_{DSS}/\Delta T_J$	$BV_{DSS}$ Temperature Coefficient	Reference to $25^{\circ}\text{C}$ , $I_D=-1\text{mA}$	---	-0.023	---	V/ $^{\circ}\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=-10V$ , $I_D=-30A$	---	13	18	m $\Omega$
		$V_{GS}=-4.5V$ , $I_D=-20A$	---	18	25	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$ , $I_D=-250\mu A$	-1.0	-1.6	-2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	4.74	---	mV/ $^{\circ}\text{C}$
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=-40V$ , $V_{GS}=0V$ , $T_J=25^{\circ}\text{C}$	---	---	1	$\mu A$
		$V_{DS}=-40V$ , $V_{GS}=0V$ , $T_J=55^{\circ}\text{C}$	---	---	5	
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS}=\pm 20V$ , $V_{DS}=0V$	---	---	$\pm 100$	nA
$Q_g$	Total Gate Charge (-4.5V)	$V_{DS}=-20V$ , $V_{GS}=-4.5V$ , $I_D=-12A$	---	25	---	nC
$Q_{gs}$	Gate-Source Charge		---	11	---	
$Q_{gd}$	Gate-Drain Charge		---	9.5	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=-15V$ , $R_L=15\Omega$ $I_D=-1A$ , $V_{GEN}=-10V$ , $R_G=6\Omega$	---	48	---	ns
$T_r$	Rise Time		---	24	---	
$T_{d(off)}$	Turn-Off Delay Time		---	88	---	
$T_f$	Fall Time		---	9.6	---	
$C_{iss}$	Input Capacitance	$V_{DS}=-20V$ , $V_{GS}=0V$ , $f=1\text{MHz}$	---	2760	---	pF
$C_{oss}$	Output Capacitance		---	260	---	
$C_{rss}$	Reverse Transfer Capacitance		---	85	---	
$I_S$	Continuous Source Current <sup>1,5</sup>	$V_G=V_D=0V$ , Force Current	---	---	-40	A
$I_{SM}$	Pulsed Source Current <sup>2,5</sup>		---	---	-90	A
$V_{SD}$	Diode Forward Voltage <sup>2</sup>	$V_{GS}=0V$ , $I_S=-1A$ , $T_J=25^{\circ}\text{C}$	---	---	-1.3	V

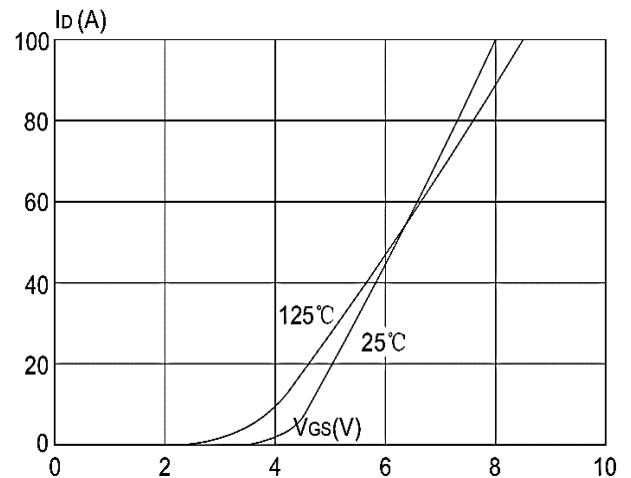
**Note :**

- 1、The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2、The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$
- 3、The EAS data shows Max. rating . The test condition is  $V_{DD}=-32V$ ,  $V_{GS}=-10V$ ,  $L=0.1\text{mH}$ ,  $I_{AS}=-18A$
- 4、The power dissipation is limited by  $150^{\circ}\text{C}$  junction temperature
- 5、The data is theoretically the same as  $I_D$  and  $I_{DM}$  , in real applications , should be limited by total power dissipation.

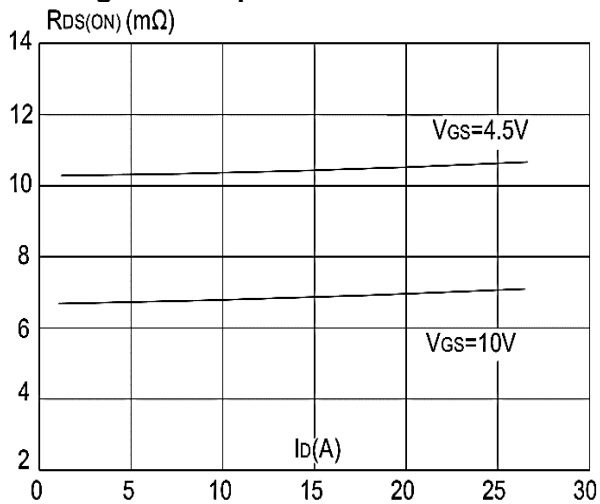
**N-Typical Characteristics**



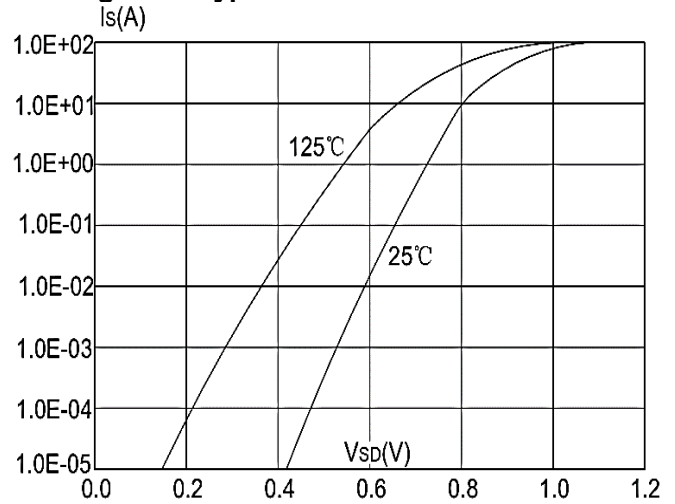
**Figure1: Output Characteristics**



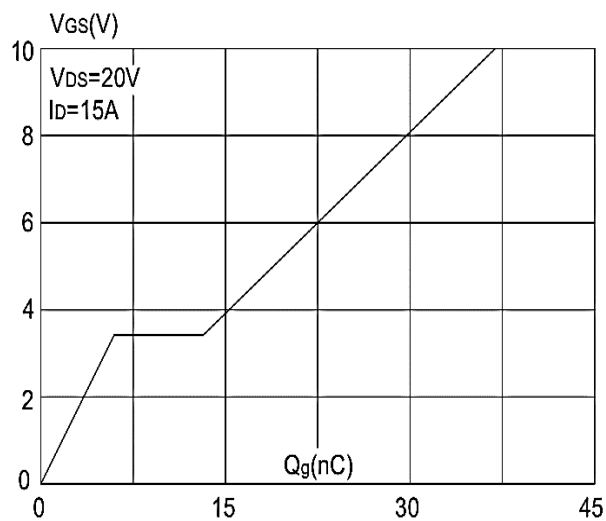
**Figure 2: Typical Transfer Characteristics**



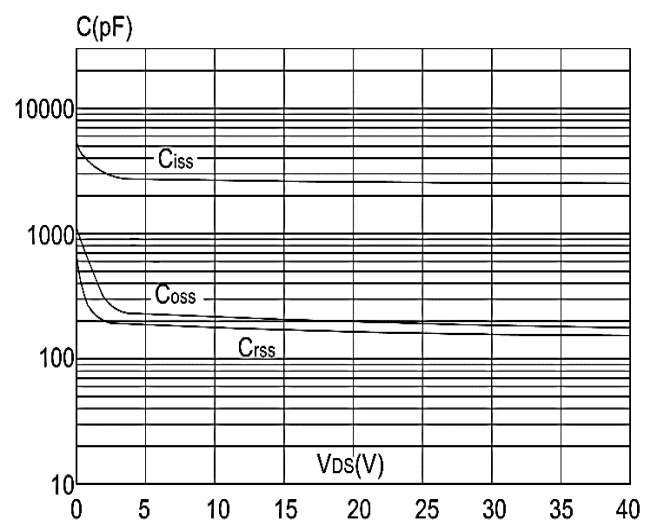
**Figure 3: On-resistance vs. Drain Current**



**Figure 4: Body Diode Characteristics**

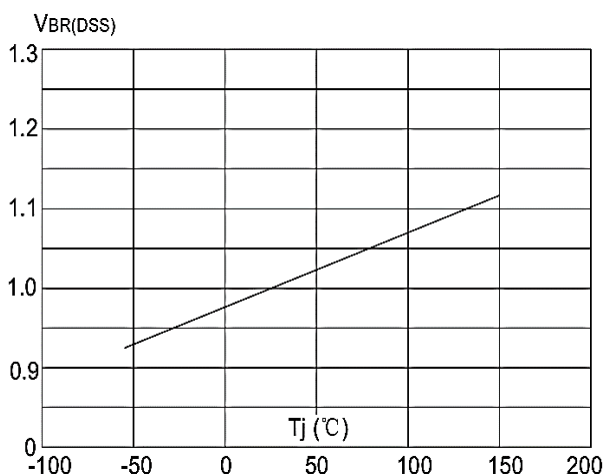


**Figure 5: Gate Charge Characteristics**

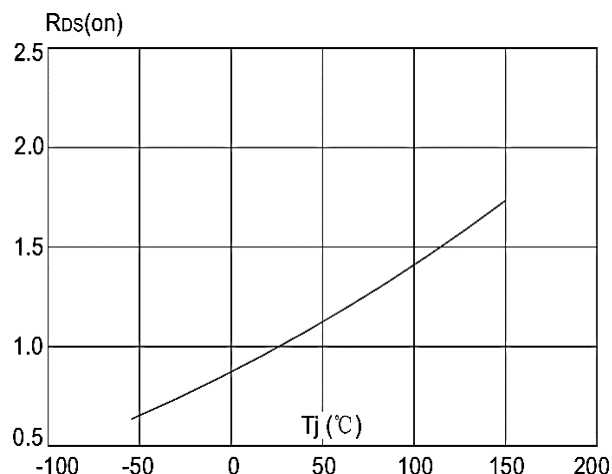


**Figure 6: Capacitance Characteristics**

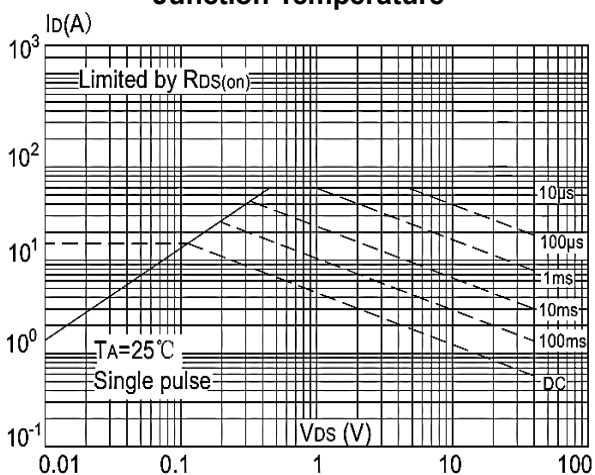
**40V N+P-Channel Enhancement Mode MOSFET**



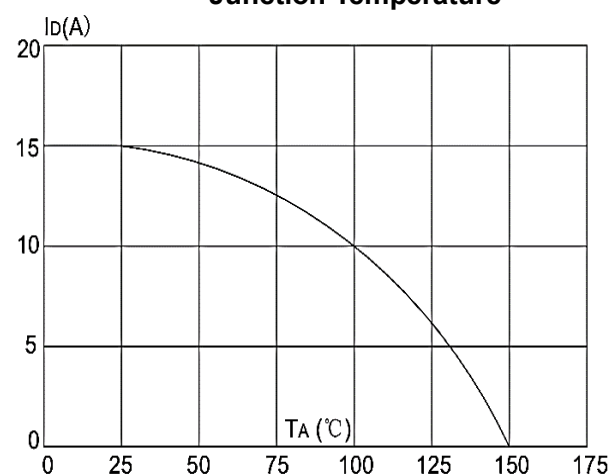
**Figure 7: Normalized Breakdown Voltage vs. Junction Temperature**



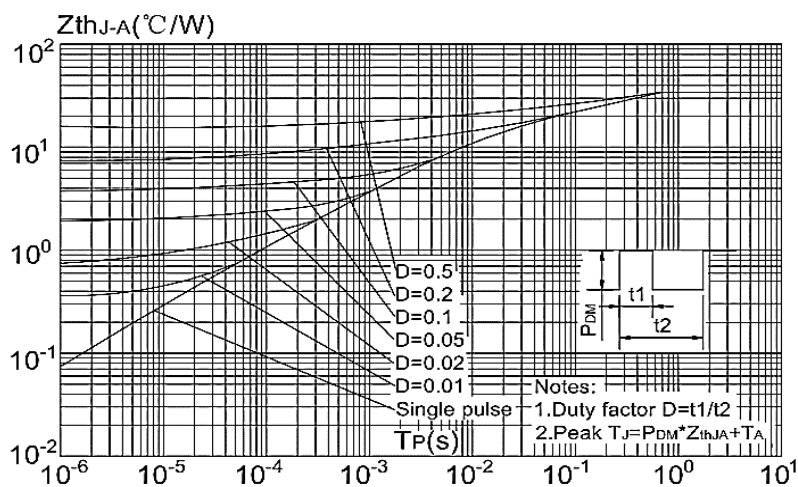
**Figure 8: Normalized on Resistance vs. Junction Temperature**



**Figure 9: Maximum Safe Operating Area vs. Case Temperature**



**Figure 10: Maximum Continuous Drain Current vs. Case Temperature**



**Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case**

P-Typical Characteristics

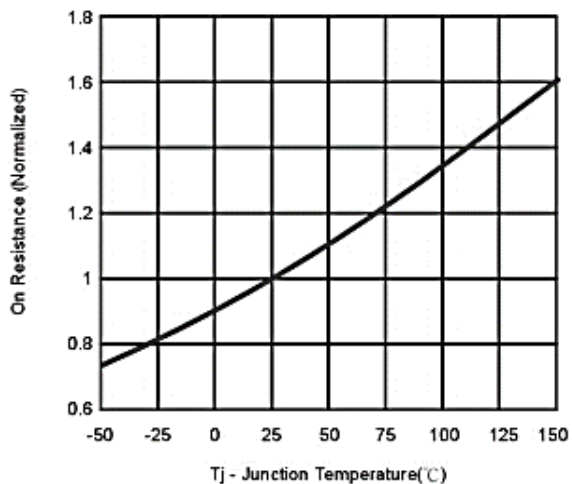


Figure.1 On Resistance Vs Junction Temperature

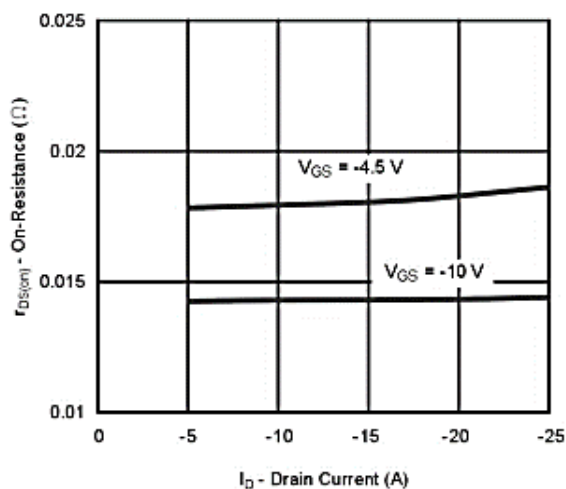


Figure.2: On-Resistance Vs.Drain Current

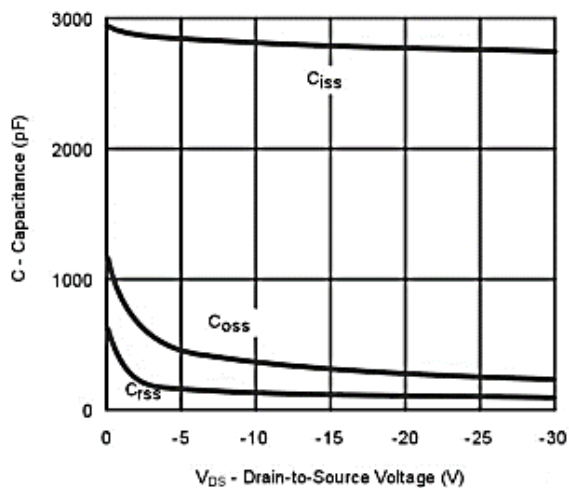


Figure.3: Capacitance

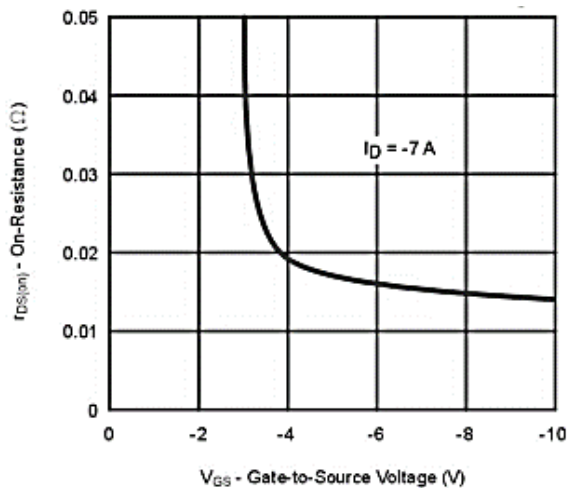


Figure.4: On-Resistance Vs. Gate-to-Source Voltage

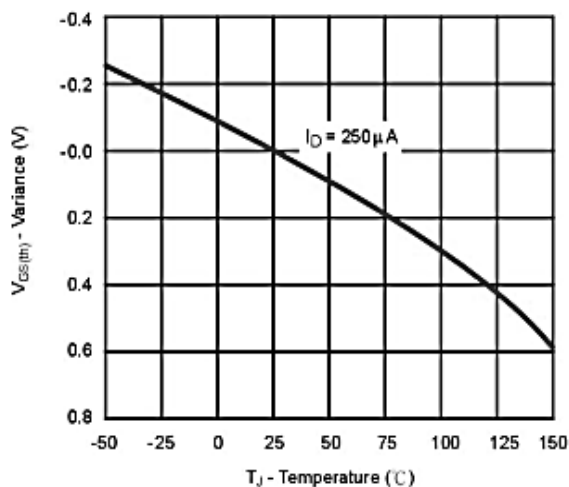


Figure.5: Threshold Voltage

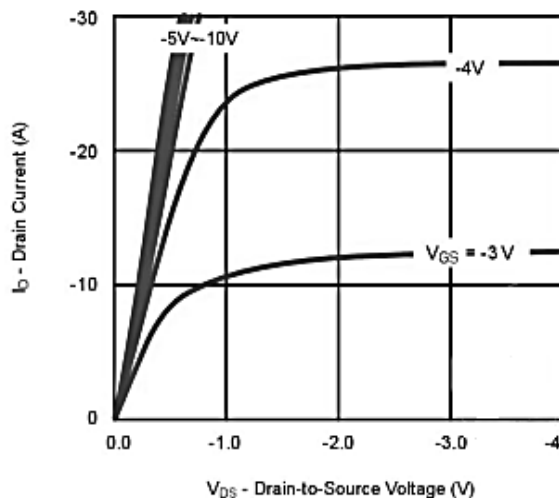


Figure.6: On-Region Characteristics





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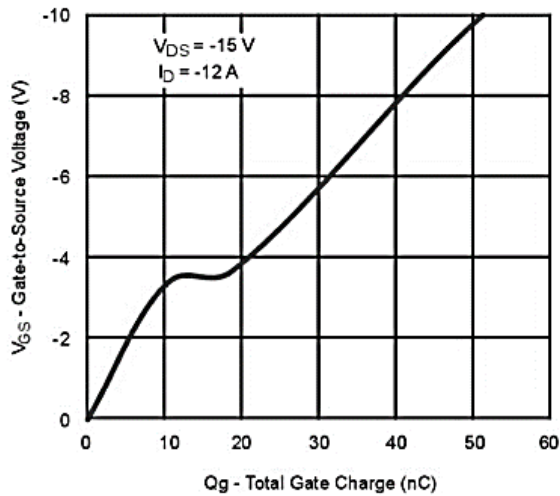


Figure.7: Gate Charge

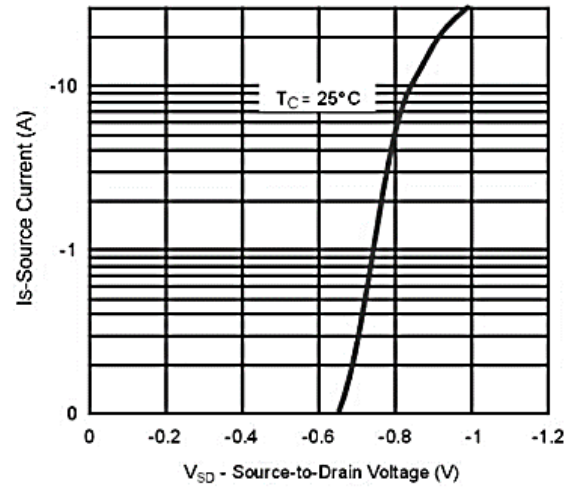


Figure.8: Body-diode Characteristic

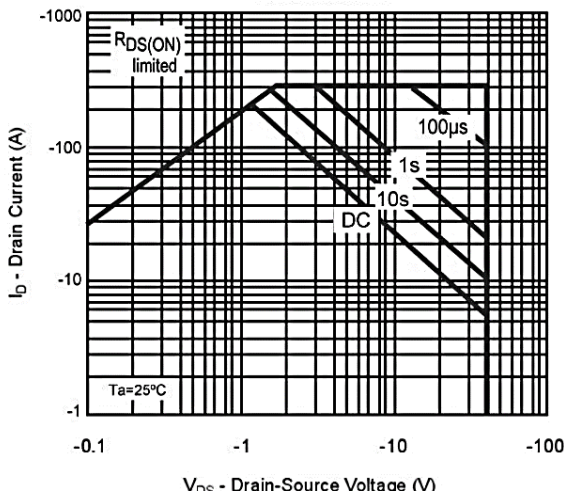


Figure.9: Safe Operating Area

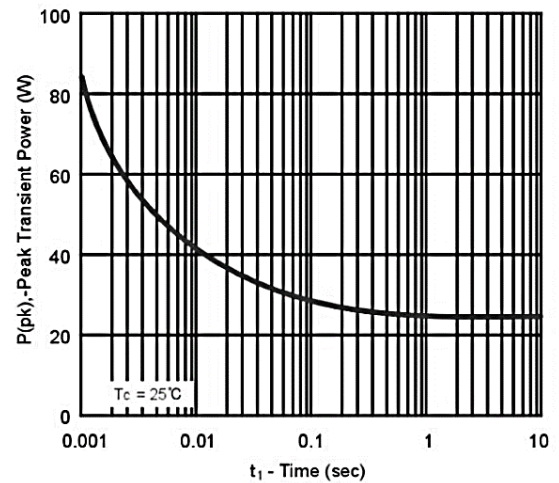


Figure.10: Single Pluse Maximum Power Dissipation

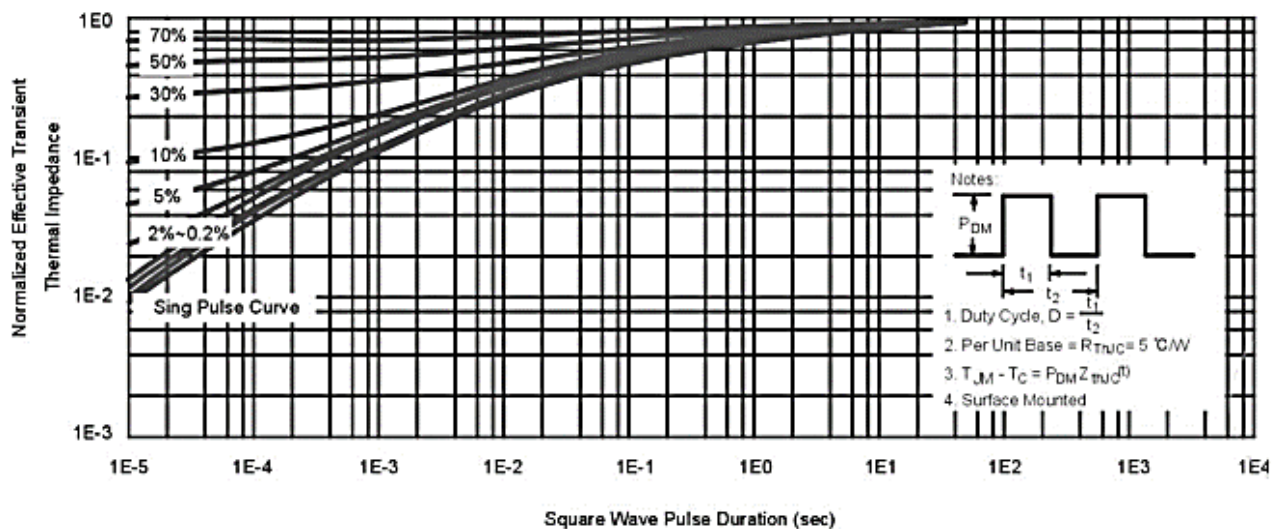
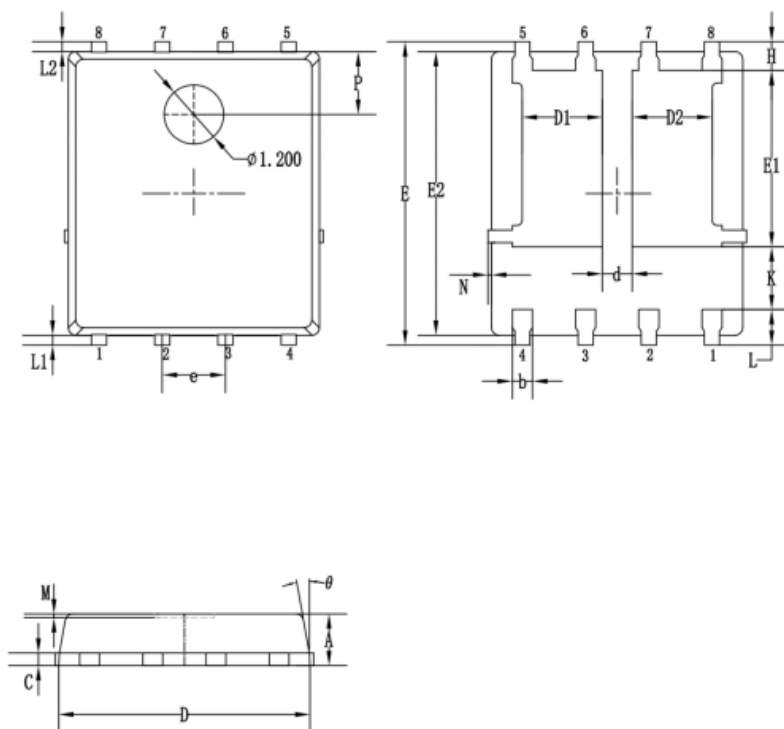


Figure.11: Normalized Maximum Transient Thermal Impedance

Package Mechanical Data-PDFN5X6-8L



Symbol	Dim in mm		
	min	typ	max
A	0.9	1.05	1.2
b	0.3	0.4	0.5
C	0.2	0.25	0.35
D	4.9	5.05	5.2
D1/D2	1.51	1.66	1.81
E	5.9	6.1	6.3
E1	3.3	3.5	3.7
E2	5.6	5.75	5.9
e	1.27BSC		
H	0.48	0.58	0.7
K	1.14	1.27	1.4
L	0.54	0.74	0.84
L1/L2	0.1	0.2	0.3
$\theta$	8°	10°	12°
M	0.08REF		
N	0		0.15
P	1.28REF		
d	0.5	0.6	0.7



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Edition	Date	Change
REV1.0	2024/3/29	Initial release

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