AP30G10GD

100V N+P-Channel Enhancement Mode MOSFET

Description

The AP30G10GD uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

V_{DS} = 100V I_D =32A

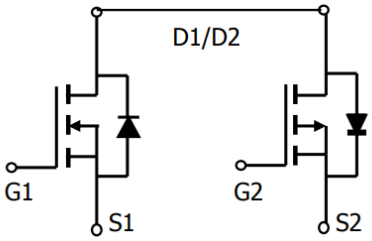
$R_{DS(ON)}$ < 42mΩ @ V_{GS}=10V （**Type：35mΩ**）

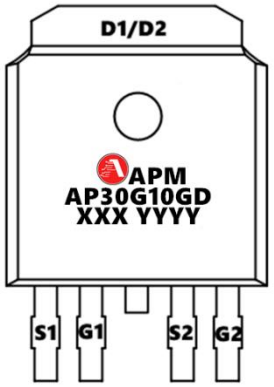
V_{DS} = -100V I_D =-28A

$R_{DS(ON)}$ < 100mΩ @ V_{GS}=-10V（**Type：80mΩ**）

Application

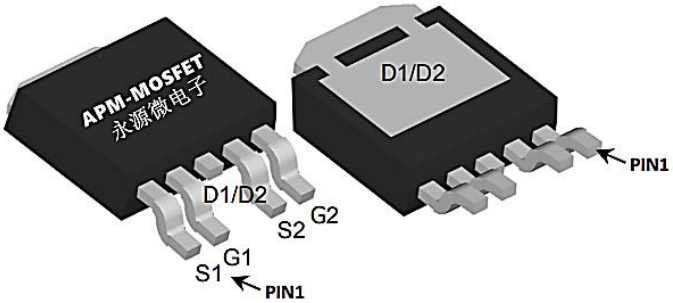
BLDC





Top View

Bottom View



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP30G03GD	TO-252-4L	AP30G03GD XXX YYYY	2500

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	N-Ch	P-Ch	Units
VDS	Drain-Source Voltage	30	-30	V
VGS	Gate-Source Voltage	±20	±20	V
I_D@T_A=25℃	Continuous Drain Current, V_{GS} @ 10V[1]	32	-28	A
I_D@T_A=70℃	Continuous Drain Current, V_{GS} @ 10V[1]	21	-18.1	A
IDM	Pulsed Drain Current[2]	90	-85	A
EAS	Single Pulse Avalanche Energy[3]	138	147	mJ
IAS	Avalanche Current	17	33	A
P_D@T_A=25℃	Total Power Dissipation[4]	46	46	W
TSTG	Storage Temperature Range	-55 to 150		℃
T_J	Operating Junction Temperature Range	-55 to 150		℃
$R_{\theta}JA$	Thermal Resistance Junction-Ambient [1]	62.5		℃/W
$R_{\theta}JC$	Thermal Resistance Junction-Case[1]	2.6		℃/W

N-Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V(BR)DSS	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	100	107	-	V
IDSS	Zero Gate Voltage Drain Current	V_{DS}=100V, V_{GS}=0V,	-	-	1.0	μA
IGSS	Gate to Body Leakage Current	V_{DS}=0V, V_{GS}=±20V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1.0	1.5	2.2	V
RDS(on)	Static Drain-Source on-Resistance	V_{GS}=10V, I_D=10A	-	36	48	mΩ
		V_{GS}=4.5V, I_D=6A	-	39	55	mΩ
Ciss	Input Capacitance	V_{DS}=25V, V_{GS}=0V, f=1.0MHz	-	1964	-	pF
Coss	Output Capacitance		-	90	-	pF
Crss	Reverse Transfer Capacitance		-	74	-	pF
Q_g	Total Gate Charge	V_{DS}=80V, I_D=20A, V_{GS}=4.5V	-	20	-	nC
Qgs	Gate-Source Charge		-	3.1	-	nC
Qgd	Gate-Drain(“Miller”) Charge		-	14	-	nC
td(on)	Turn-on Delay Time	V_{DS}=80V, I_D=20A, R_G=3.1Ω, V_{GS}=4.5V	-	11	-	ns
tr	Turn-on Rise Time		-	91	-	ns
td(off)	Turn-off Delay Time		-	40	-	ns
t_f	Turn-off Fall Time		-	71	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	30	A
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	80	A
VSD	Drain to Source Diode Forward Voltage	V_{GS}=0V, I_S=20A	-	-	1.2	V
trr	Body Diode Reverse Recovery Time	I_F=20A, dI/dt=100A/μs	-	64	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	152	-	nC

Note :

1、The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3、The EAS data shows Max. rating . The test condition is VDD=80V,VGS=10V,L=0.1mH,IAS=17A

4、The power dissipation is limited by 150℃ junction temperature

5、The data is theoretically the same as I D and I DM , in real applications , should be limited by total power dissipation.

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P-Channel Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V(BR)DSS	Drain-Source Breakdown Voltage	VGS=0V, ID=-250μA	-100	-110	-	V
IGSS	Gate-body Leakage current	VDS=0V, VGS=±20V	-	-	±100	nA
IDSS TJ=25°C	Zero Gate Voltage Drain Current	VDS=-100V, VGS = 0V	-	-	-1	μA
IDSS TJ=100°C			-	-	-100	
VGS(th)	Gate-Threshold Voltage	VDS = VGS, ID = -250μA	-1.2	-1.6	-2.5	V
RDS(on)	Drain-Source On-Resistance4	VGS = -10V, ID = -10A	-	80	100	mΩ
		VGS = -4.5V, ID = -6A		88	120	
gfs	Forward Transconductance4	VDS = -10V, ID = -10A	-	30	-	S
Ciss	Input Capacitance	VDS = -50V, VGS = 0V, f = 1MHz	-	3985	-	pF
Coss	Output Capacitance		-	85	-	
Crss	Reverse Transfer Capacitance		-	71	-	
Rg	Gate Resistance	f = 1MHz	-	4	-	Ω
Qg	Total Gate Charge	VGS = -10V, VDS = -50V, ID= -10A	-	65	-	nC
Qgs	Gate-Source Charge		-	10.2	-	
Qgd	Gate-Drain Charge		-	13	-	
td(on)	Turn-On Delay Time	VGS = -10V, VDD = -50V, RG = 3Ω, ID= -10A	-	12.8	-	ns
tr	Rise Time		-	30	-	
td(off)	Turn-Off Delay Time		-	82	-	
tf	Fall Time		-	61	-	
trr	Body Diode Reverse Recovery Time	IF = -10A,dI/dt= 100A/μs	-	62	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	56	-	nC
VSD	Diode Forward Voltage4	IS = -10A, VGS = 0V	-	-	-1.2	V
IS	Continuous Source Current TC= 25°C	-	-	-	-18	A

Note :

1、The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3、The EAS data shows Max. rating . The test condition is V DD =-72V,VGS =-10V,L=0.1mH,IAS =-33A

4、The power dissipation is limited by 150℃ junction temperature

5、The data is theoretically the same as I D and I DM , in real applications , should be limited by total power dissipation.

N-Typical Characteristics

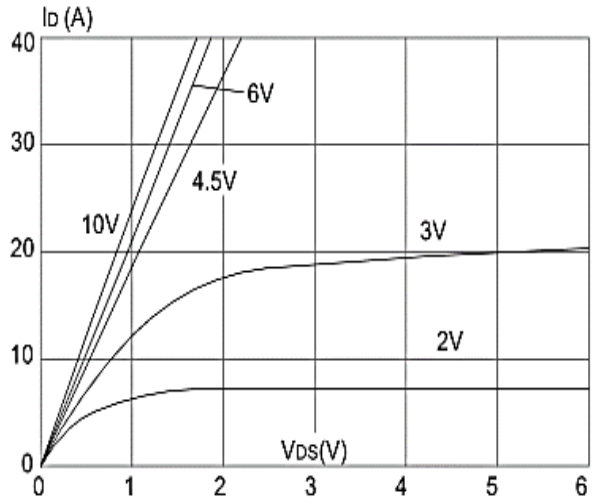


Figure1: Output Characteristics

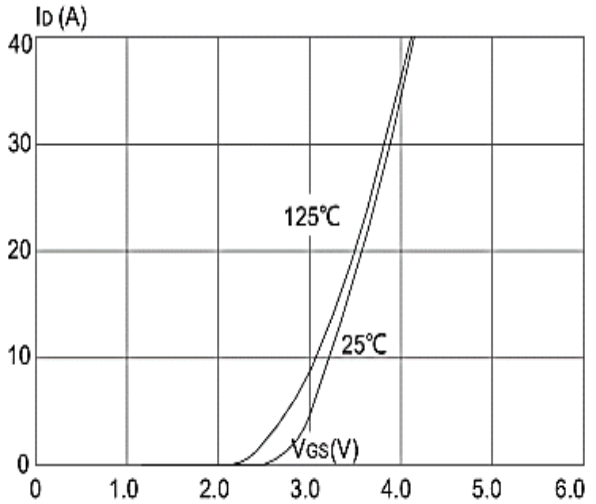


Figure 2: Typical Transfer Characteristics

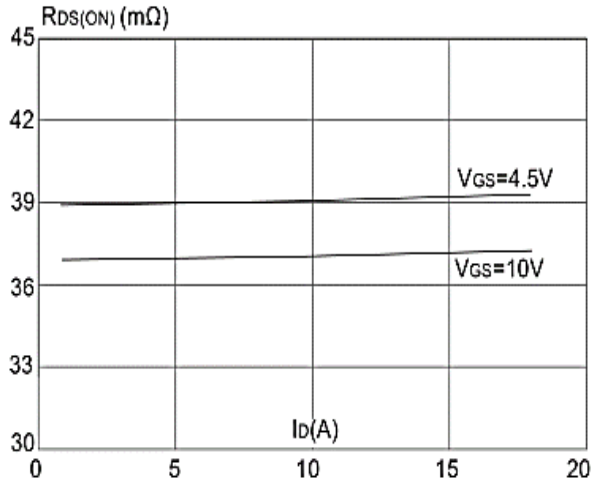


Figure 3:On-resistance vs. Drain Current

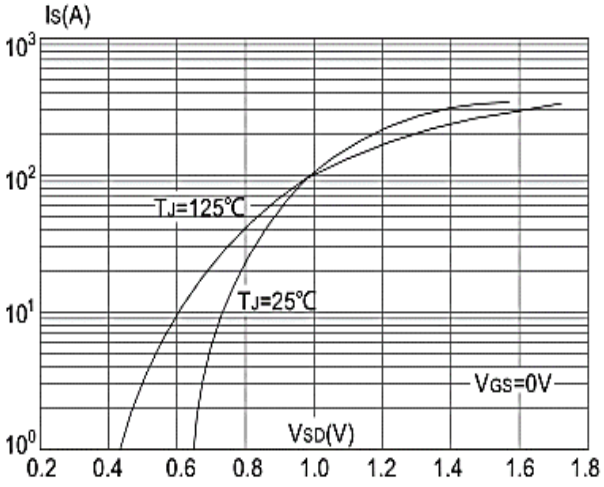


Figure 4: Body Diode Characteristics

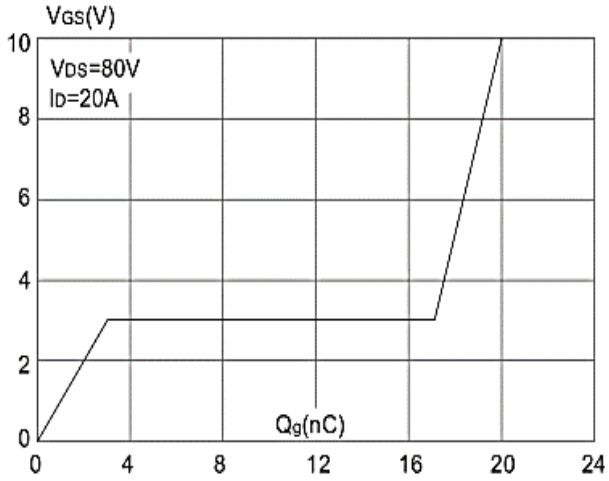


Figure 5: Gate Charge Characteristics

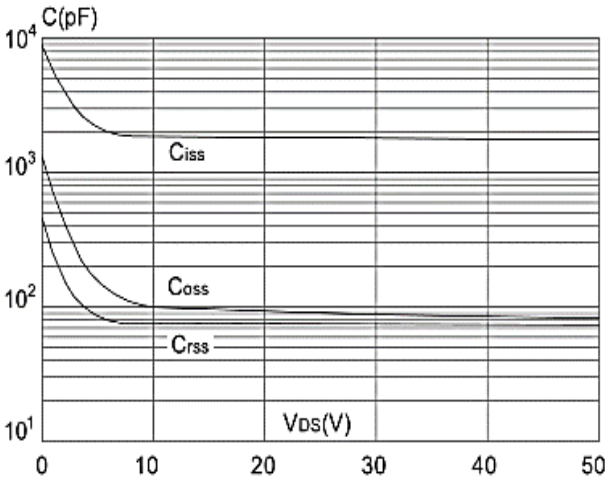


Figure 6: Capacitance Characteristics

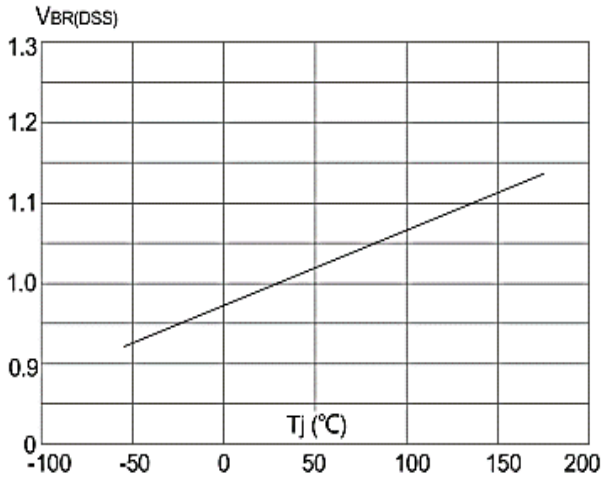


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

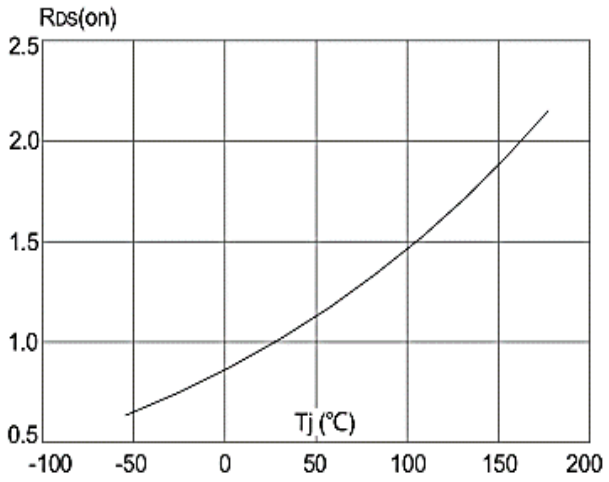


Figure 8: Normalized on Resistance vs Junction Temperature

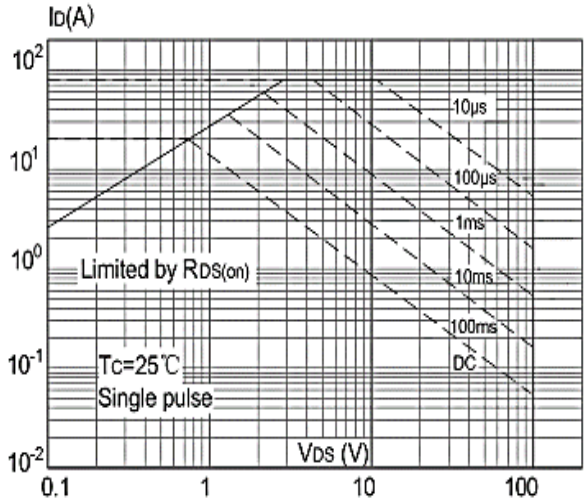


Figure 9: Maximum Safe Operating Area vs. Case Temperature

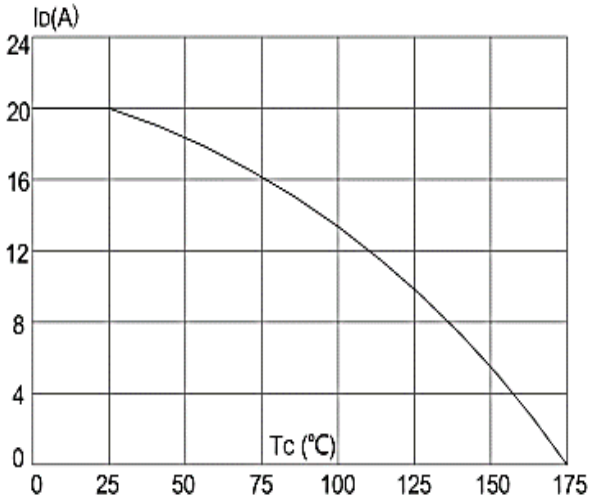


Figure 10: Maximum Continuous Drain Current

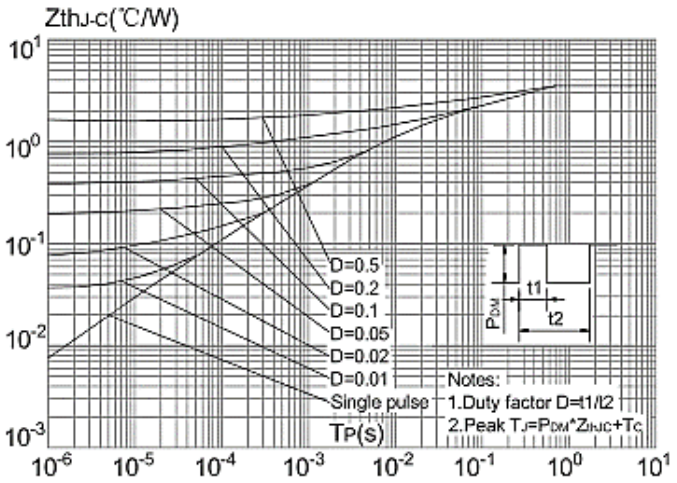


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

P- Typical Characteristics

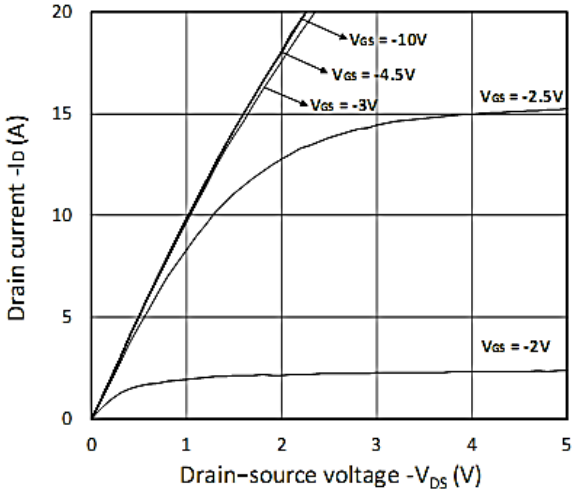


Figure 1. Output Characteristics

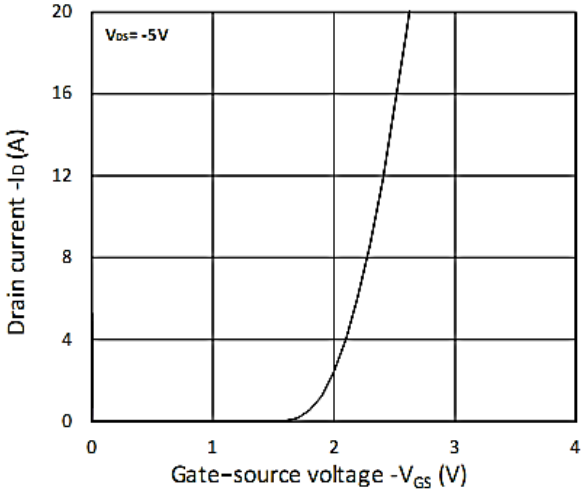


Figure 2. Transfer Characteristics

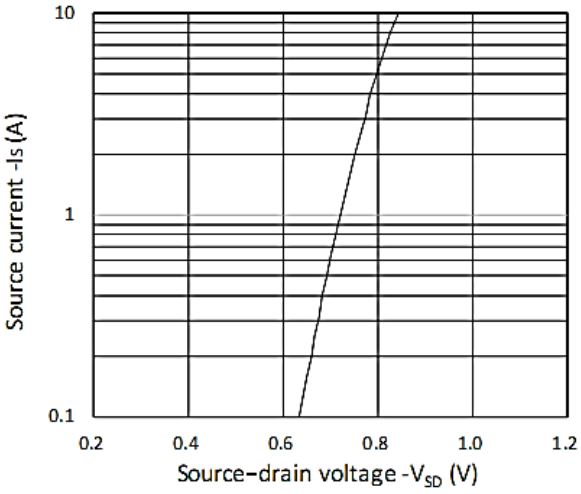


Figure 3. Forward Characteristics of Reverse

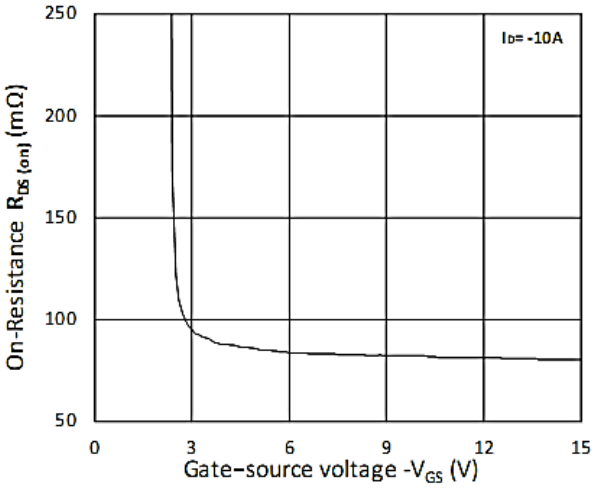


Figure 4. RDS(ON) vs. VGS

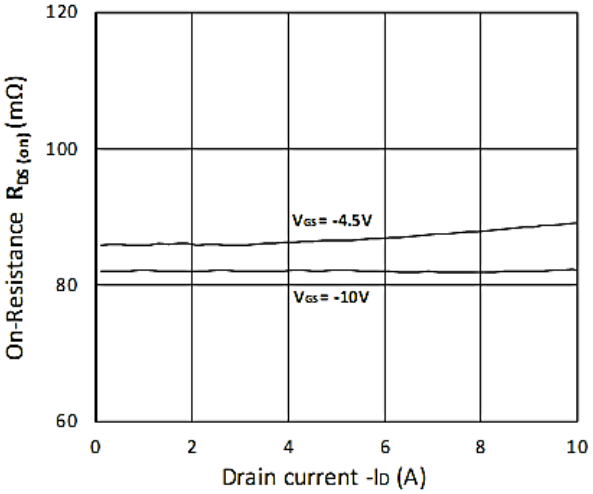


Figure 5. RDS(ON) vs. ID

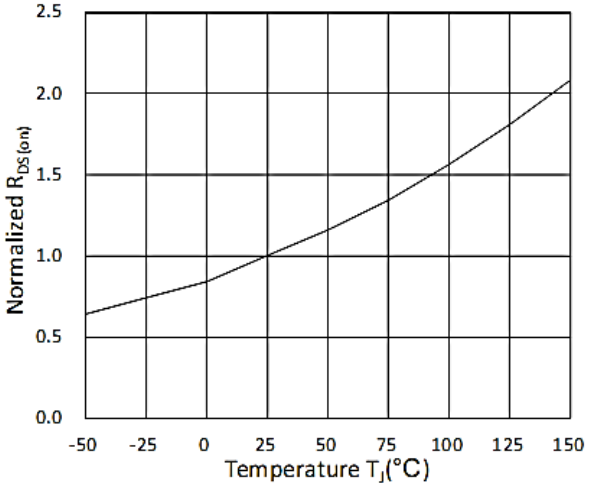


Figure 6. Normalized RDS(on) vs. Temperature

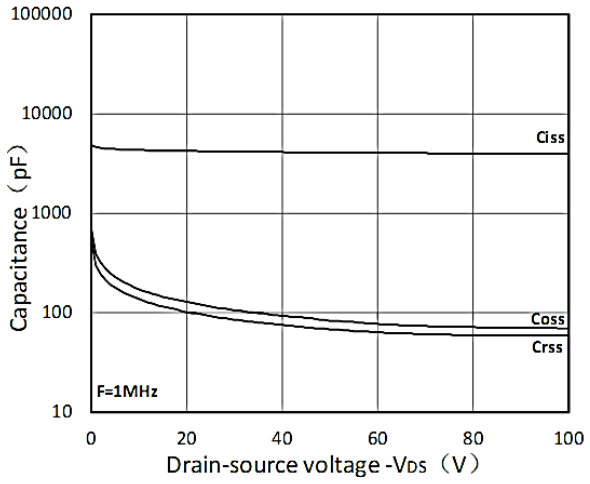


Figure 7. Capacitance Characteristics

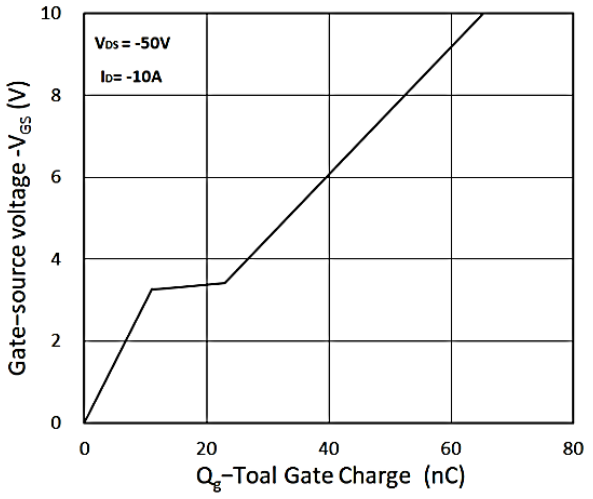


Figure 8. Gate Charge Characteristics

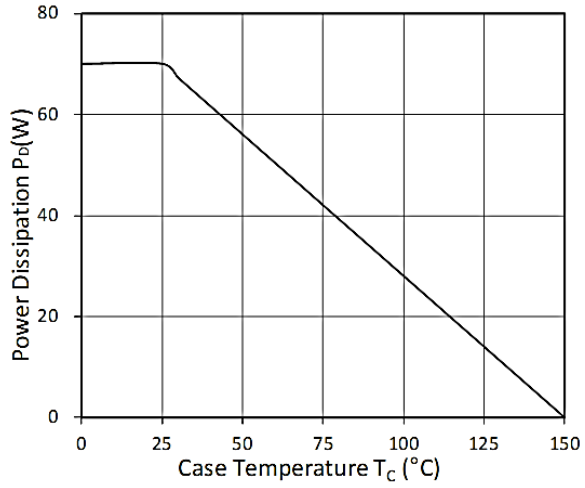


Figure 9. Power Dissipation

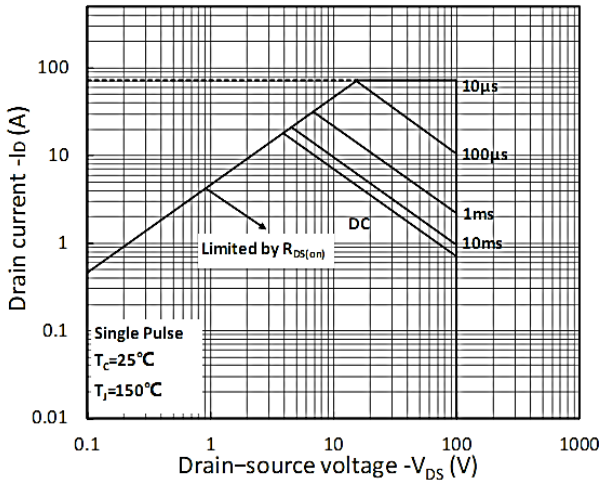


Figure10. Safe Operating Area

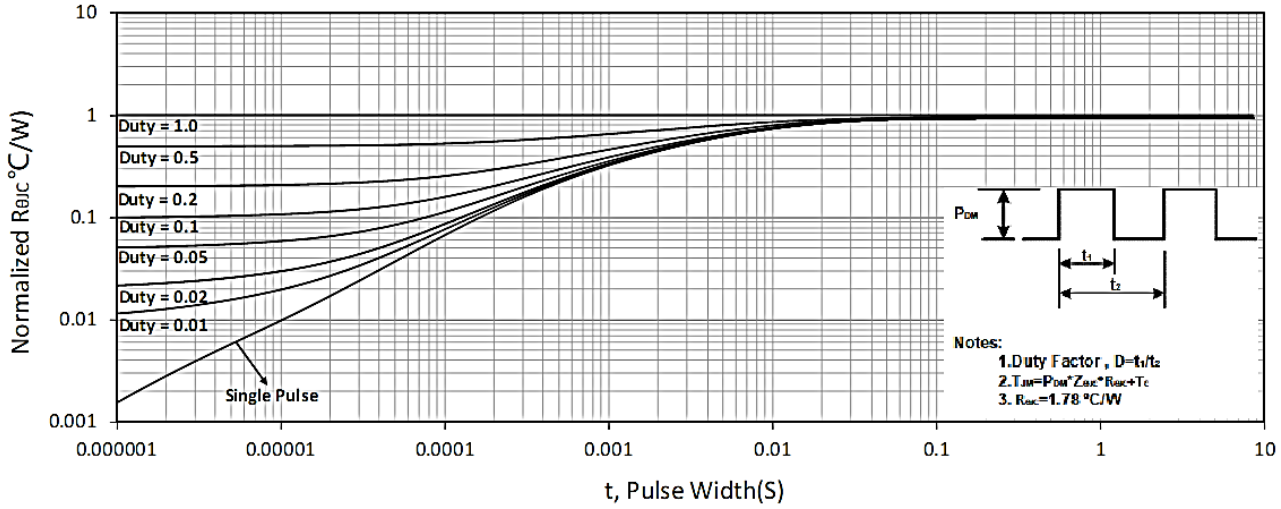
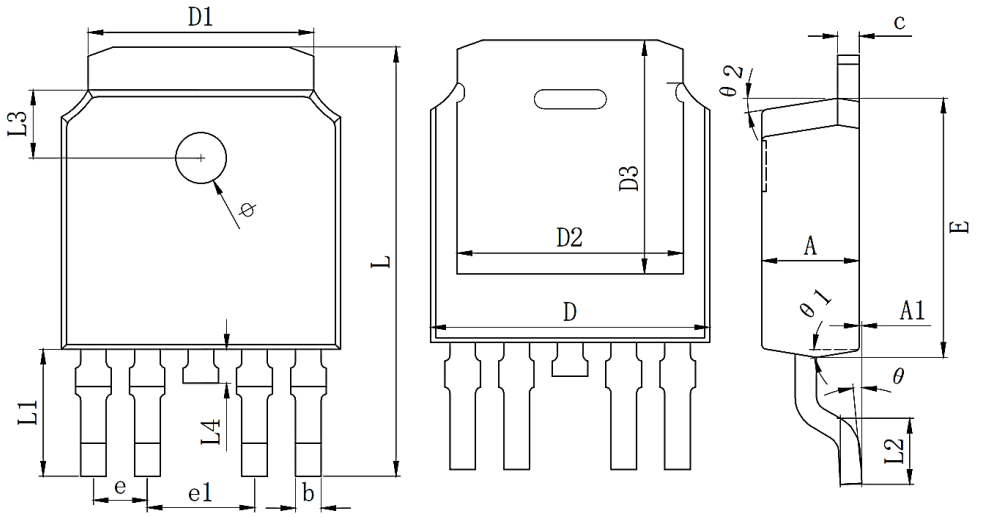


Figure 11. Normalized Maximum Transient Thermal Impedance

Package Mechanical Data:TO-252-4L



Symbol	Dim in mm		
	Min	Typ	Max
A	2.1	2.3	2.5
A1	0	0.064	0.128
b	0.5	0.6	0.7
c	0.45	0.52	0.6
D	6.4	6.6	6.8
D1	5.33REF		
D2	5.06REF		
D3	5.25REF		
E	5.9	6.1	6.3
e	1.27TYP		
e1	2.54TYP		
L	9.8	10.1	10.4
L1	2.888REF		
L2	1.4	1.5	1.7
L3	1.65REF		
L4	0.6	0.8	1
ϕ	1.1	1.2	1.3
θ	0°		10°
θ1	5°		10°
θ2	5°		10°

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Edition	Date	Change
RVE1.0	2023/1/12	Initial release