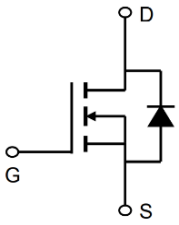
AP30N65MP

650V N-Channel Enhancement Mode MOSFET

Description

The AP30N65MP is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.



General Features

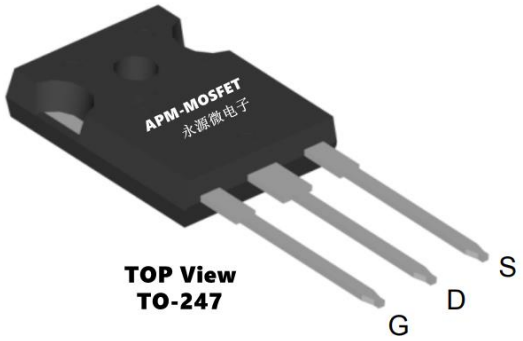
V_{DS} = 650V I_D =30A

$R_{DS(ON)}$ < 270mΩ @ V_{GS}=10V （Type：230mΩ）

Application

Uninterruptible Power Supply(UPS)

Power Factor Correction (PFC)



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP30N65MP	TO-247-3L	AP30N65MP XXX YYYY	360

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Value	Unit
VDSS	Drain-Source Voltage (V_{GS} = 0V)	650	V
ID@TC=25°C	Continuous Drain Current	30	A
ID@TC=100°C	Continuous Drain Current	16	A
IDM	Pulsed Drain Current (note1)	100	A
VGS	Gate-Source Voltage	±30	V
E_{AS}	Single Pulse Avalanche Energy (note2)	1500	mJ
P_D	Power Dissipation (T_C = 25ºC)	300	W
TJ, Tstg	Operating Junction and Storage Temperature Range	-55~+150	ºC
RthJC	Thermal Resistance, Junction-to-Case	0.42	ºC/W
RthJA	Thermal Resistance, Junction-to-Ambient	62.5	ºC/W

Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V(BR)DSS	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	650	690	--	V
IDSS	Zero Gate Voltage Drain Current	V_{DS} = 500V, V_{GS} = 0V, T_J = 25ºC	--	--	1	μA
IGSS	Gate-Source Leakage	V_{GS} = ±30V	--	--	±100	nA
VGS(th)	Gate-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	2.0	3.0	4.0	V
RDS(on)	Drain-Source On-Resistance (Note3)	V_{GS} = 10V, I_D = 9A	--	230	270	mΩ
C_{iss}	Input Capacitance	V_{GS} = 0V, V_{DS} = 25V, f= 1.0MHz	--	3450	--	pF
C_{oss}	Output Capacitance		--	214	--	
C_{rss}	Reverse Transfer Capacitance		--	10	--	
Q_g	Total Gate Charge	VDD =400V,ID=30A, VGS =10V	--	64	--	nC
Q_{gs}	Gate-Source Charge		--	17	--	
Q_{gd}	Gate-Drain Charge		--	23	--	
td(on)	Turn-on Delay Time	VDS=250V, ID=30A, VGS =10V	--	37	--	ns
t_r	Turn-on Rise Time		--	64	--	
td(off)	Turn-off Delay Time		--	87	--	
t_f	Turn-off Fall Time		--	46	--	
I_S	Continuous Body Diode Current	T_C = 25 ºC	--	--	30	A
ISM	Pulsed Diode Forward Current		--	--	100	
V_{SD}	Body Diode Voltage	T_J = 25ºC, I_{SD} = 30A, V_{GS} = 0V	--	--	1.5	V
trr	Reverse Recovery Time	V_{GS} = 0V,I_S = 30A, di_F/dt =100A /μs	--	490	--	ns
Q_{rr}	Reverse Recovery Charge		--	6246	--	μC

Note :

1、The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.

2、The EAS data shows Max. rating . L=4.1Mh IAS=30A, VDD=50V, RG=25Ω, Starting TJ = 25 ºC

3、The test condition is Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%

4、The power dissipation is limited by 150℃ junction temperature

5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics

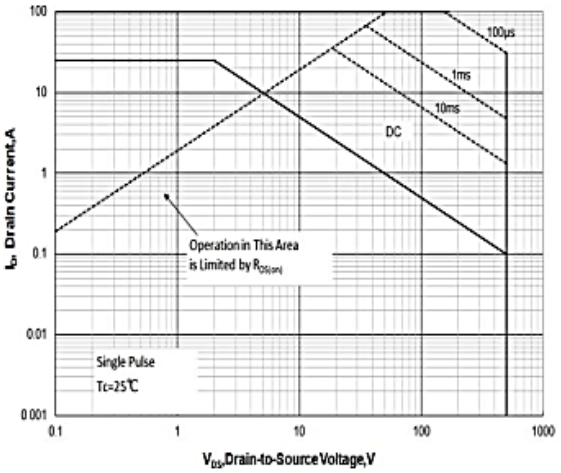


Figure 1 Maximum Forward Bias Safe Operating Area

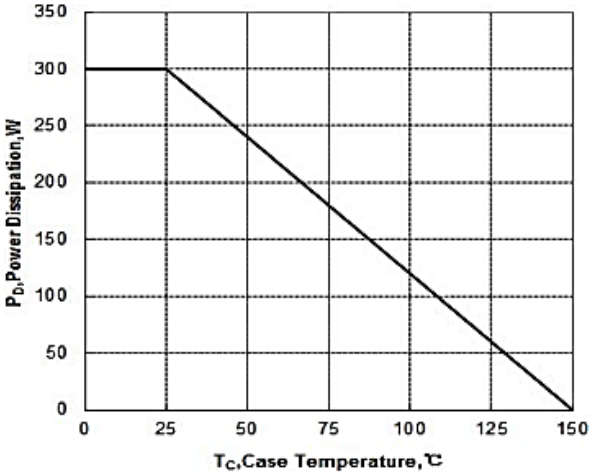


Figure 2 Maximum Power dissipation vs Case Temperature

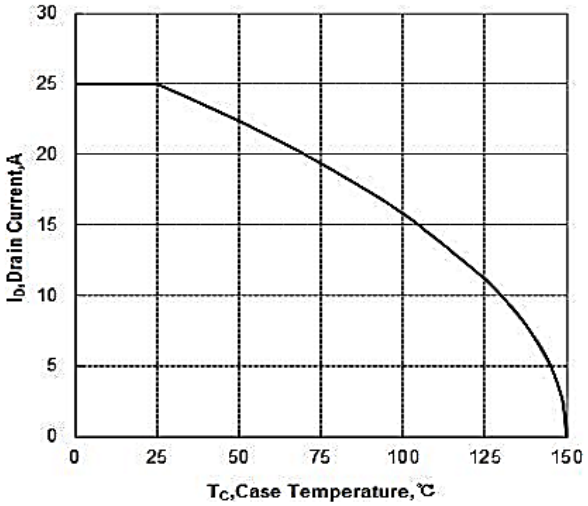


Figure3 MaximumContinuousDrainCurrentvs CaseTemperature

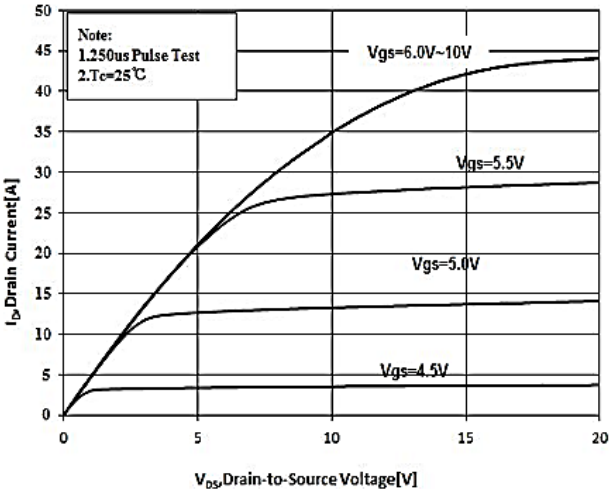


Figure 4 Typical Output Characteristics

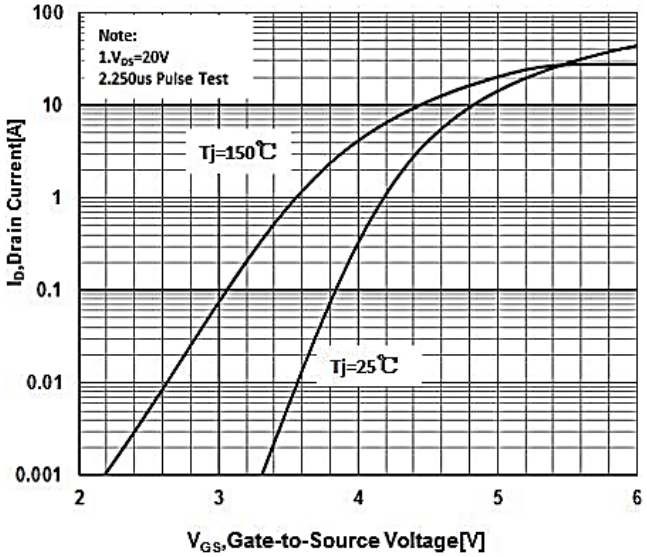


Figure 6 TypicalTransferCharacteristics

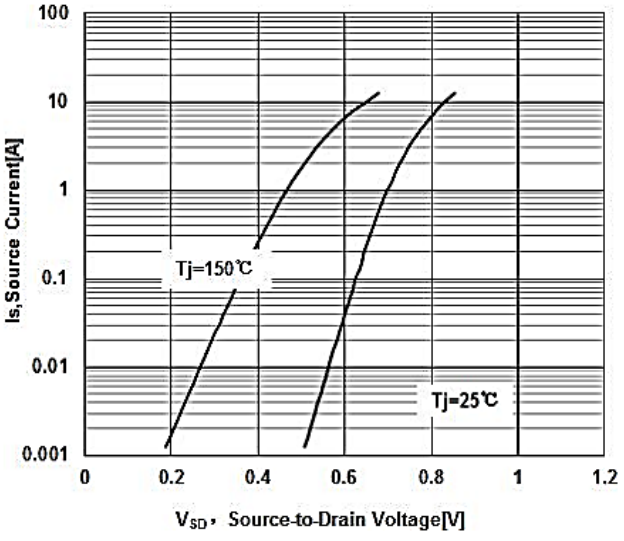


Figure7 TypicalBody DiodeTransfer Characteristics

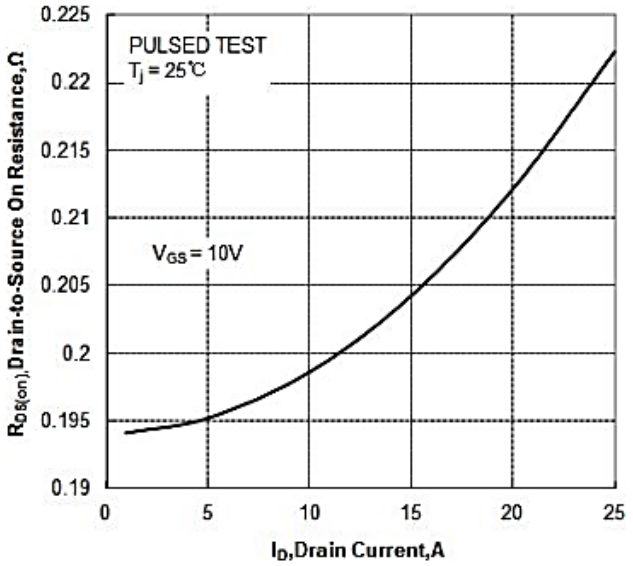


Figure 8 Typical Drain to Source ON Resistance vs JunctionTemperature

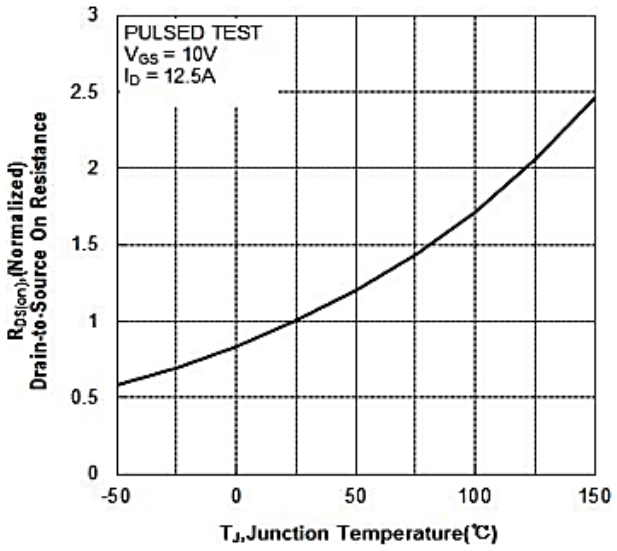


Figure9 TypicalDrianto Sourceon Resistance vs Drain Current

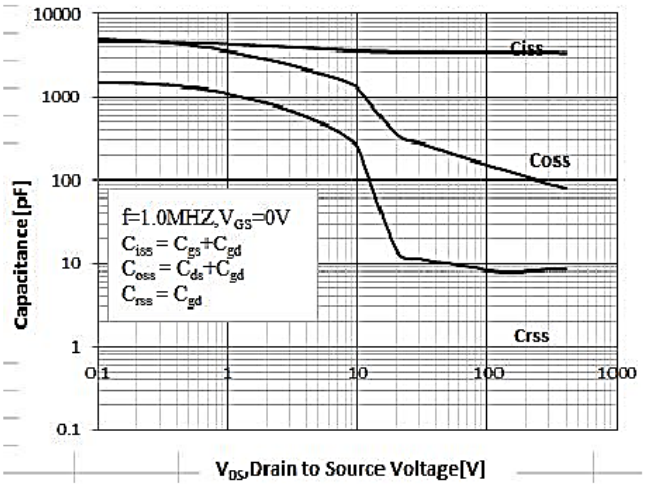


Figure11 TypicalCapacitancevs Drainto SourceVoltage

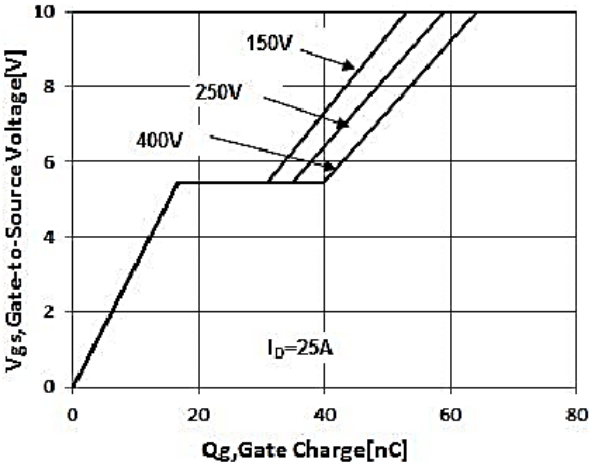


Figure12 TypicalGateChargevs Gateto SourceVoltage

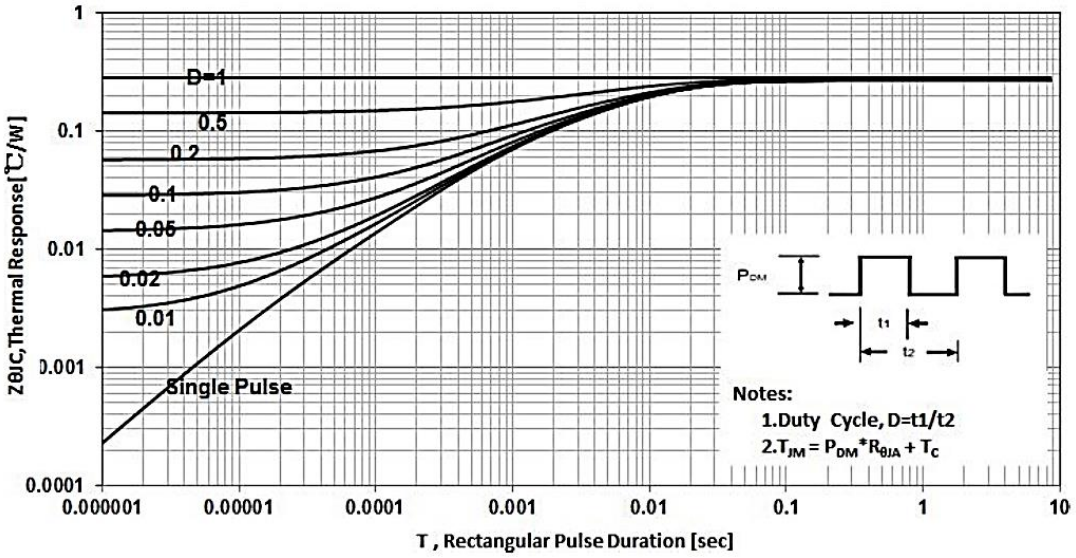
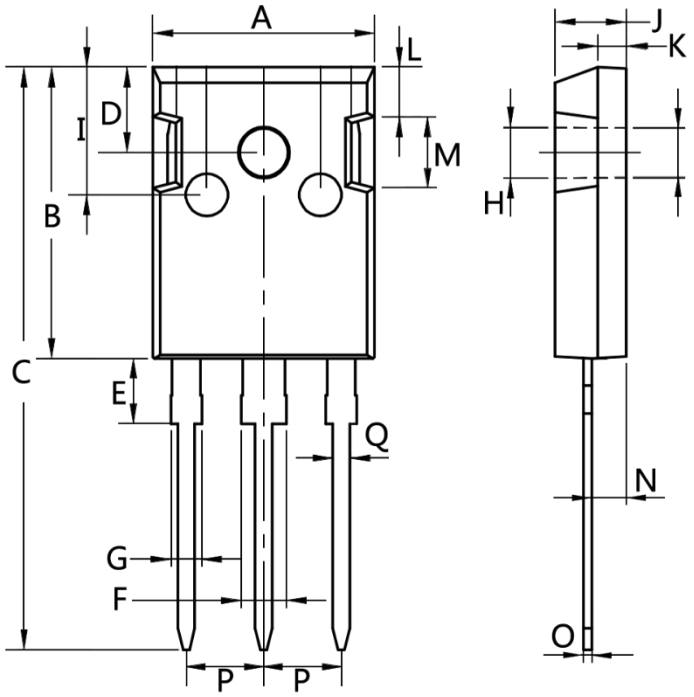


Figure 5 Maximum Effective Thermal Impedance , Junction to Case

Package Mechanical Data-TO-247-3L



Dim.	Min.	Max.
A	15.0	16. 0
B	20.0	21.0
C	41.0	42.0
D	5.0	6.0
E	4.0	5.0
F	2.5	3.5
G	1.75	2.5
H	3.0	3.5
I	8.0	10.0
J	4.9	5.1
K	1.9	2.1
L	3.5	4.0
M	4.75	5.25
N	2.0	3.0
O	0.55	0.75
P	Typ 5.08	
Q	1.2	1.3

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Edition	Date	Change
REV1.0	2024/1/31	Initial release