# AP320N10BTLG2

## 100V N-Channel Enhancement Mode MOSFET

### Description

The AP320N10BTLG2 uses advanced **APM-SGT II** technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 10V. This device is suitable for use as a Battery protection or in other Switching application.

### General Features

$V_{DS}$ = 100V $I_D$ =320A

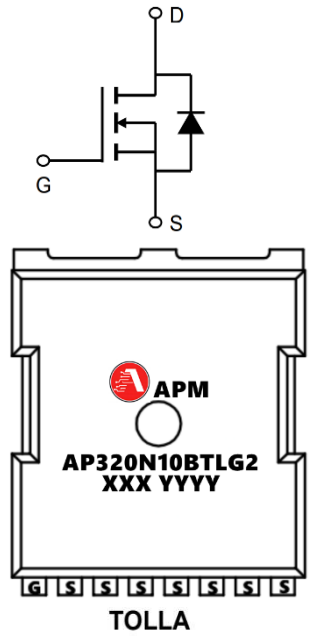
$R_{DS(ON)}$ < 1.6mΩ @ $V_{GS}$=10V **(Type：1.25mΩ)**

### Application

Isolated DC

Motor control

Synchronous-rectification

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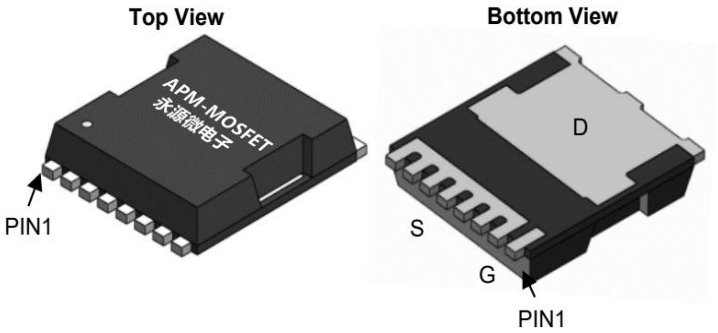



### Package Marking and Ordering Information

| Product ID | Pack | Marking | Qty(PCS) |
|---|---|---|---|
| AP320N10BTLG2 | TOLLA-8L | AP320N10BTLG2 XXXYYYY | 2000 |

### Absolute Maximum Ratings ($T_C$=25℃unless otherwise noted)

| Symbol | Parameter | Rating | Units |
|---|---|---|---|
| VDS | Drain-Source Voltage | 100 | V |
| VGS | Gate-Source Voltage | ±20 | V |
| $I_D$@$T_C$=25℃ | Continuous Drain Current, $V_{GS}$ @ 10V | 320 | A |
| $I_D$@$T_C$=100℃ | Continuous Drain Current, $V_{GS}$ @ 10V | 210 | A |
| IDM | Pulsed Drain Current | 1248 | A |
| EAS | Single Pulse Avalanche Energy | 2340 | mJ |
| IAS | Avalanche Current | 53.4 | A |
| $P_D$@$T_C$=25℃ | Total Power Dissipation[4] | 390.6 | W |
| TSTG | Storage Temperature Range | -55 to 175 | ℃ |
| $T_J$ | Operating Junction Temperature Range | -55 to 175 | ℃ |
| $R_{\theta}JA$ | Thermal Resistance Junction-Ambient | 40 | ℃/W |
| $R_{\theta}JC$ | Thermal Resistance Junction-Case | 0.32 | ℃/W |

## Electrical Characteristics ($T_C$=25℃unless otherwise noted)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| V(BR)DSS | Drain-Source Breakdown Voltage | $V_{GS}$ = 0V, $I_D$ = 250μA | 100 | 105 | - | V |
| IGSS | Gate-body Leakage current | $V_{DS}$ = 0V, $V_{GS}$ = ±20V | - | - | ±100 | nA |
| IDSS | Zero Gate Voltage Drain Current $T_J$=25°C | $V_{DS}$ = 100V, $V_{GS}$ = 0V | - | - | 1 | μA |
| IDSS | Zero Gate Voltage Drain Current$T_J$=100°C | | - | - | 100 | |
| VGS(th) | Gate-Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250μA | 2.0 | 3.0 | 4.0 | V |
| RDS(on) | Drain-Source on-Resistance[4] | $V_{GS}$ = 10V, $I_D$ = 20A | - | 1.25 | 1.6 | mΩ |
| gfs | Forward Transconductance[4] | $V_{DS}$ = 10V, $I_D$ =20A | - | 84 | - | S |
| Ciss | Input Capacitance | $V_{DS}$ = 50V, $V_{GS}$ =0V, f =1MHz | - | 14300 | - | pF |
| Coss | Output Capacitance | | - | 2120 | - | |
| Crss | Reverse Transfer Capacitance | | - | 50 | - | |
| $R_g$ | Gate Resistance | f=1MHz | - | 2.8 | - | Ω |
| $Q_g$ | Total Gate Charge | $V_{GS}$ = 10V, $V_{DS}$ = 50V, $I_D$= 20A | - | 250 | - | nC |
| Qgs | Gate-Source Charge | | - | 53 | - | |
| Qgd | Gate-Drain Charge | | - | 77 | - | |
| td(on) | Turn-on Delay Time | $V_{GS}$ =10V, $V_{DD}$ = 50V, $R_G$ = 3Ω, $I_D$= 20A | - | 41 | - | ns |
| $t_r$ | Rise Time | | - | 88 | - | |
| td(off) | Turn-off Delay Time | | - | 163 | - | |
| $t_f$ | Fall Time | | - | 98 | - | |
| trr | Body Diode Reverse Recovery Time | $I_F$=20A, di/dt = 100A/μs | - | 106 | - | ns |
| $Q_{rr}$ | Body Diode Reverse Recovery Charge | | - | 245 | - | nC |
| VSD | Diode Forward Voltage[4] | $I_S$ = 20A, $V_{GS}$ = 0V | - | - | 1.2 | V |
| IS | Continuous Source Current $T_C$=25°C | | - | - | 312 | A |

**Notes:**

1、The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%

3、The EAS data shows Max. rating . The test condition is $V_{DD}$=90V, $V_{GS}$=10V, L=1.0mH, $I_{AS}$=50A

4、The power dissipation is limited by 150°C junction temperature

5、The data is theoretically the same as $I_D$ and $I_{DM}$ , in real applications , should be limited by total power dissipation.

## Typical Characteristics

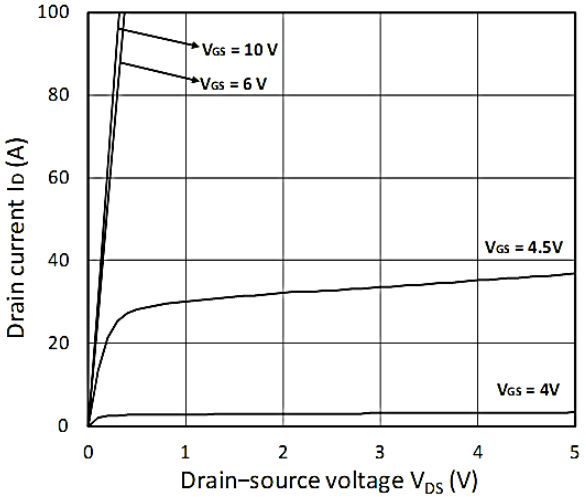



Figure 1. Output Characteristics

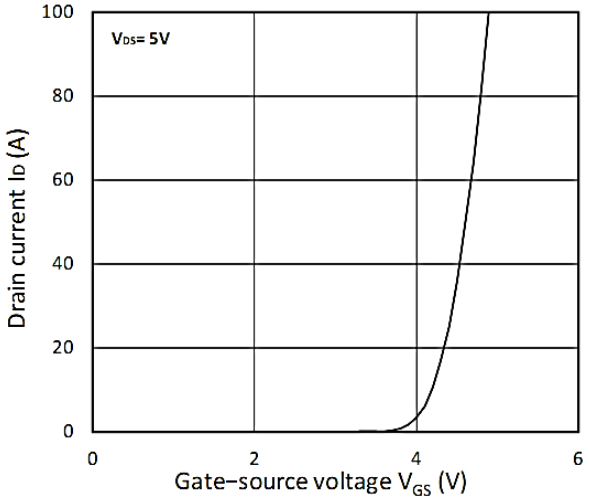



Figure 2. Transfer Characteristics

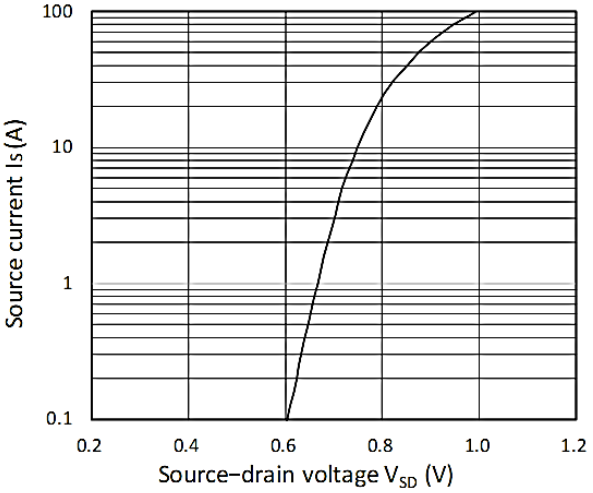



Figure 3. Forward Characteristics of Reverse

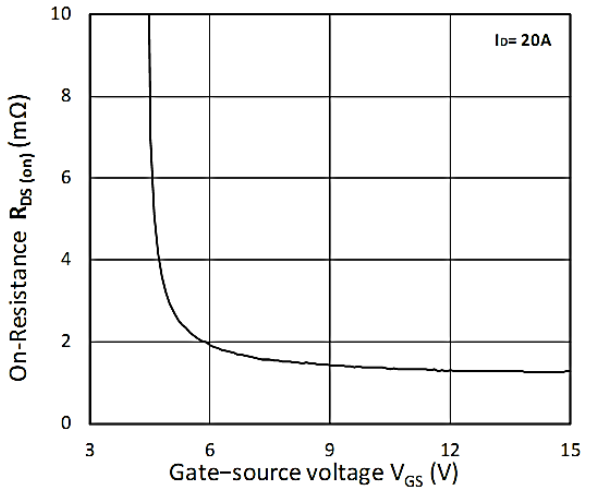



Figure 4. RDS(ON) vs. VGS

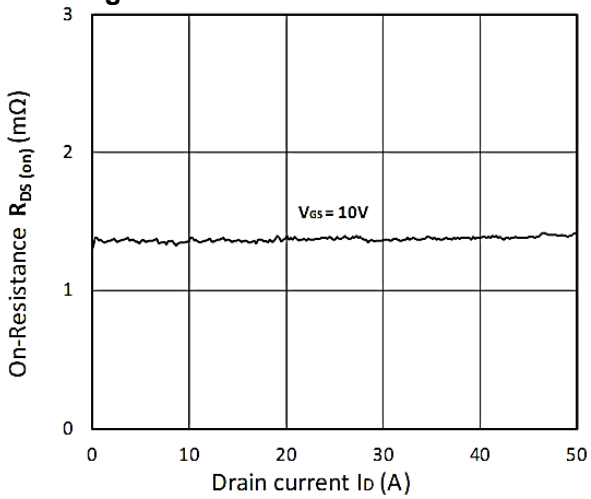



Figure 5. RDS(ON) vs. ID

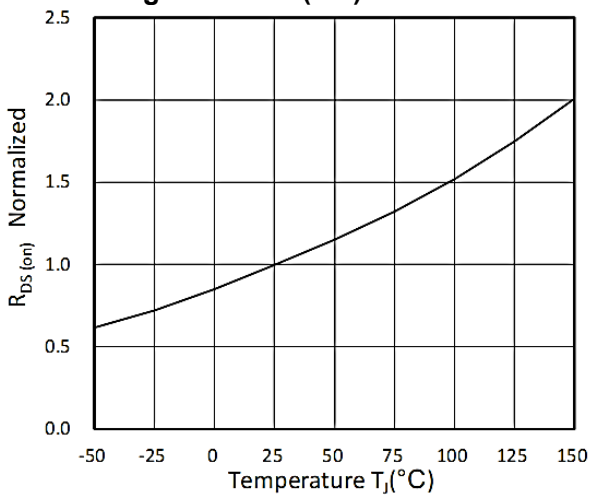



Figure 6. Normalized R DS(on) vs. Temperature

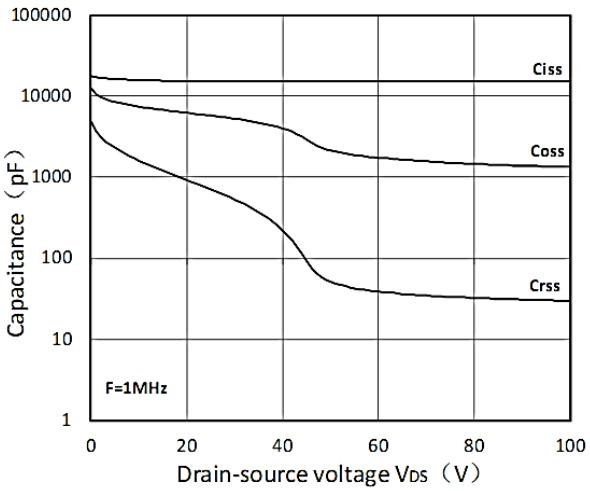



Figure 7. Capacitance Characteristics

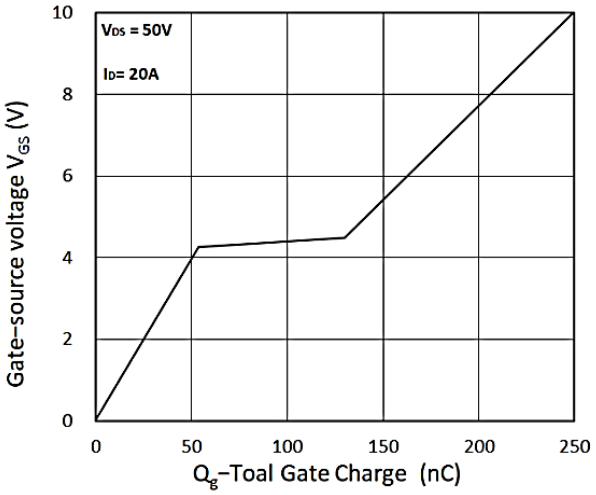



Figure 8. Gate Charge Characteristics

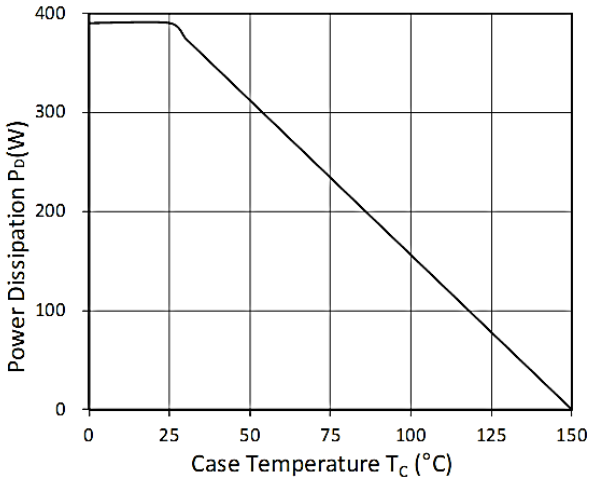



Figure 9. Power Dissipation

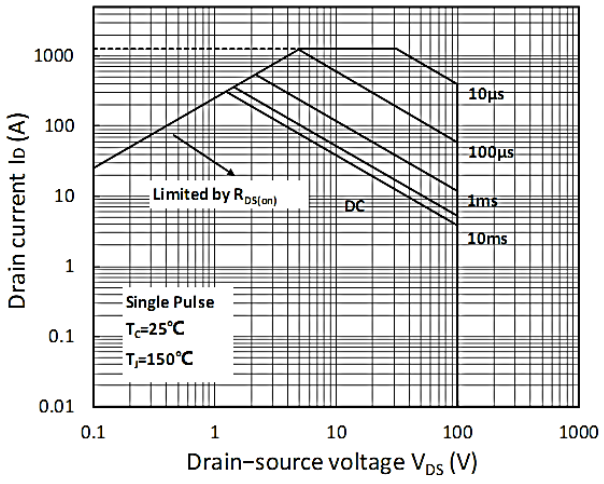



Figure10. Safe Operating Area

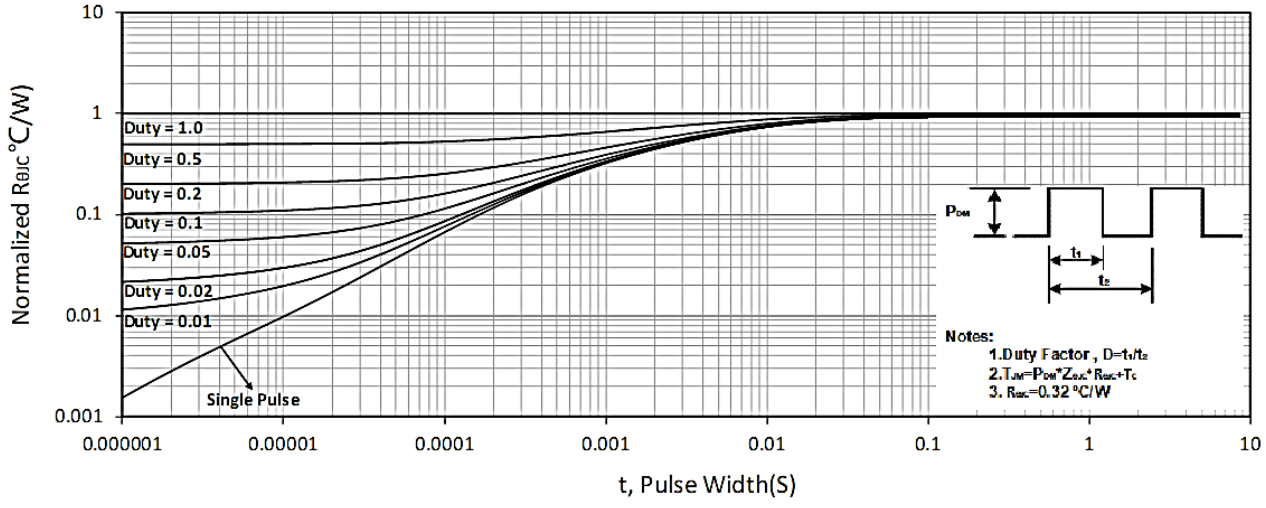
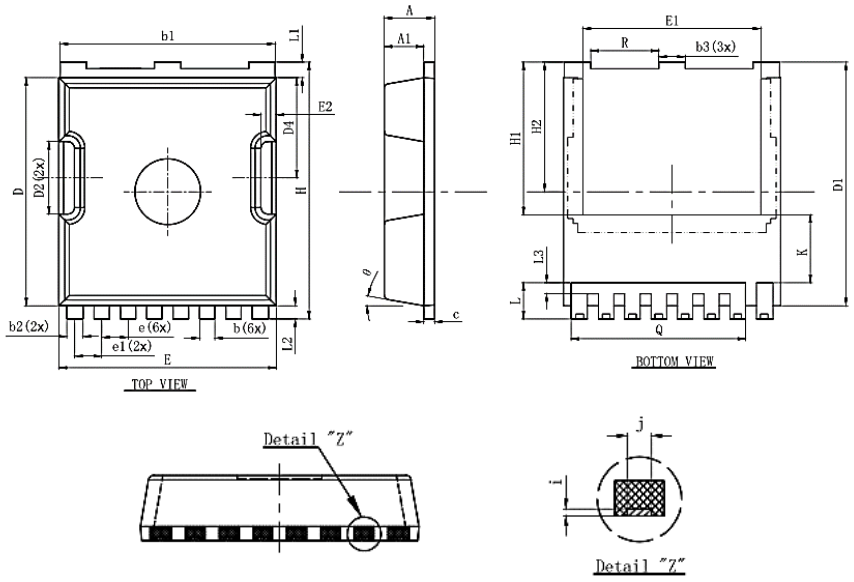



Figure 11. Normalized Maximum Transient Thermal Impedance

## Package Mechanical Data-TOLLA-8-XZ Single




| Symbol | Dimensions In Millimeters | | |
|---|---|---|---|
| | Min. | Nom | Max. |
| A | 2.2 | 2.3 | 2.4 |
| A1 | 1.7 | 1.8 | 1.9 |
| b | 0.6 | 0.7 | 0.8 |
| b1 | 9.7 | 9.8 | 9.9 |
| b2 | 0.65 | 0.75 | 0.85 |
| b3 | 1.1 | 1.2 | 1.3 |
| C | 0.4 | 0.5 | 0.6 |
| D | 10.3 | 10.4 | 10.5 |
| D1 | 11.0 | 11.1 | 11.2 |
| D2 | 3.2 | 3.3 | 3.4 |
| D4 | 4.47 | 4.57 | 4.67 |
| E | 9.8 | 9.9 | 10.0 |
| E1 | 8.0 | 8.1 | 8.2 |
| E2 | 0.5 | 0.6 | 0.7 |
| e | 1.200（BSC） | | |
| e1 | 1.225（BSC） | | |
| H | 11.6 | 11.7 | 11.8 |
| H1 | 6.95BSC | | |
| H2 | 5.9BSC | | |
| i | 0.1REF | | |
| j | 0.350REF | | |
| K | 3.100REF | | |
| L | 1.55 | 1.65 | 1.75 |
| L1 | 0.6 | 0.7 | 0.8 |
| L2 | 0.5 | 0.6 | 0.7 |
| L3 | 0.4 | 0.5 | 0.6 |
| Q | 7.95REF | | |
| R | 3.0 | 3.1 | 3.2 |
| θ | 10°REG | | |

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## 100V N-Channel Enhancement Mode MOSFET

| Edition | Date | Change |
|---|---|---|
| REV1.0 | 2024/5/5 | Initial release |