AP3440ABN182

High-Accurate Step-Down DC-DC Converter with 4.5A MOSFET

1. General Description

The AP3440 is a synchronous rectification PWM control step-down DC-DC converter of the current mode with excellent transient load response characteristics. The recommended operational temperature ranges from −40 to 125ºC. It is capable for automotive use that demands high reliability. The AP3440 supports input voltage from 4.1V to 5.5V and its output voltage is 1.822V. It integrates power MOSFET corresponding to a 4.5A output current at the maximum. The AP3440 is equipped with Output Over-Current Protection, Output Over-Voltage Protection, Under Voltage Lock Out, Thermal Protection, and Power-good function. The AP3440 is housed in a 28-pin QFN0505 package.

2. Features

Input Voltage Range : 4.1V ~ 5.5V
Output Voltage : 1.822V (+1.81%, −1.87%)
Output Current Peak : 4.5A
Oscillation Frequency : 2100 kHz
External Synchronization (supporting Master/Slave mode), Frequency Range : 1800kHz ~ 2250kHz
Integrated Power MOSFET
Soft Start Function
High-Accurate Power-Good Function
Discharging Function of Output Capacitor
Protection Functions: Over Current, Over Voltage, Under Voltage Lock Out and Thermal Protections
Recommended Operational Temperature Range: Ta=−40 ~ 125ºC
Package: 28-pin QFN0505 (Exposed Pad and Pins are Plated)

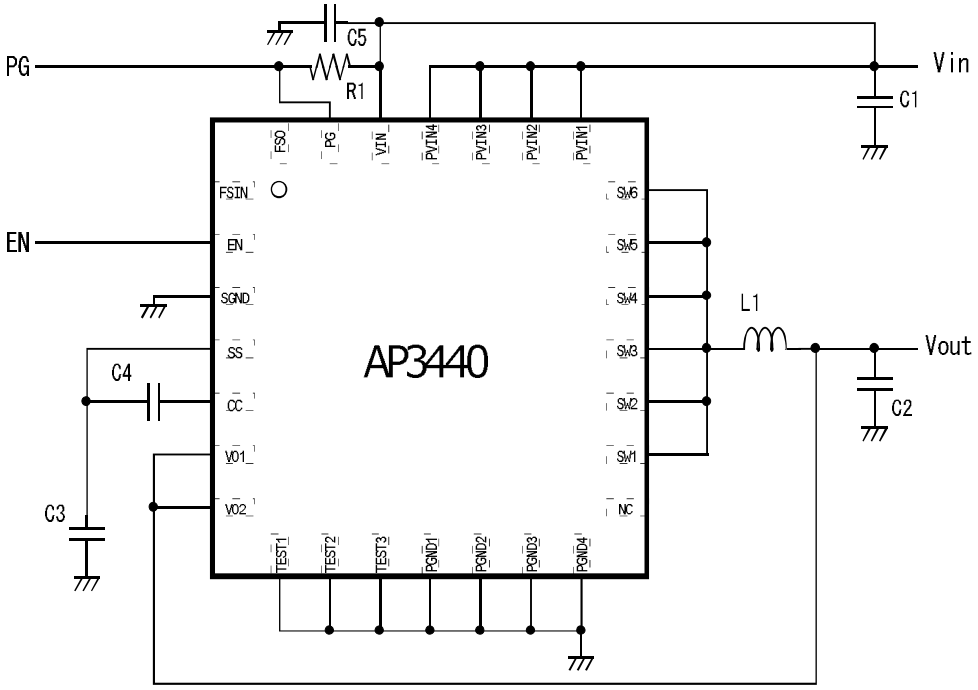

Figure 1. Application

3. Table of Contents

4. Block Diagram

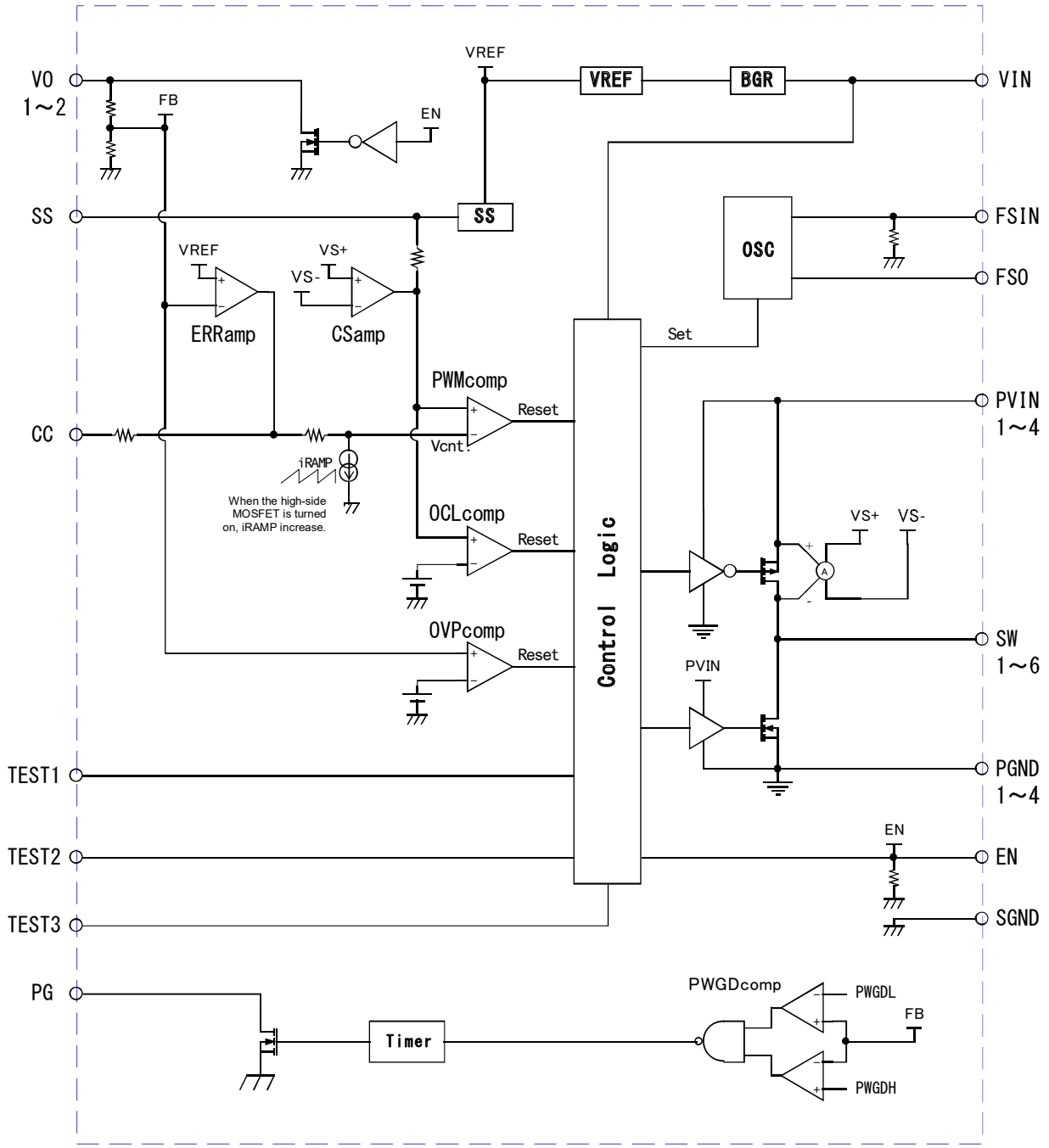

Figure 2. Block Diagram

5. Ordering Guide

Part #	Output Voltage	Operational Temperature Range	Package
AP3440ABN182	1.822V	-40 ~ 125	28-pin QFN(0505) SFS

6. Pin Configurations and Functions

■ Pin Configurations

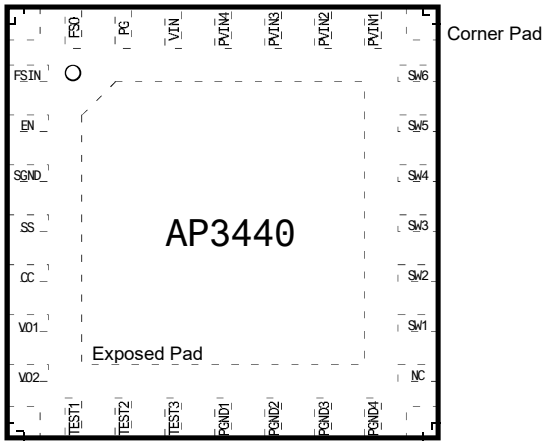

Figure 3. Pin Configurations

■ Functions

No	Pin	I/O	Description
1	FSIN	I	External Synchronous Clock Input Drive frequency is synchronized to the external synchronous clock frequency. This pin should be open or connected to the SGND and PGND pins when not using external synchronous clock.
2	EN	I	Enable Signal Input The AP3440 starts operation by “H” signal input.
3	SGND	—	Signal Ground
4	SS	I/O	Soft Start Pin Connect a capacitor between this pin and the SGND for soft start time adjustment.
5	CC	O	Error Amplifier Output Connect a capacitor and a resistor between this pin and the SS pin for phase compensation of the error amplifier.
6	VO1	I	Output Voltage Feedback Output voltage is adjusted to meet a setting value.
7	VO2	I	
8	TEST1	I	Test Pin Connect to the PGND and SGND pins.
9	TEST2	I	
10	TEST3	I	
11	PGND1	—	Power Ground
12	PGND2	—	
13	PGND3	—	
14	PGND4	—	
15	NC	—	Open Pin
16	SW1	O	Internal MOSFET Switching Output
17	SW2	O	
18	SW3	O	
19	SW4	O	
20	SW5	O	
21	SW6	O	
22	PVIN1	I	Power Supply Input
23	PVIN2	I	
24	PVIN3	I	
25	PVIN4	I	
26	VIN	I	Control Power Input
27	PG	O	Power-Good Signal Output Open drain output of the N-ch MOSFET. This output is off by power-good.
28	FSO	O	External Synchronous Clock Output Internal oscillator or external synchronous clock is inverted and output.
Exposed Pad			Connect to the ground plane of the printed circuit board for heat dissipation.
Corner Pad			Connect to the ground plane of the printed circuit board for the improvement of the solder junction strength.

7. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Voltage between PGND1~4 and VIN, PVIN1~4 or SW1~6	Vterm1	-0.3	+6.0	V
Voltage between SGND and FSIN, EN, SS, CC, TEST1~3, PG, FSO, VO1 or VO2	Vterm2	-0.3	+6.0	V
Voltage between SGND and PGND1~4	Vterm3	-0.3	+0.3	V
Voltage between VIN and PVIN1~4	Vterm4	-0.3	+0.3	V
Storage Ambient Temperature Range	Tstg	-40	150	°C
Junction Temperature	Tj	-40	150	°C
Power Dissipation (Note 1) Ta=25°C	Pd parallel		11.767	W

Note 1. Junction to Ambient Thermal Resistance θ_{JA} = 39.7°C/W
Junction to Case Thermal Resistance θ_{JC} = 0.93°C /W
Parallel Thermal Resistance (θ_{JA}: 25%, θ_{JC}: 75%) $\theta_{(JA+JC)}$ = 10.63°C /W
Ambient temperature of 25°C using JEDEC 4L board. (114.3mm × 76.2mm)

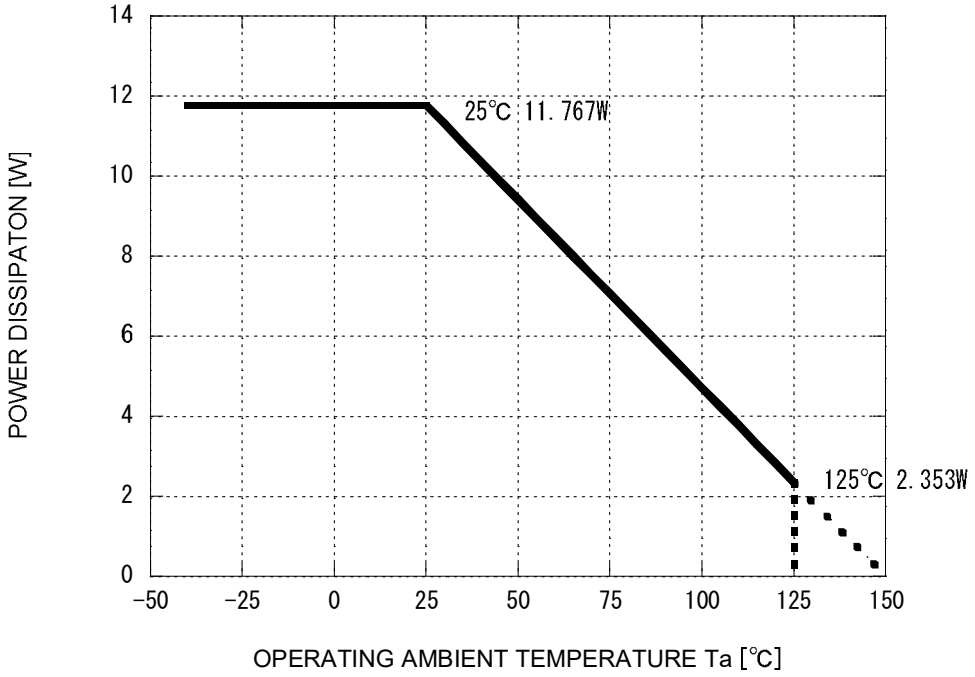

Figure 4. Power Dissipation

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

8. Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input Voltage Range	Vin	4.1	-	5.5	V
Operation Ambient Temperature Range	Ta	-40	-	125	°C
MOSFET Current Capacity on PG Output	I_{MOSON}	-	-	50	mA
External Synchronous Clock Frequency	F_{SYN}	1800	2100	2250	kHz
External Synchronous Clock Frequency ("L" period)	T_{FSYNL}	100	-	384	ns
Continuous Output Current (DC)	I_{DC}	-	-	3.0	A
Output Current Peak Maximum value of 10% duty in every 25ms. 90% Duty: 3A 10% Duty: 4.5A	I_{PEAK}	-	-	4.5	A

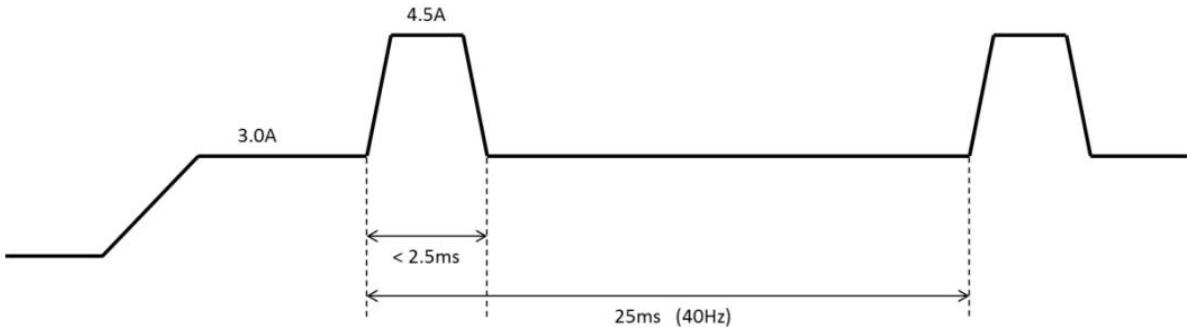

Figure 5. Iout Profile

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

9. Electrical Characteristics

(VIN=5.05V, Tj=-40°C~150°C, unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Output Voltage Accuracy (Note 5)	Vout	1.788	1.822	1.855	V	
VIN Pin Current (in operation)	Isupply	-	-	3	mA	
VIN Shut-down Current	Ishd1	-	-	1	uA	Tj=25°C
PVIN Shut-down Current	Ishd2	-	-	1	uA	Tj=25°C
Over Current Protection Threshold	OCL	5.5	7.85	10.2	A	Coil Peak Current
Over Voltage Protection Threshold	OVP	126	134	142	%	Vout ratio
Oscillation Frequency	Freq	1950	2100	2250	kHz	
Soft Start Charging Current	Iss	24	30	36	uA	
Soft Start Finishing Threshold	Vss	1.11	1.17	1.23	V	
Soft Start Time	Tss	2.1	3.9	6.7	ms	Css=0.1uF
High-side Minimum On-pulse	SWUMINon	-	-	85	ns	
Low-side Minimum On-pulse	SWLMINon	-	-	132	ns	
High-side On-resistance of Internal Switching MOSFET	$R_{DSON}H$	-	91	139		Include Cu wire resistor
Low-side On-resistance of Internal Switching MOSFET	$R_{DSON}L$	-	41	69		Include Cu wire resistor
Under Voltage Lock Out Threshold(UVLO)	V_D	3.8	3.95	4.1	V	
Output Voltage Monitoring Threshold (H) (Note 5)	PWGDH	1.873	1.905	1.936	V	
Output Voltage Monitoring Threshold (L) (Note 5)	PWGDL	1.734	1.763	1.792	V	
PG_BAD Detection Time	T_{RESET1}	1	-	4.7	us	
PG_GOOD Detection Time	T_{RESET2}	8	10	12	ms	
PG Output MOSFET On-resistance	R_{MOSON}	-	-	50		Drain Current =20mA
EN Pin Pull-down Resistance	R_{EN}	60	100	140		
EN Pin Input Voltage “H” (Note 2)	$V_{SHDN}H$	2.0	-	5.5	V	
EN Pin Input Voltage “L” (Note 2)	$V_{SHDN}L$	0	-	0.4	V	
MOSFET On-resistance for EN Off Output Discharge	R_{MOSON}	-	-	200		Discharging Current = 10mA
Line Regulation (Note 3)		-	-	0.685	%/V	Vin=4.7~5.4V
Load Regulation (Note 3)		-	-	0.3	%	Io=0.1~3.5A
Load Transient Response (Note 3) Overshoot	VtranO	-	-	35.3	mV	Io=2↔3.5A Slew rate= 0.2A/us
Undershoot	VtranU	-	-	33.0	mV	
Thermal Protection Threshold (Note 2, Note 4)	Ttsd	155	175	200	°C	
Thermal Protection Hysteresis (Note 2, Note 4)	TSDhys	1	25	50	°C	
FSIN Pin Pull-down Resistance	R_{FSIN}	350	500	650		
FSIN Pin Input Voltage “H” (Note 2)	$V_{SHDN}H$	2.0		5.5	V	
FSIN Pin Input Voltage “L” (Note 2)	$V_{SHDN}L$	0		0.4	V	

Note 2. Guaranteed by design.

Note 3. A reference value with the recommended circuit.

Note 4. This function is to protect the IC from an overheat situation. Functional operation of the device including its reliability is not guaranteed under the condition that the overheat status beyond the specifications continues.

Note 5. There is no overlap between Output Voltage and Output Voltage Monitoring since these values are interlocked by tracking.

10. Timing Chart

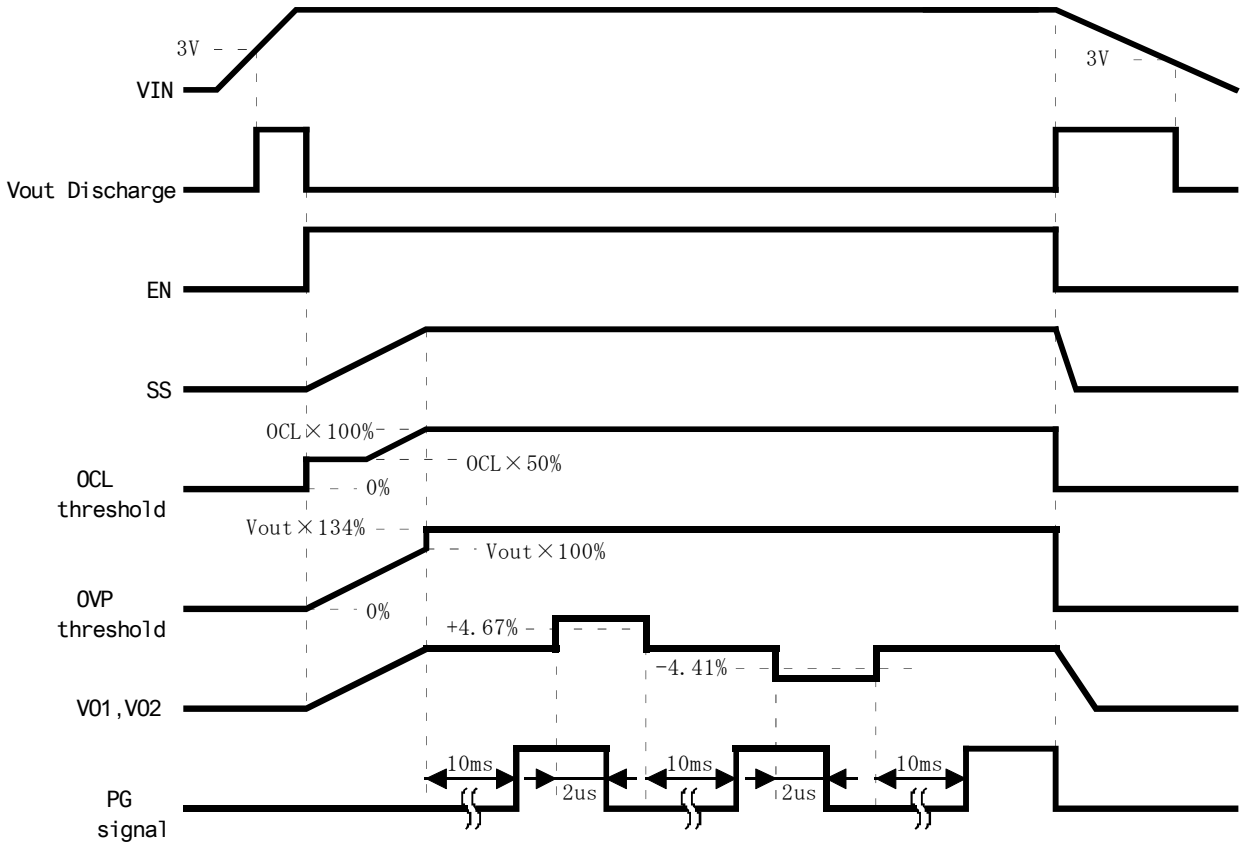

Figure 6. Timing Chart

The AP3440 begin start-up in Soft-Start mode when “H” signal is input to the EN pin while the VIN pin is 4.1V or more. Soft-start operation is controlled by over current and voltage limitations. Each of thresholds change according to the conditions shown below and return to OCL and OVP threshold values at Normal Operation after Soft-Start is completed.

	During Soft-Start	Normal Operation
Over Current Limit (OCL) threshold	SS Pin Voltage < 0.6V: OCL (7.85Atyp) × 1/2	OCL (7.85Atyp)
	SS Pin Voltage ≥ 0.6V: OCL (7.85Atyp) × SS voltage/1.2V	
Over Voltage Protection(OVP) threshold	SS Pin Voltage**:** Vout/1.2V	OVP (Vout×134%typ)

An open drain Nch-MOSFET of the PG pin(hereinafter called as PG_MOS) is turned off when 10ms is passed after V_{OUT} became a level within power-good range following soft-start completion. The PG_MOS is turned on if V_{OUT} is out of the power-good range for more than 2us continuously. PG_MOS is turned off in 10ms after V_{OUT} is returned into power-good range again.

11. Functional Descriptions

11.1 Normal Operation

The AP3440 operates by PWM control in current mode. It integrates feedback resistances and the output voltage is 1.822V typ. A potential difference of the feedback output voltage of the VO1/2 pin and internal reference voltage is amplified by the error amplifier to set a target value of the coil current. An internal current sense circuit detects the coil current. Synchronous rectification is executed as the internal high-side P-channel MOSFET is turned off and low-side N-channel MOSFET is turned on when the coil current reaches a target value after internal high-side P-channel MOSFET is turned on.

11.2 External Synchronous Function

The AP3440 synchronizes the driving frequency to a falling edge (“H” → “L”) of input clock to the FSIN pin. Frequency of the input clock must be in a range from 1800kHz to 2250kHz and the “L” period should be in a range from 100ns to 384ns. When using an internal oscillation frequency, the FSIN pin should be open or connected to the SGND and PGND pins. Note that switching operation is stopped if the FSIN pin is fixed to “H” level since a falling edge of the internal clock is not generated.

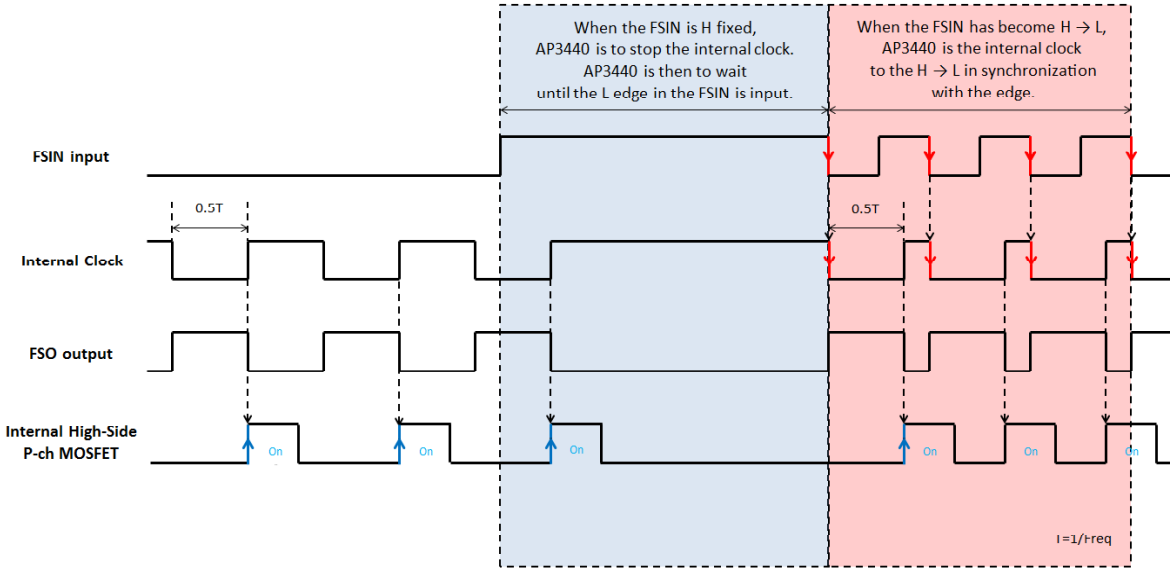

Figure 7. External Synchronous Timing Chart

11.3 Extrenal Synchronous Clock Output

An inverted clock of the driving frequency generated internally is output from the FSO pin. The AP3440 outputs an inverted clock of the external synchronous clock when inputting an external synchronous clock.

11.4 Power Good Function

The AP3440 has a power good function that indicates the output voltage status by the PG pin. The PG pin must be pulled up by a resistor connected to the VIN pin since the PG pin is an open drain output of N-channel MOSFET (hereinafter PG_MOS). The PG-MOS is turned off when the output voltage is in a range of PWGDH and PWGDL for 10ms. The PG-MOS is turned on when the output voltage is out of the power-good range for more than 2us continuously. The PG-MOS is always ON during power-off status and soft start operation. Refer to the section “9. Electrical Characteristics” about PWGDH and PWGDL.

11.5 Over Voltage Protection (OVP)

The output voltage Vout is limited so as not to rise drastically from the setting value.

Protections	About on Product Function	
	Condition	Action
OVP (Over Voltage Protection)	Vout ≥ 134% (typ)	High-side P-ch Power MOSFET = OFF Low-side N-ch Power MOSFET = ON

11.6 Under Voltage Lockout (UVLO)

The AP3440 stops operation when the input voltage drops to a level that is out of operational range.

Protections	About on Product Function	
	Condition	Action
UVLO (Under Voltage Lockout)	VIN ≤ 4.1V	DCDC internal circuit is powered off. High-side P-ch Power MOSFET = OFF Low-side N-ch Power MOSFET = OFF

11.7 Over Current Protection (OCL: Over Current Limit)

Current of high-side P-ch power MOSFET is monitored and limited so that the output current does not become too high.

Protections	About on Product Function	
	Condition	Action
OCL (Over Current Limit)	Current of High-side P-ch power MOSFET ≥7.85A	High-side P-ch Power MOSFET = OFF Low-side N-ch Power MOSFET = ON

The AP3440 changes OCL level to 75% when OCL is detected 2 cycles continuously. In case that Vout decreases farther, the AP3440 goes into hiccup mode.

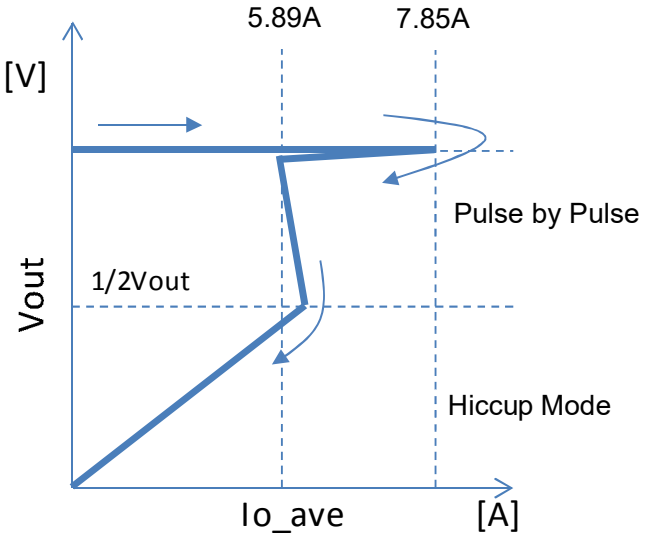

Figure 8. OCL vs Vout

The AP3440 starts hiccup operation that repeats ON and OFF if over current statement is kept for 6 cycles while the output voltage is less than half of the setting value. This counter will be reset if one of the 6 cycles does not meet the over current condition. In the OFF period of hiccup operation, the soft-start capacitor is discharged by 1.5uA to reduce the voltage at the SS pin.

The AP3440 starts soft start operation after grounding the SS pin for 32 cycles of the internal clock when the SS pin voltage drops to 0.52V. Hiccup operation is disabled during soft start.

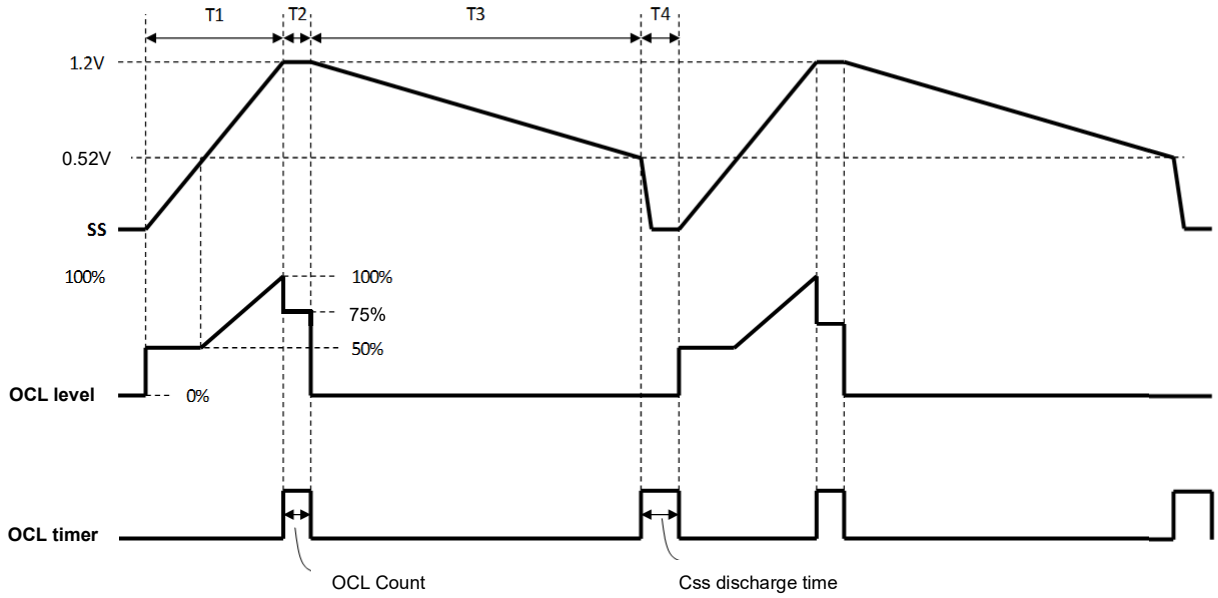

Figure 9. Hiccup Timing Chart

T1: Soft Start Setting Time. Charging current is 30uA.
T2: 6 count time of drive frequency. Hiccup mode detection is executed only in this period.
T3: Discharging Time of Soft Start Capacitor. Discharge current is 1.5uA. This time is equivalent to 12 times as Soft Start Setting Time T1.
T4: Discharging Time of Soft Start Capacitor. (32 cycles of Internal Clock)

11.8 Thermal Protection (TSD: Thermal Shut Down)

The AP3440 stops operation if the chip temperature overs 175°C (typ) for protection.

Protections	About on Product Function	
	Condition	Action
TSD (Thermal Shut down)	Chip Temperature ≥ 175°C (typ)	High-side P-ch Power MOSFET = OFF Low-side N-ch Power MOSFET = OFF DC-DC Circuit Block is OFF.

The AP3440 restarts by soft start when the chip temperature drops.

11.9 Output Capacitor Discharge

The output capacitor is discharged by the N-ch power MOSFET for discharge that are built into the VO terminal (200Ωmax) is turned on , if there is no “H” signal input to the EN pin while the VIN voltage is 3V or more. The N-ch power MOSFET for output discharge(200Ωmax) is turned off by “H” signal input to the EN pin or when the VIN voltage becomes less than 3V.

12. Typical Characteristics

Values in “Iout > 3A” condition are measured in every 25ms with less than 10% duty.

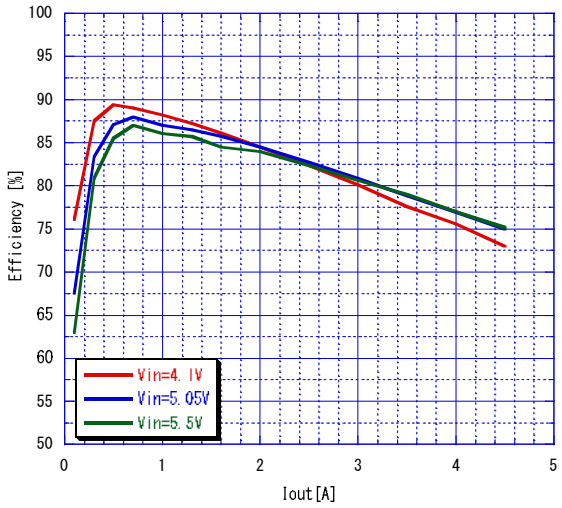

Figure 10. Efficiency

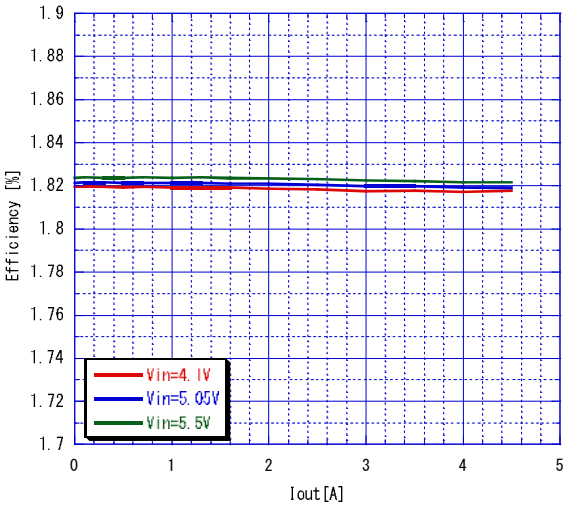

Figure 11. Load Regulation

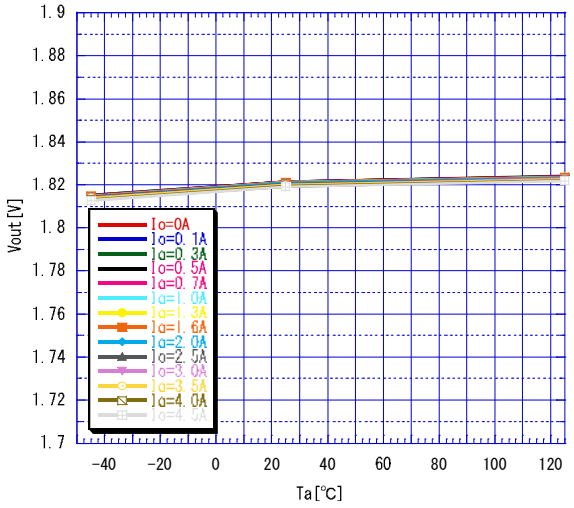

Figure 12. Vout vs Ta

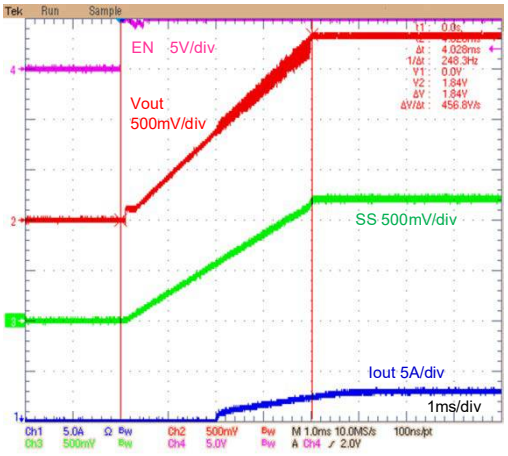

Figure 13. Soft Start

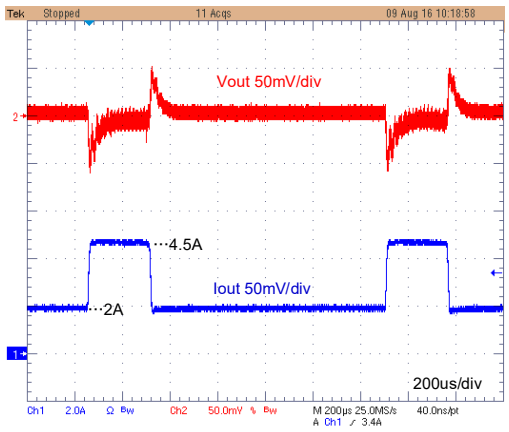

Figure 14. Load Transient

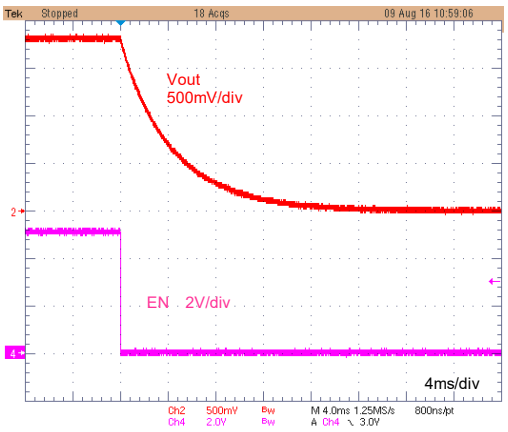

Figure 15. Shut Down

13. Recommended External Circuits

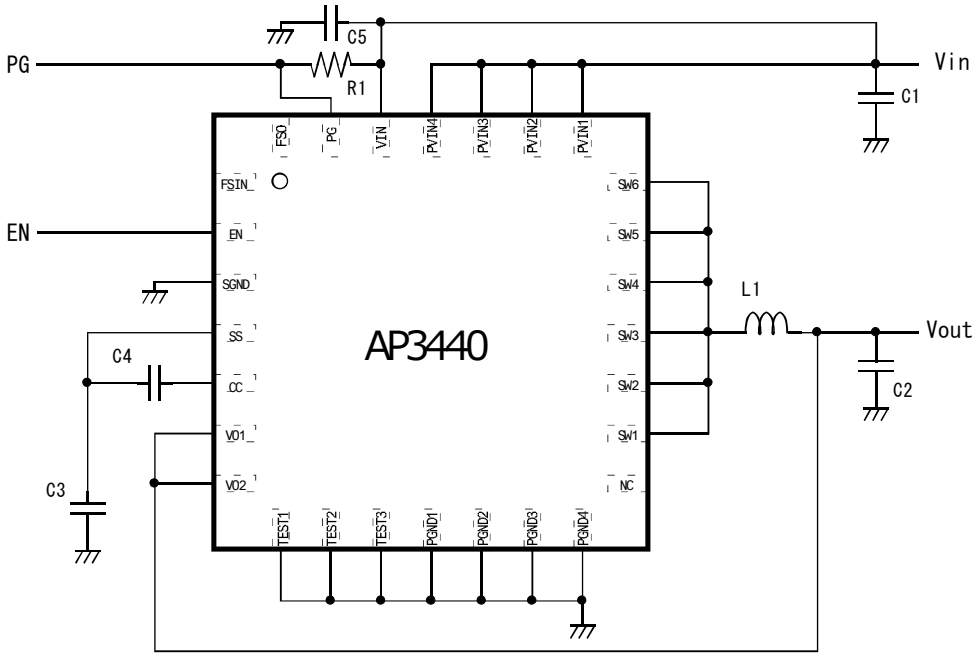

Figure 16. Typical Application

Parameter	Symbol	Effective Value	Nominal Value	Manufacturer
Input Ceramic Capacitor	C1	10uF ±30%	-	-
Output Ceramic Capacitor	C2	50uF ±30%	-	-
Soft Start Capacitor	C3	0.1uF ±30%	-	-
Phase Compensation Capacitor	C4	2.2nF ±30%	-	-
Input Ceramic Capacitor	C5	1uF ±30%		
PWGD Pull-up Resistance	R1	47kΩ ±10%	-	-
Power Inductor	L	-	2.2uH	CLF7045NIT-2R2N-D(TDK)

14. Layout Examples

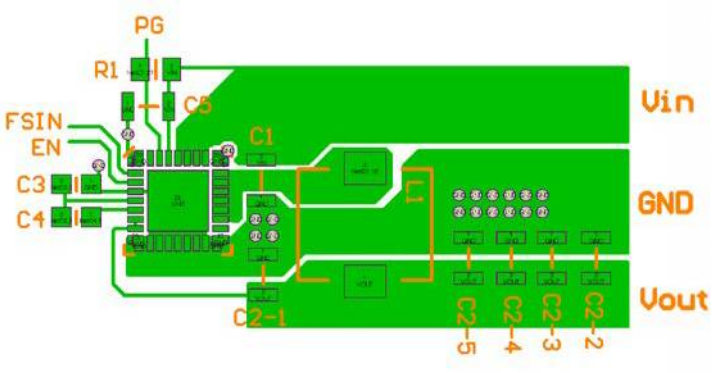

Figure 17. Top Layer

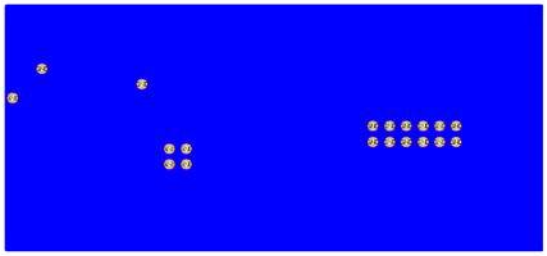

Figure 18. Bottom Layer

■ VIN Capacitor Wiring

A capacitor connected between a VIN pin and the ground should be as close as possible to a VIN pin or a PGND pin.

■ GND Wiring

GND plane should be large as much as possible. The output capacitor and input capacitor should be connected to the same ground plane. The heat dissipation pad on the back surface of the package should be connected to the GND. Each of the PGND1~4 and SGND pins should be connected to the ground directly under the device.

■ Switching Node Connection

Wirings for switching node that are connected to SW pins should be short and thick.

■ Soft Start Capacitor

A VREF capacitor between the SS pin and the ground should be connected as close as possible to the AP3440.

15. Package

■ Outline Dimensions

28-pin QFN0505 (Unit: mm)

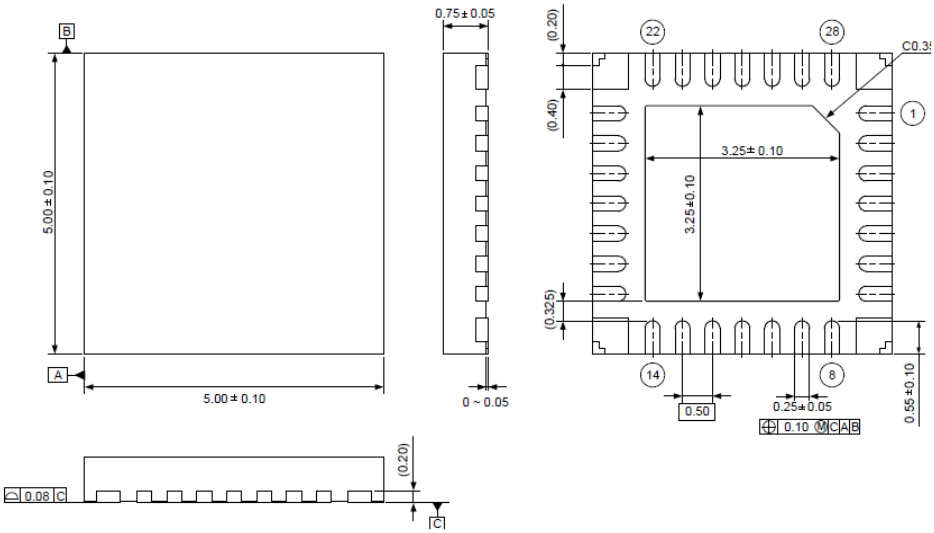

Figure 19. Outline Dimensions

■ Recommended Land

(Unit: mm)

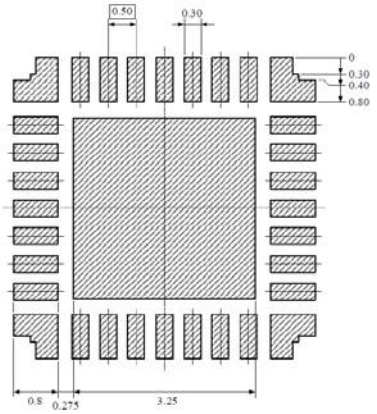

Figure 20.
Recommended Land Pattern

■ Marking

1. Marketing Code : AP3440
2. Output Voltage Code : 182
3. Date Code : XXX Week
   : Y Administration Code

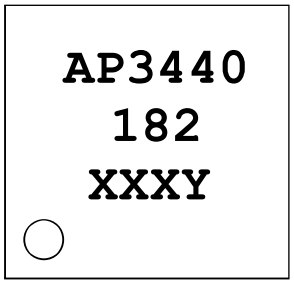

Figure 20. AP3440 Marking

16. Revision History

Date (Y/M/D)	Revision	Page	Contents
17/02/08	00	-	First Edition

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