Dual Phase Synchronous Rectified Buck Controller AP3595

General Description

The AP3595 is a compact dual phase synchronous rectified buck controller specifically designed to deliver high quality output voltage. This device operates at adjustable operation frequency and is capable of delivering up to 60A output current.

This controller integrates internal MOSFET drivers that support 12V+12V bootstrapped voltage for high efficiency power conversion. The bootstrap diode is built-in to simplify the circuit design and minimize external part count.

The AP3595 features configurable gate driving voltage for maximum efficiency and optimal performance. The built-in bootstrap diode simplifies the circuit design and reduces external part count and PCB space. The output voltage is precisely regulated to the reference input that is dynamically adjustable by external voltage divider.

Other features include adjustable soft start, adjustable operation frequency, and quick response to step-load transient. With afore-mentioned functions, the IC provides customers a compact, high efficiency, well-protected and cost-effective solution.

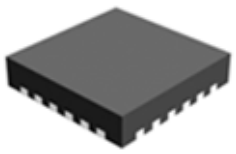
This IC is available in QFN-4×4-24 package.

Features

- Operate with Single Supply Voltage
- Simple Single Loop Voltage Mode Control
- 12V+12V Bootstrapped Drivers with Internal Bootstrap Diode
- Adjustable Over Current Protection by DCR Current Sensing
- Adjustable Current Balancing by $R_{DS(ON)}$ Current Sensing
- Adjustable Operation Frequency from 50kHz to 1MHz Per Phase
- External Compensation
- Dynamic Output Voltage Adjustment
- Adjustable Soft Start
- QFN-4×4-24 Package
- RoHS Compliant and 100% Lead (Pb)-free

Applications

- Middle-High End GPU Core Power
- High End Desktop PC Memory Core Power
- Low Output Voltage, High Power Density DC-DC Converters
- Voltage Regulator Modules



QFN-4×4-24

Figure 1. Package Type of AP3595

Pin Configuration

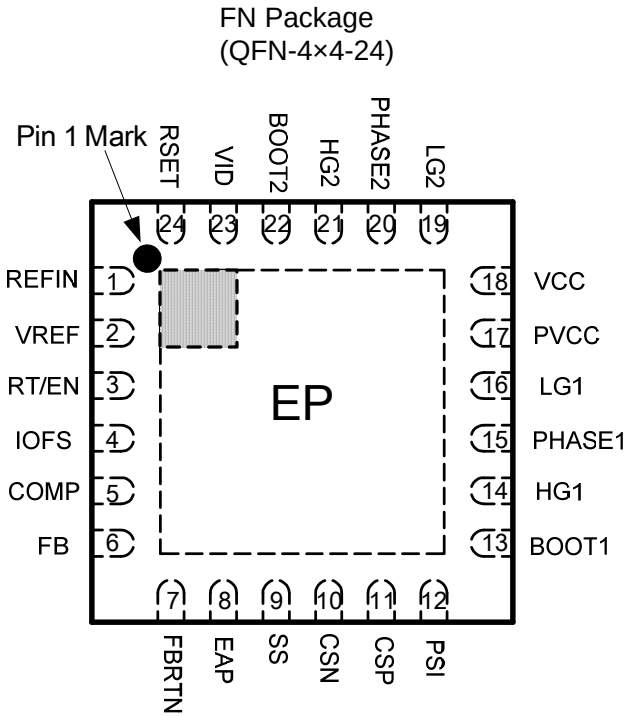


Figure 2. Pin Configuration of AP3595 (Top View)

Pin Description

Pin Number	Pin Name	Function
1	REFIN	External Reference Input. This is the input pin of external reference voltage. Connect a voltage divider from VREF to REFIN and FBRTN to set the reference voltage
2	VREF	Output for Reference Voltage. This is the output pin of high precision 2V reference voltage. Bypass this pin with a 1μF ceramic capacitor to FBRTN
3	RT/EN	Operation Frequency Setting. Connecting a resistor between this pin and GND to set the operation frequency. Pull this pin to ground to shut down the AP3595
4	IOFS	Current Balance Adjustment. Connect a resistor from this pin to VREF or GND to adjust the current sharing
5	COMP	Error Amplifier Output. This is the output of the error amplifier (EA) and the non-inverting input of the PWM comparators. Use this pin in combination with the FB pin to compensate the voltage control feedback loop of the converter
6	FB	Feedback Voltage. This pin is the inverting input to the error amplifier. Use this pin in combination with the COMP pin to compensate the voltage control feedback loop of the converter
7	FBRTN	Feedback Return. Connect this pin to the ground where the output voltage is to be regulated
8	EAP	Non-inverting Input of Error Amplifier. Connect a resistor from this pin to SS pin to set the droop slope
9	SS	Soft Start Output. Connect a capacitor to FBRTN to set the soft start interval
10	CSN	Negative Input for Current Sensing Amplifier
11	CSP	Positive Input for Current Sensing Amplifier
12	PSI	Power Saving Mode. Connect this pin to VREF for always two phase operation. Short this pin to ground for always single phase operation
13	BOOT1	Bootstrap Supply for the Floating Upper Gate Driver of Channel 1. Connect a bootstrap capacitor between BOOT1 pin and the PHASE1 pin to form a bootstrap circuit
14	HG1	Upper Gate Driver Output for Channel 1. Connect this pin to the gate of upper MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off
15	PHASE1	Switch Node for Channel 1. Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin is used as the sink for the Upper GATE driver. It is also monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off
16	LG1	Lower Gate Driver Output for Channel 1. Connect this pin to the gate of lower MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turned off

Pin Description (Continued)

Pin Number	Pin Name	Function
17	PVCC	Supply Voltage for Gate Driver. This pin is the output of internal 9V LDO. This pin provides current for gate drivers. Bypass this pin with a minimum 1μF ceramic capacitor
18	VCC	Supply Voltage. This pin provides current for internal control circuit and 9V LDO. Bypass this pin with a minimum 1μF ceramic capacitor next to the IC
19	LG2	Lower Gate Driver Output for Channel 2. Connect this pin to the gate of lower MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turned off
20	PHASE2	Switch Node for Channel 2. Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin is used as the sink for the HG2 driver. It is also monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off
21	HG2	Upper Gate Driver Output for Channel 2. Connect this pin to the gate of upper MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off
22	BOOT2	Bootstrap Supply for the Floating Upper Gate Driver of Channel 2. Connect a bootstrap capacitor between BOOT2 pin and the PHASE2 pin to form a bootstrap circuit
23	VID	VID Input. This pin is used to adjust the reference voltage. Logic high enables the internal MOSFET connected to RSET pin
24	RSET	Reference Voltage Setting. This pin is an open drain output that is pulled low when VID sets to high. Connect a resistor from this pin to REFIN pin to set the reference voltage
	Exposed Pad GND	Power Ground. Tie this pin to the ground island/plane through the lowest available impedance connection

Dual Phase Synchronous Rectified Buck Controller AP3595

Functional Block Diagram

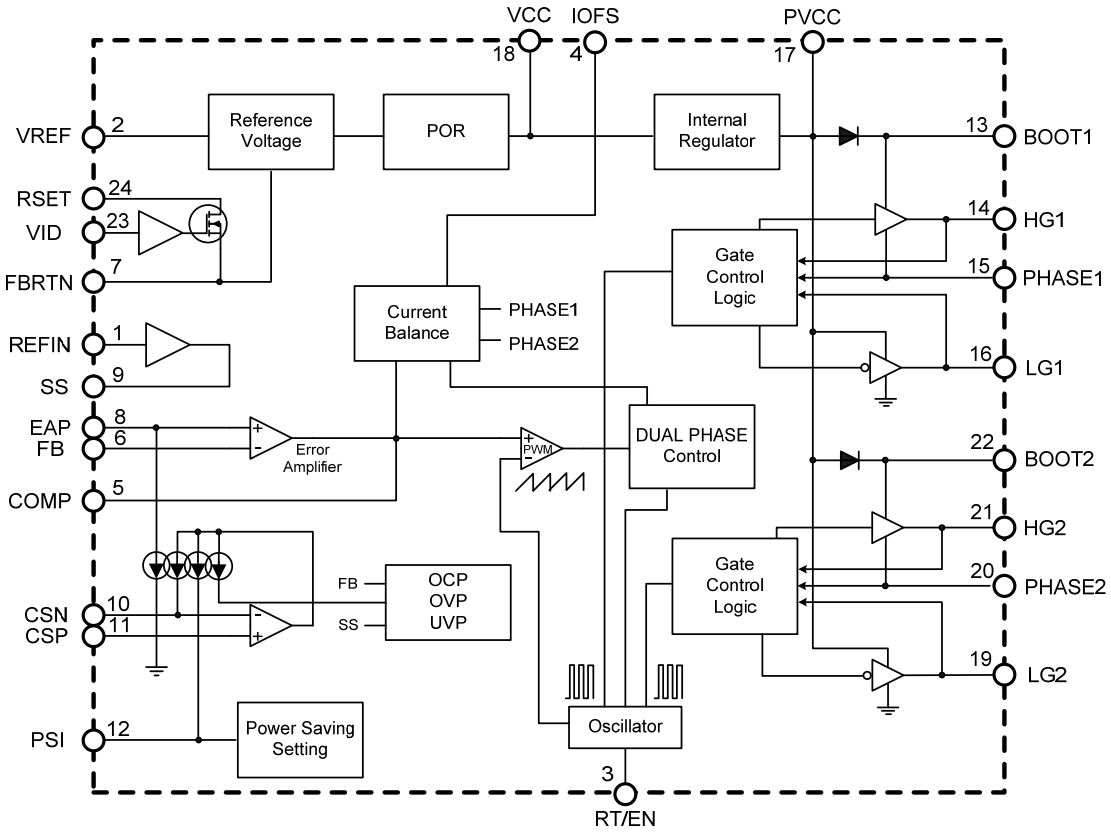
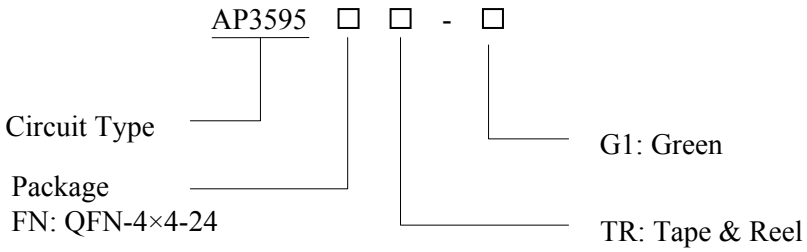


Figure 3. Functional Block Diagram of AP3595

Ordering Information



Package	Temperature Range	Part Number	Marking ID	Packing Type
QFN-4×4-24	-40 to 85°C	AP3595FNTR-G1	B3D	Tape & Reel

BCD Semiconductor's Pb-free products, as designated with "G1" suffix in the part number, are RoHS compliant and green.

Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Value		Unit
Supply Input Voltage	V_{CC}	-0.3 to 15		V
PHASE to GND Voltage	V_{PHASE}	DC	-0.3 to 15	V
		<200nS	-5 to 30	
HG to PHASE Voltage	V_{HG}	DC	-0.3 to $V_{BOOT-PHASE}$+0.3	V
		<200ns	-5 to $V_{BOOT-PHASE}$+5	
LG to GND Voltage	V_{LG}	DC	-0.3 to V_{CC}+0.3	V
		<200ns	-5 to V_{CC}+5	
BOOT to PHASE Voltage		15		V
BOOT to GND Voltage	V_{BOOT}	DC	-0.3 to V_{PHASE}+15	V
		<200nS	-0.3 to 42	
Input, Output or I/O Voltage		-0.3 to 6		V
Power Dissipation	P_D	2.5		W
Thermal Resistance (Junction to Ambient)	θ_{JA}	40		ºC/W
Storage Temperature Range	T_{STG}	-65 to 150		ºC
Junction Temperature	T_J	150		ºC
Lead Temperature (Soldering, 10sec)	T_{LEAD}	260		ºC
ESD (Human Body Model)	V_{HBM}	2000		V
ESD (Machine Model)	V_{MM}	200		V

Note 1: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to “Absolute Maximum Ratings” for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply Input Voltage	V_{CC}	10.8	13.2	V
Operating Ambient Temperature	T_A	-40	85	ºC
Operating Junction Temperature	T_J	-40	125	ºC

Electrical Characteristics

V_{CC}=12V, T_A=25ºC, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SUPPLY INPUT						
Supply Input Voltage	V_{CC}		10.8		13.2	V
Supply Current	I_{CC}	HG and LG Open, V_{CC}=12V, Switching		5		mA
Quiescent Current	I_Q	No Switching, I_{PCC}=0mA		4		mA
Regulated Supply Voltage	V_{PCC}	RT/EN=0V, I_{PCC}=0mA	8	9	10	V
POR Threshold	V_{RTH}		8	9	10	V
POR Hysteresis	V_{HYS}			1		V
CHIP ENABLE/FREQUENCY SETTING						
RT/EN Sourcing Current	$I_{RT/EN}$	$V_{RT/EN}$=GND	100	150	200	μA
RT/EN Voltage	$V_{RT/EN}$	R_{RT}=33kΩ		1		V
Switching Frequency Setting Range			50		1000	kHz
Free Run Switching Frequency	f_{OSC}	R_{RT}=33kΩ	270	300	330	kHz
Switching Frequency Accuracy	$\triangle f_{OSC}$	f_{OSC}=200kHz to 500kHz	-15		15	%
OSCILLATOR						
Maximum Duty Cycle				40		%
Minimum Duty Cycle				0		%
Ramp Amplitude	V_{OSC}	V_{CC}=12V		3.5		V
POWER SAVING MODE						
Threshold Voltage for Entering Dual Phase	V_{PSI_H}	V_{PSI} rising	1.2			V
Threshold Voltage for Entering Single Phase	V_{PSI_L}	V_{PSI} falling			0.4	V
REFERENCE VOLTAGE						
Reference Voltage Accuracy	V_{REF}	I_{REF}=100μA	1.98	2.0	2.02	V
Reference Voltage Load Regulation	$\triangle V_{REF}$	I_{REF}=0 to 2mA	-5		5	mV
Output Voltage Accuracy	$\triangle V_{FB}$	$\lvert V_{REFIN}-V_{FB}\rvert$, V_{CC}=12V, No Load, R_{DRP}=0, V_{REFIN}=0.8V to 1.6V			5	mV
ERROR AMPLIFIER						
Open Loop DC Gain	A_O	Guaranteed by design	70	80		dB
Gain Bandwidth Product	G_{BW}	C_{LOAD}=5pF, Guaranteed by design		20		MHz
Slew Rate	SR	Guaranteed by design	15	20		V/μs
Maximum Current (Sink and Source)	I_{COMP}	V_{COMP}=1.6V	1.5	2.0		mA

Electrical Characteristics (Continued)

V_{CC}=12V, T_A=25ºC, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SOFT START						
Soft Start Current	I_{SS}	During soft start		22		μA
Supply Current	I_{SS_CC}	After soft start end		200		μA
TOTAL CURRENT SENSE						
Maximum Sourcing Current	I_{CSN_MAX}		100			μA
GM Amplifier Offset Voltage			-5	0	5	mV
Over Current Protection Threshold	I_{CSN_OCP}			60		μA
Droop Accuracy	I_{DRP}/I_{CSN}		90	100	110	%
PSI Accuracy	I_{PSI}/I_{CSN}		90	100	110	%
PHASE CURRENT SENSE						
Trans-conductance				1.0		mS
IOFS Voltage	V_{OFS}	100kΩ from IOFS to VREF		1.5		V
		100kΩ from IOFS to GND		0.5		
VID CONTROL INPUT						
Logic High Threshold Level	V_{IH}		1.2			V
Logic Low Threshold Level	V_{IL}				0.4	V
On Resistance of RSET MOSFET	R_{RSET}	V_{ID}=High		20		Ω
Leakage Current of RSET Pin	I_{RSET}	V_{RSET}=2V, V_{ID}=0V			0.1	μA
GATE DRIVER						
Upper Gate Sourcing Current	I_{HG_SRC}	V_{BOOT}-V_{PHASE}=6V		1.2		A
Upper Gate Sinking Resistance	R_{HG_SNK}	I_{HG}=100mA sinking		1.5	3	Ω
Lower Gate Sourcing Current	I_{LG_SRC}	V_{PCC}-V_{LG}=6V		1.2		A
Lower Gate Sinking Resistance	R_{LG_SNK}	I_{LG}=100mA sinking		1	2	Ω
Dead Time	t_{DT}			50		ns
PROTECTION						
Over Voltage Protection	V_{FB}-V_{SS}			300		mV
Under Voltage Protection	V_{FB}-V_{SS}			-300		mV
Over Temperature Protection				150		°C
Over Temperature Hysteresis				20		°C

Typical Performance Characteristics

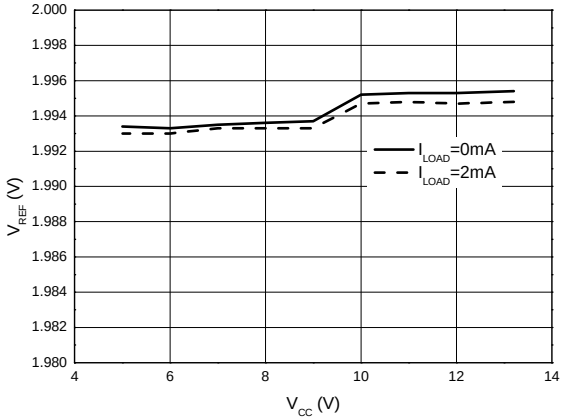


Figure 4. V_{REF} Line Regulation

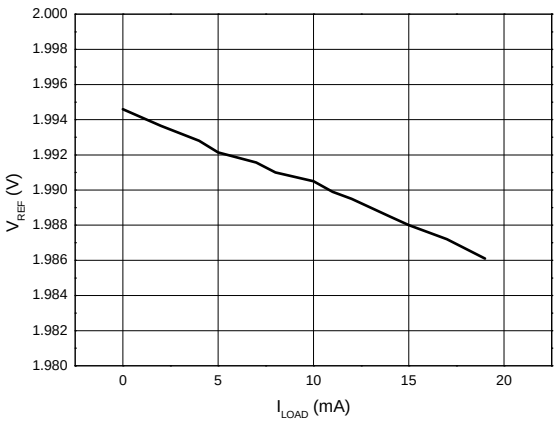


Figure 5. V_{REF} Load Regulation

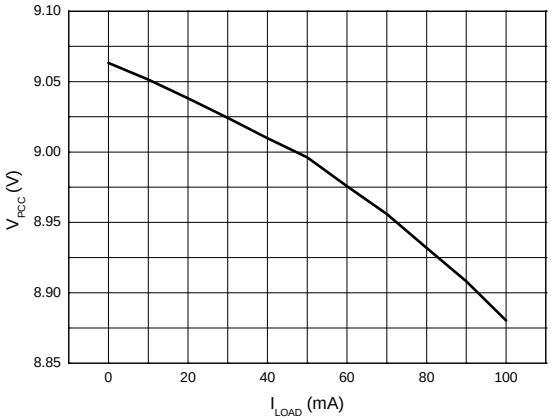


Figure 6. V_{PCC} Load Regulation

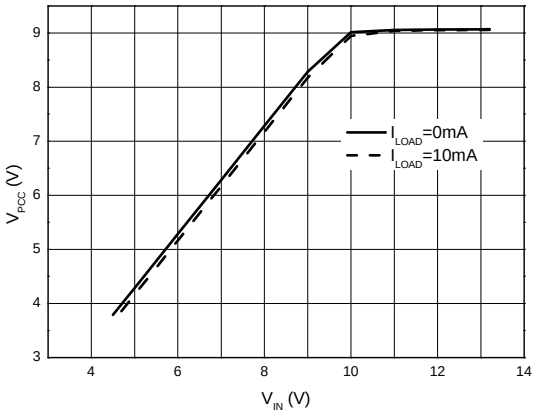


Figure 7. V_{PCC} Line Regulation

Typical Performance Characteristics (Continued)

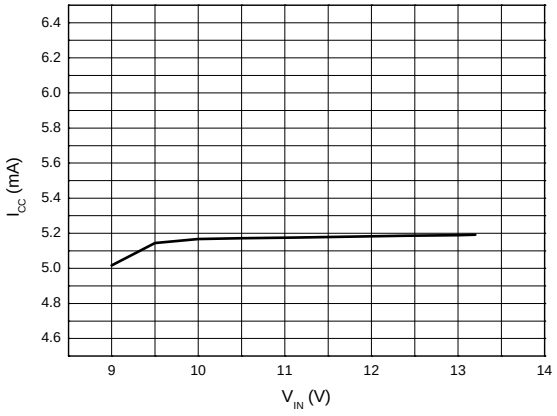


Figure 8. I_{CC} vs. V_{IN}

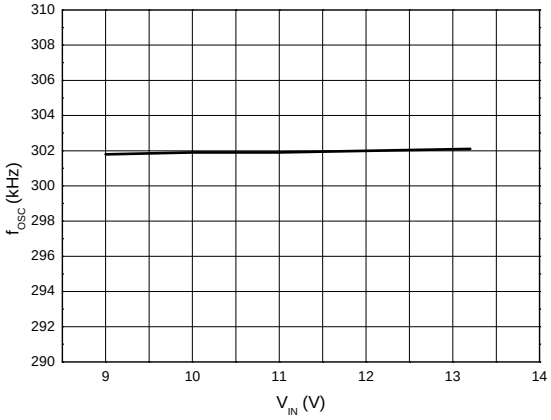


Figure 9. f_{OSC} vs. V_{IN}

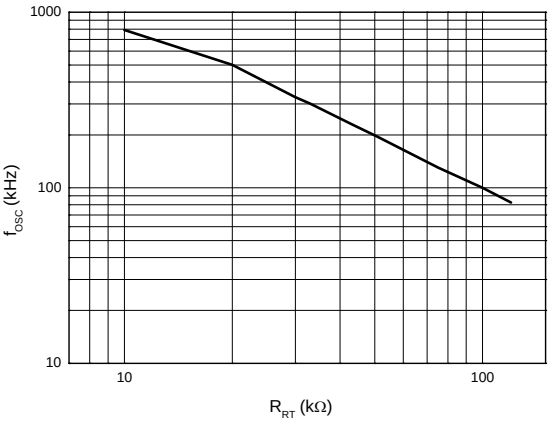


Figure 10. f_{OSC} vs. R_{RT}

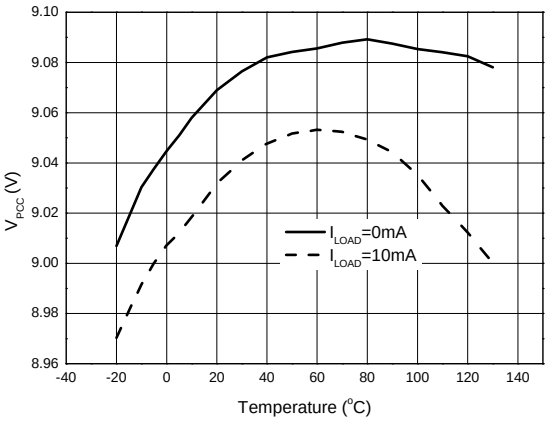


Figure 11. V_{PCC} vs. Temperature

Typical Performance Characteristics (Continued)

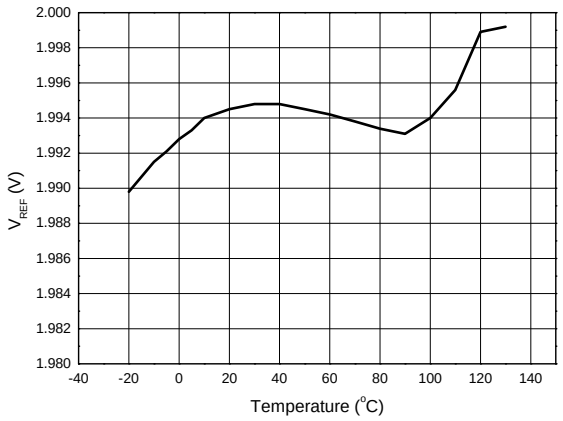


Figure 12. V_{REF} vs. Temperature

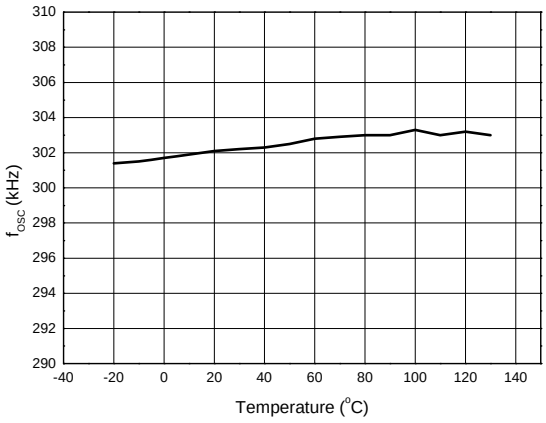
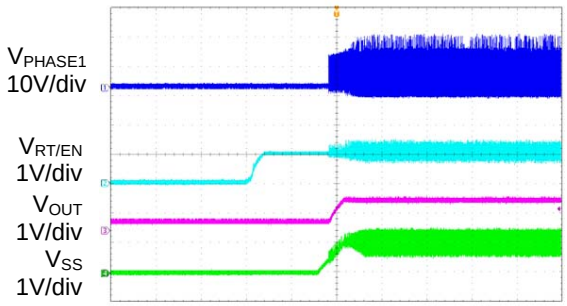
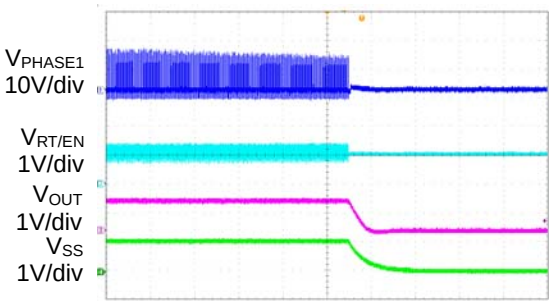


Figure 13. f_{OSC} vs. Temperature



Time 4ms/div

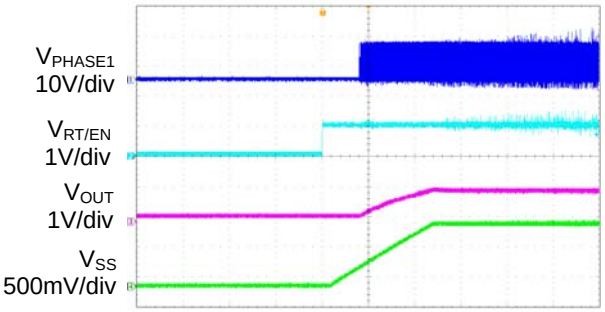
Figure 14. Power On Waveforms



Time 200μs/div

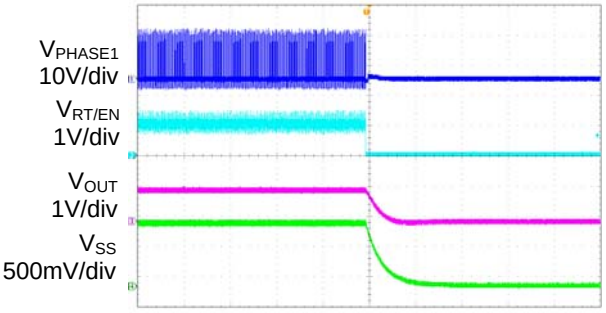
Figure 15. Power Off Waveforms

Typical Performance Characteristics (Continued)



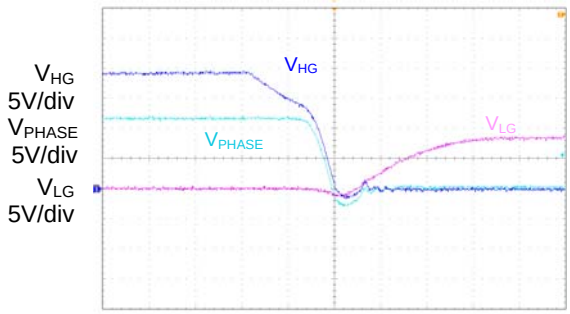
Time 1ms/div

Figure 16. EN On Waveform



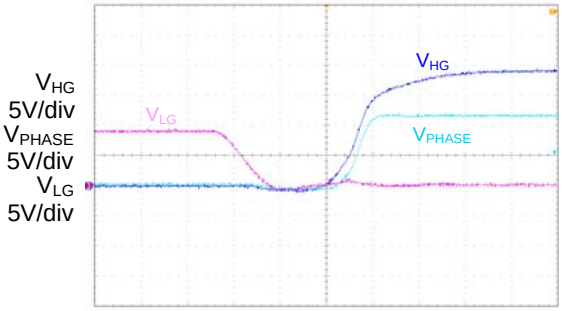
Time 200µs/div

Figure 17. EN Off Waveform



Time 40ns/div

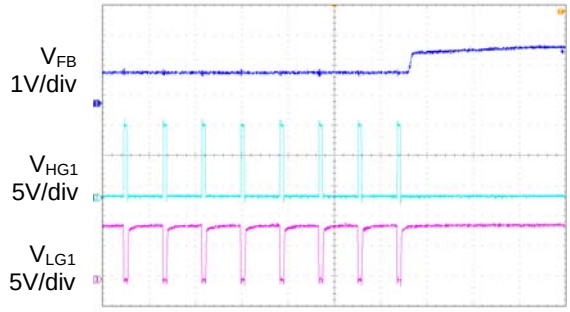
Figure 18. Dead Time 1



Time 40ns/div

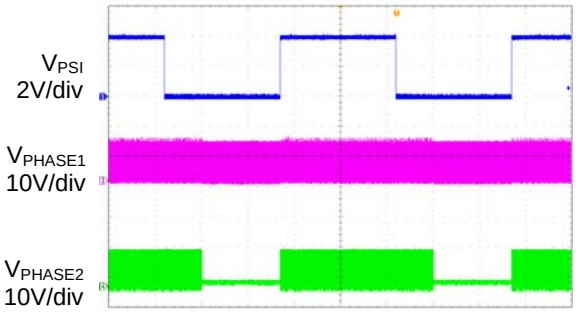
Figure 19. Dead Time 2

Typical Performance Characteristics (Continued)



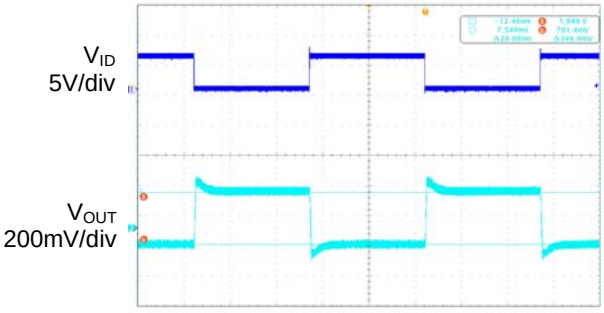
Time 4μs/div

Figure 20. OVP Function



Time 2ms/div

Figure 21. PSI Function



Time 2ms/div

Figure 22. VID Change

Typical Application

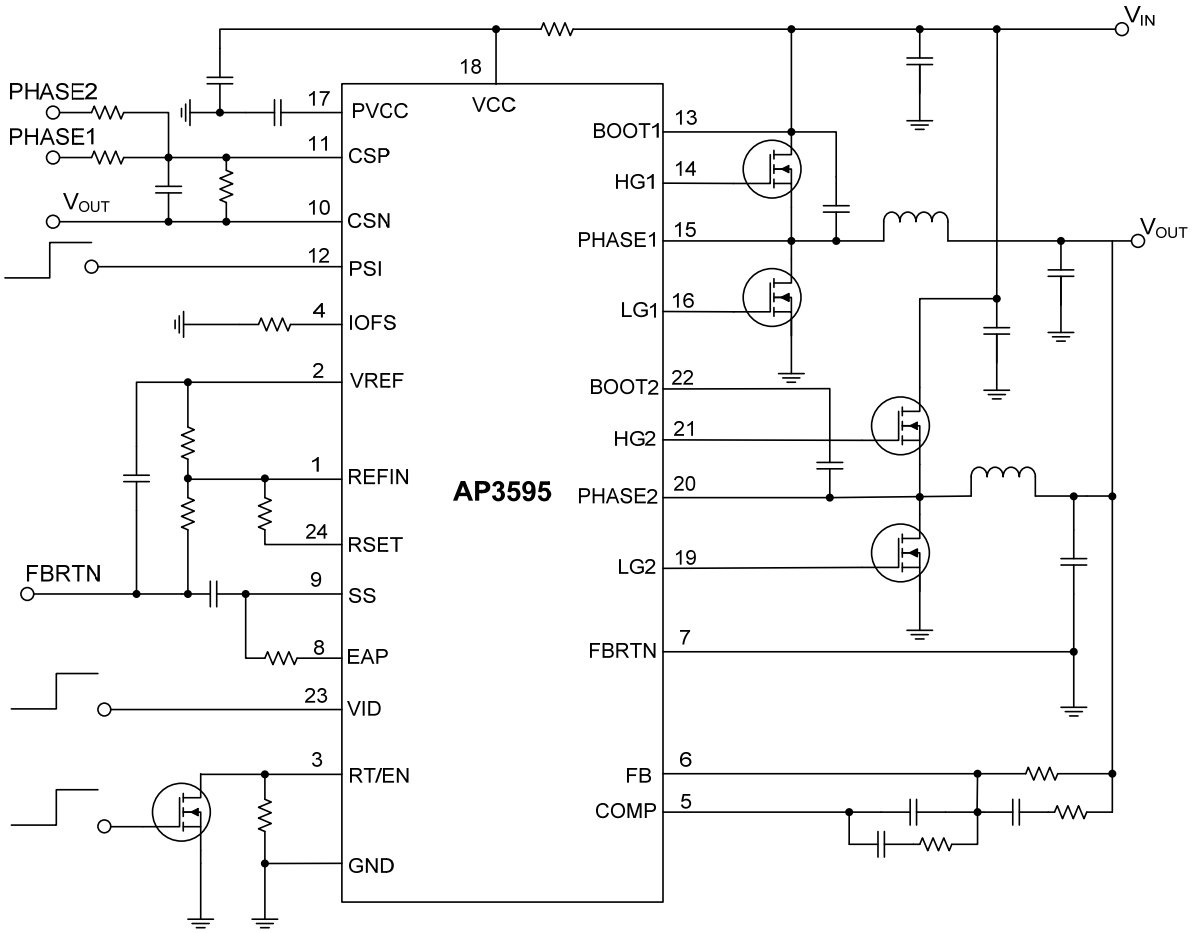


Figure 23. Typical Application of AP3595

Application Information

1. Overview

AP3595 is a dual-phase synchronous-rectified buck controller designed to deliver high quality output voltage for high power applications. It is capable of delivering up to 60A output current with embedded bootstrapped drivers that support 12V+12V driver capability. The built-in bootstrap diode simplifies the circuit design and reduces external part count and PCB space.

The output voltage is precisely regulated to the reference input that is dynamically adjustable by external voltage divider. The adjustable current balance is achieved by $R_{DS(ON)}$ current sensing technique.

AP3595 features comprehensive protection functions including over current protection, input/output under voltage protection, over voltage protection and over temperature protection.

Other features include adjustable soft start, adjustable operation frequency, and quick response to step load transient. With aforementioned functions, the IC provides customer a compact, high efficiency, well-protected and cost effective solution.

2. Power on Reset

A Power On Reset (POR) circuitry continuously monitors the supply voltage at VCC. Once the rising POR threshold is exceeded, the AP3595 sets itself to active state and is ready to accept chip enable command. The rising POR threshold is typically 9V.

3. Soft Start

The AP3595 initiates its soft start cycle when the RT/EN pin is released from ground once the POR is granted as shown in Figure 24.

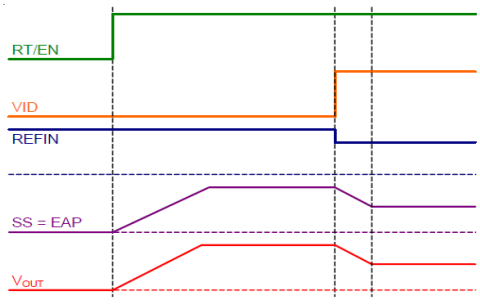


Figure 24. Soft Start Cycle (R_{DRP}=0)

As mentioned in the above section, the slew rate of voltage transition at SS pin and V_{OUT} during soft start and V_{REFIN} jumping is controlled by the capacitor connected to the SS pin. This reduces inrush current to charge/discharge the large output capacitors during soft start and VID changing, and prevents OCP, OVP/UVP false trigger. The SS buffer sinking/sourcing capability is limited to 22μA during soft start and 200μA after soft start end. Therefore, the slew rate of voltage ramping up/down at SS, EAP and FB pin during soft start or VID changing is calculated as:

$$\frac{dV_{SS}}{dt}=\frac{dV_{EAP}}{dt}=\frac{dV_{FB}}{dt}=\frac{22\mu A}{C_{SS}}$$ During Soft Start

$$\frac{dV_{SS}}{dt}=\frac{dV_{EAP}}{dt}=\frac{dV_{FB}}{dt}=\frac{200\mu A}{C_{SS}}$$ After Soft Start

4. Pre-Bias Function

AP3595 features pre-bias start-up capability. If the output voltage is pre-biased with a voltage V_{BIAS}, that accordingly makes V_{FB} higher than reference voltage ramping V_{EAP}. The error amplifier keeps V_{COMP} lower than the valley of the sawtooth waveform and makes PWM comparators output low until the ramping V_{EAP} catches up the feedback voltage. The IC keeps both upper and lower MOSFETs off until the first pulse takes place.

5. Chip Oscillator Frequency Programming

A resistor R_{FS} connected to RT/EN pin programs the oscillator frequency as:

$$f_{OSC}=\frac{10000}{R_{FS}(k\Omega)}(kHz)$$

Figure 25 shows the relationship between oscillation frequency and R_{FS}.

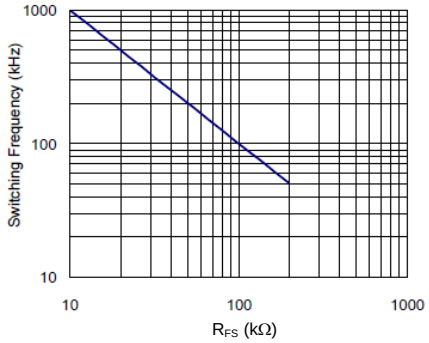


Figure 25. Switching Frequency vs. R_{FS}

Application Information (Continued)

When released, the RT/EN pin voltage is regulated at 1V. Pulling the RT/EN pin to ground shuts down the IC.

6. Current Balance

AP3595 extracts phase currents for current balance by parasitic on-resistance of the lower switches when turned on as shown in Figure 26.

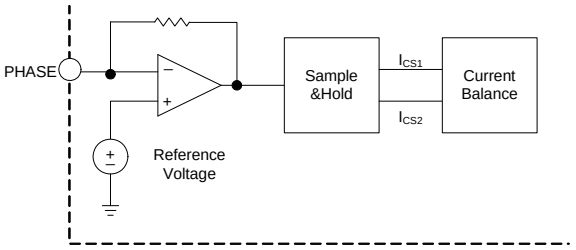


Figure 26. $R_{DS(ON)}$ Current Sensing Scheme

The GM amplifier senses the voltage drop across the lower switch and converts it into current signal when it turns on. The sampled and held current is expressed as:

$$I_{CSX} = I_{LX} \times R_{DS(ON)} \times 10^{-3} + 12\mu A$$

Where I_{LX} is the phase x current in Ampere, $R_{DS(ON)}$ is the on-resistance of low side MOSFET, 12μA is a constant current to compensate the offset voltage of the current sensing circuit.

AP3595 tunes the duty cycle of each channel for current balance according to the sensed inductor current signals as shown in Figure 27. If the current of channel 1 is smaller than the current of channel 2, the IC increases the duty cycle of the corresponding phase to increase its phase current accordingly, vice versa.

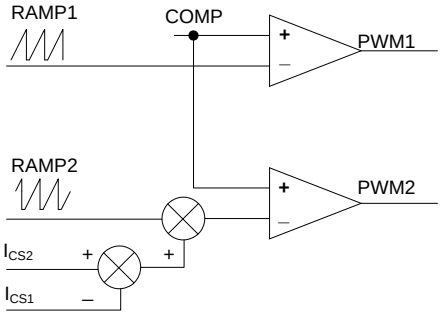


Figure 27. Current Balance Scheme of AP3595

7. Power Saving Interface (PSI)

The AP3595 supports dual phase or single phase which is controlled by V_{PSI}. If V_{PSI}>1.2V, AP3595 will operate in dual phase mode. If V_{PSI}<0.4V, AP3595 will operate in single phase mode. There is 2ms delay at the transient from dual phase to single phase, and no delay time from single phase to dual phase.

8. Current Sense by DCR

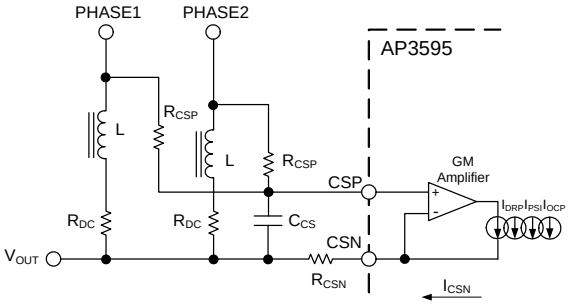


Figure 28. Output Current Sensing Block

The above figure shows the output current sensing block of AP3595. The voltage V_{CS} across the current sensing capacitor C_{CS} can be expressed as

$$V_{CS} = I_{OUT} \times R_{DC} / 2,$$

if the following condition is true:

$$2 \times L / R_{DC} = R_{CSP} \times C_{CS}$$

Where L is the output inductor of the buck converter, R_{DC} is the parasitic resistance of the inductor, R_{CSP} and C_{CS} are the external RC network for current sensing.

The GM amplifier will source a current I_{CSN} to the CSN pin to let its inputs virtually short circuit.

$$I_{CSN} \times R_{CSN} = V_{CS}$$

Therefore the output current signal I_{CSN} can be expressed as:

$$I_{CSN} = \frac{I_{OUT} \times R_{DC}}{2 \times R_{CSN}}$$

The output current signal I_{CSN} is used to droop tuning and output over current protection.

9. Short Circuit Protection (SCP)

The AP3595 has over current protection (OCP) and output under voltage protection (UVP) functions.

Application Information (Continued)

9.1 OCP Function

The sensed current signals are monitored for over current protection. If I_{CSN} is higher than 60μA, the over current protection OCP is activated. Take the above case for example, the OCP level is calculated as:

$$I_{OCP} = \frac{2 \times 60\mu A \times 2k\Omega}{2m\Omega} = 120A$$

The OCP is of latch-off type and can be reset by toggling RT/EN or VCC POR.

9.2 UVP Function

The output feedback voltage V_{FB} is also monitored for under voltage protection after soft start. The UV threshold is set as V_{FB}-V_{SS}<-0.3V. The under voltage protection has 30μs triggered delay. When UVP is triggered, both high side and low side are shutdown immediately.

OCP and UVP are latched functions. the IC can power off, and then power on or use RT/EN reset to restart again.

10. Over Voltage Protection (OVP)

The output voltage V_{FB} is continuously monitored for over voltage protection. When it is 300mV higher than setting, the OVP function is triggered. The over voltage protection has 30μs triggered delay. When OVP is triggered, the LGATE will go high and the HGATE will go low to discharge the output capacitor.

11. Droop Setting

In some high current applications, a requirement on precisely controlled output impedance is imposed. This dependence of output voltage on load current is often termed droop regulation. The droop control block generates a voltage through external resistor R_{DRP} (Which is between SS and EAP) and then sets the droop voltage. The droop voltage, V_{DRP}, is proportional to the total current in two channels (For more information about the I_{CSN} and I_{DRP}, please refer to the current sense section). As shown in the following equation:

$$V_{FB} = V_{SS} - I_{DRP} \times R_{DRP}$$

Where I_{DRP} is the droop current which is mirrored from I_{CSN}. The output voltage also can be described as:

$$V_{FB} = V_{SS} - I_{DRP} \times R_{DRP} = V_{SS} - \frac{I_{OUT} \times DCR1 \times R_{DRP}}{2 \times R_{CSN}}$$

12. Offset Current Setting

The AP3595 integrated IOFS allows the offset current to adjust phase current. The IOFS pin voltage is nominal 0.5V when connecting a resistor to GND and 1.5V when connecting a resistor to VREF. Connecting a resistor from IOFS pin to GND generates a current source as:

$$I_{OFS} = 0.5V / R_{IOFS}$$

This current is added to phase 1 current signal I_{SEN1} for current balance. Consequently, phase 2 will share more percentage of output current. Connecting a resistor from IOFS pin to VREF pin generates a current source as:

$$I_{OFS} = (2V - 1.5V) / R_{IOFS}$$

This current is added to phase 2 current signal I_{SEN2} for current balance. Consequently, phase 1 will share more percentage of output current.

13. PWM Compensation

The output LC filter of a step down converter introduces a double pole, which contributes with -40dB/decade gain slope and 180 degrees phase shift in the control loop. A compensation network among COMP, FB, and V_{OUT} should be added. The compensation network is shown in Figure 32. The output LC filters consist of the output inductors and output capacitors. For two-phase convertor, when assuming that V_{IN1}=V_{IN2}=V_{IN}, L1=L2=L, the transfer function of the LC filter is given by:

$$Gain_{LC} = \frac{1 + s \times R_{ESR} \times C_{OUT}}{s^2 \times (1/2) L \times C_{OUT} + s \times R_{ESR} \times C_{OUT} + 1}$$

The poles and zero of the transfer functions are:

$$f_{LC} = \frac{1}{2 \times \pi \times \sqrt{(1/2) L \times C_{OUT}}}$$

$$f_{ESR} = \frac{1}{2 \times \pi \times R_{ESR} \times C_{OUT}}$$

The f_{LC} is the double-pole frequency of the two-phase LC filters, and f_{ESR} is the frequency of the zero introduced by the ESR of the output capacitors.

Application Information (Continued)

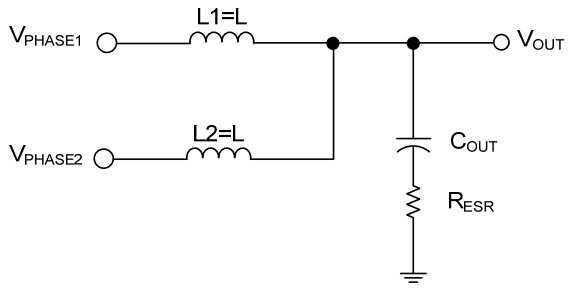


Figure 29. The Output LC Filter

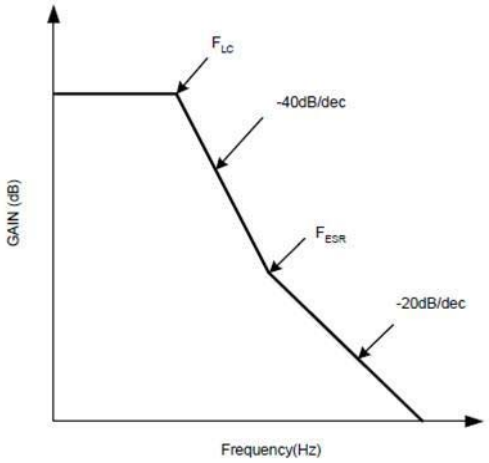


Figure 30. Frequency Response of the LC Filters

The PWM modulator is shown in Figure 31. The input is the output of the error amplifier and the output is the PHASE node. The transfer function of the PWM modulator is given by:

$$Gain_{PWM} = \frac{V_{IN}}{\Delta V_{OSC}}$$

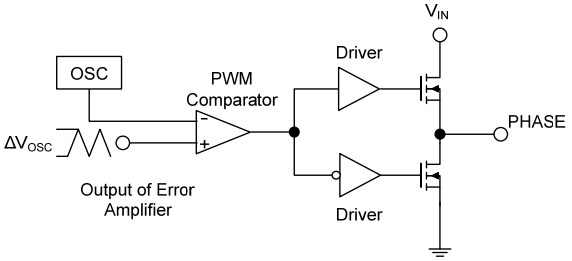


Figure 31. The PWM Modulator

The compensation network is shown in Figure 32. It provides a close loop transfer function with the highest zero crossover frequency and sufficient phase margin. The transfer function of error amplifier is given by:

$$Gain_{AMP} = \frac{V_{COMP}}{V_{OUT}} = \frac{\frac{1}{sC1} // (R2 + \frac{1}{sC2})}{R1 // (R3 + \frac{1}{sC3})}$$

$$= \frac{R1 + R3}{R1 \times R3 \times C1} \times \frac{(s + \frac{1}{R2 \times C2}) \times \{s + \frac{1}{(R1 + R3) \times C3}\}}{s(s + \frac{C1 + C2}{R2 \times C1 \times C2}) \times (s + \frac{1}{R3 \times C3})}$$

The pole and zero frequencies of the transfer function are:

$$f_{Z1} = \frac{1}{2 \times \pi \times R2 \times C2}$$

$$f_{Z2} = \frac{1}{2 \times \pi \times (R1 + R3) \times C3}$$

$$f_{P1} = \frac{1}{2 \times \pi \times R2 \times (\frac{C1 \times C2}{C1 + C2})}$$

$$f_{P2} = \frac{1}{2 \times \pi \times R3 \times C3}$$

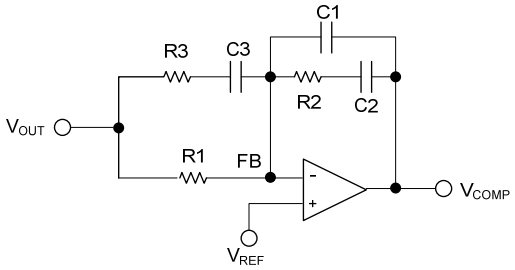


Figure 32. Compensation Network

The closed loop gain of the converter can be written as:

$$Gain_{LC} \times Gain_{PWM} \times Gain_{AMP}$$

Figure 33 shows the asymptotic plot of the closed loop converter gain, and the following guidelines will help to design the compensation network. Using the below guidelines will give a compensation similar to the curve plotted. A stable closed loop has a

Application Information (Continued)

-20dB/decade slope and a phase margin greater than 45 degree.

1. Choose a value for R1, usually between 1kΩ and 5kΩ.

2. Select the desired zero crossover frequency.

$$f_O = (1/5 \sim 1/10) \times f_{SW}$$

Use the following equation to calculate R2:

$$R2 = \frac{\Delta V_{OSC}}{V_{IN}} \times \frac{f_O}{f_{LC}} \times R1$$

3. Place the first zero f_{Z1} before the output LC filter double pole frequency f_{LC}.

$$f_{Z1} = 0.75 \times f_{LC}$$

Calculate the C2 by the equation:

$$C2 = \frac{1}{2 \times \pi \times R2 \times f_{LC} \times 0.75}$$

4. Set the pole at the ESR zero frequency f_{ESR}:

$$f_{P1} = f_{ESR}$$

Calculate the C1 by the following equation:

$$C1 = \frac{C2}{2 \times \pi \times R2 \times C2 \times f_{ESR} - 1}$$

5. Set the second pole f_{P2} at the half of the switching frequency and also set the second zero f_{Z2} at the output LC filter double pole f_{LC}. The compensation gain should not exceed the error amplifier open loop gain. Check the compensation gain at f_{P2} with the capabilities of the error amplifier.

$$f_{P2} = 0.5 \times f_{SW}$$

$$f_{Z2} = f_{LC}$$

Combine the two equations will get the following component calculations:

$$R3 = \frac{R1}{\frac{f_{SW}}{2 \times f_{LC}} - 1}$$

$$C3 = \frac{1}{\pi \times R3 \times f_{SW}}$$

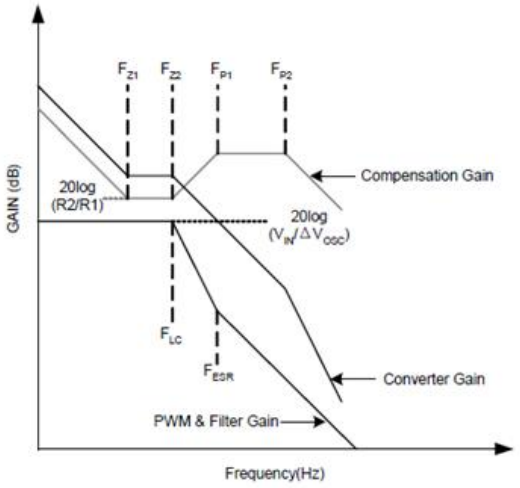


Figure 33. Converter Gain and Frequency

14. Output Inductor Selection

The duty cycle (D) of a buck converter is the function of the input voltage and output voltage. Once an output voltage is fixed, it can be written as:

$$D = V_{OUT} / V_{IN}$$

For two-phase converter, the inductor value (L) determines the sum of the two inductor ripple current, ΔI_{P-P}, and affects the load transient response. Higher inductor value reduces the output capacitors' ripple current and induces lower output ripple voltage. The ripple current can be approximated by:

$$\Delta I_{P-P} = \frac{V_{IN} - 2V_{OUT}}{f_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

Where f_{SW} is the switching frequency of the regulator.

Although the inductor value and frequency are increased and the ripple current and voltage are reduced, a tradeoff exists between the inductor's ripple current and the regulator load transient response time. A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current. Increasing the switching frequency (f_{SW}) also reduces the ripple current and voltage, but it will increase the switching loss of the MOSFETs and the power dissipation of the converter. The maximum ripple current occurs at the maximum input voltage. A good starting point

Application Information (Continued)

is to choose the ripple current to be approximately 30% of the maximum output current. Once the inductance value has been chosen, select an inductor that is capable of carrying the required peak current without going into saturation. In some types of inductors, especially core that is made of ferrite, the ripple current will increase abruptly when it saturates. This results in a larger output ripple voltage.

15. Output Capacitor Selection

Output voltage ripple and the transient voltage deviation are factors that have to be taken into consideration when selecting output capacitors. Higher capacitor value and lower ESR reduce the output ripple and the load transient drop. Therefore, selecting high performance low ESR capacitors is recommended for switching regulator applications. In addition to high frequency noise related to MOSFET turn-on and turn-off, the output voltage ripple includes the capacitance voltage drop ΔV_{COUT} and ESR voltage drop ΔV_{ESR} caused by the AC peak-to-peak sum of the inductor's current. The ripple voltage of output capacitors can be represented by:

$$\Delta V_{COUT} = \frac{\Delta I_{P-P}}{8 \times C_{OUT} \times f_{SW}}$$

$$\Delta V_{ESR} = \Delta I_{P-P} \times R_{ESR}$$

These two components constitute a large portion of the total output voltage ripple. In some applications, multiple capacitors have to be paralleled to achieve the desired ESR value. If the output of the converter has to support another load with high pulsating current, more capacitors are needed in order to reduce the equivalent ESR and suppress the voltage ripple to a tolerable level. A small decoupling capacitor in parallel for bypassing the noise is also recommended, and the voltage rating of the output capacitors must be considered too.

To support a load transient that is faster than the switching frequency, more capacitors are needed for reducing the voltage excursion during load step change.

For getting same load transient response, the output capacitance of two-phase converter only needs to be around half of output capacitance of single-phase converter.

Another aspect of the capacitor selection is that the total AC current going through the capacitors has to be less than the rated RMS current specified on the capacitors in order to prevent the capacitor from overheating.

16. Input Capacitor Selection

Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the surge current needed each time high-side MOSFET turns on. Place the small ceramic capacitors physically close to the MOSFETs and between the drain of high-side MOSFET and the source of low-side MOSFET.

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. For two-phase converter, the RMS current of the bulk input capacitor is roughly calculated as the following equation:

$$I_{RMS} = \frac{I_{OUT}}{2} \times \sqrt{2D \times (1-2D)}$$

For a through hole design, several electrolytic capacitors may be needed. For surface mount design, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating.

17. MOSFET Selection

The AP3595 requires two N-Channel power MOSFETs on each phase. These should be selected based upon $R_{DS(ON)}$, gate supply requirements and thermal management requirements.

In high current applications, the MOSFET power dissipation, package selection, and heatsink are the dominant design factors. The power dissipation includes two loss components: conduction loss and switching loss.

The conduction losses are the largest component of power dissipation for both the high-side and the

Application Information (Continued)

low-side MOSFETs. These losses are distributed between the two MOSFETs according to duty factor (see the equations below). Only the high-side MOSFET has switching losses since the low-side MOSFETs body diode or an external Schottky rectifier across the lower MOSFET clamps the switching node before the synchronous rectifier turns on. These equations assume linear voltage current transitions and do not adequately model power loss due to the reverse-recovery of the low-side MOSFET body diode. The gate-charge losses are dissipated by AP3595 and don't heat the MOSFETs. However, large gate-charge increases the switching interval t_{SW}, which increases the high-side MOSFET switching losses. Ensure that all MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

For the high-side and low-side MOSFETs, the losses are approximately given by the following equations:

$$P_{HIGH\text{-}SIDE}=I_{OUT}^2\times(1+T_C)\times R_{DS(ON)}\times D+0.5\times I_{OUT}\times V_{IN}\times t_{SW}\times f_{SW}$$

$$P_{LOW\text{-}SIDE}=I_{OUT}^2\times(1+T_C)\times(R_{DS(ON)})\times(1-D)$$

Where I_{OUT} is the load current, T_C is the temperature dependency of $R_{DS(ON)}$, f_{SW} is the switching frequency, t_{SW} is the switching interval, D is the duty cycle.

Note that both MOSFETs have conduction losses while the high-side MOSFET includes an additional transition loss. The switching interval, t_{SW}, is the function of the reverse transfer capacitance C_{RSS}. The $(1+T_C)$ term is a factor in the temperature dependency of the $R_{DS(ON)}$ and can be extracted from the "$R_{DS(ON)}$ vs. Temperature" curve of the power MOSFET.

18. Layout Consideration

In any high switching frequency converter, a correct layout is important to ensure proper operation of the regulator.

With power devices switching at higher frequency, the resulting current transient will cause voltage spike across the interconnecting impedance and parasitic circuit elements. As an example, consider the turn-off transition of the PWM MOSFET. Before turn-off condition, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is freewheeling by the low side MOSFET and parasitic diode. Any parasitic inductance of the circuit generates a large voltage spike during the switching interval. In general, using short and wide printed circuit traces should minimize interconnecting impedances and the magnitude of voltage spike.

Besides, signal and power grounds are to be kept separating and finally combined using ground plane construction or single point grounding. The best tie-point between the signal ground and the power ground is at the negative side of the output capacitor on each channel, where there is less noise. Noisy traces beneath the IC are not recommended. Figure 34 illustrates the layout, with bold lines indicating high current paths; these traces must be short and wide. Components along the bold lines should be placed close together. Below is a checklist for your layout:

1. Keep the switching nodes (HGx, LGx, BOOTx, and PHASEx) away from sensitive small signal nodes since these nodes are fast moving signals. Therefore, keep traces to these nodes as short as possible and there should be no other weak signal traces in parallel with theses traces on any layer.

2. The signals going through theses traces have both high dv/dt and high dI/dt with high peak charging and discharging current. The traces from the gate drivers to the MOSFETs (HGx and LGx) should be short and wide.

3. Place the source of the high-side MOSFET and the drain of the low-side MOSFET as close as possible. Minimizing the impedance with wide layout plane between the two pads reduces the voltage bounce of the node. In addition, the large layout plane between the drain of the MOSFETs (V_{IN} and PHASEx nodes) can get better heat sinking.

4. For experiment result of accurate current sensing, the current sensing components are suggested to place close to the inductor part. To avoid the noise interference, the current sensing trace should be away

Application Information (Continued)

from the noisy switching nodes.

5. Decoupling capacitors, the resistor-divider, and the boot capacitor should be close to their pins. (For example, place the decoupling ceramic capacitor as close as possible to the drain of the high-side MOSFET). The input bulk capacitors should be close to the drain of the high-side MOSFET, and the output bulk capacitors should be close to the loads.

6. The input capacitor's ground should be close to the grounds of the output capacitors and the low-side MOSFET.

7. Locate the resistor-divider close to the FB pin to minimize the high impedance trace. In addition, FB pin traces can't be close to the switching signal traces (HGx, LGx, BOOTx, and PHASEx).

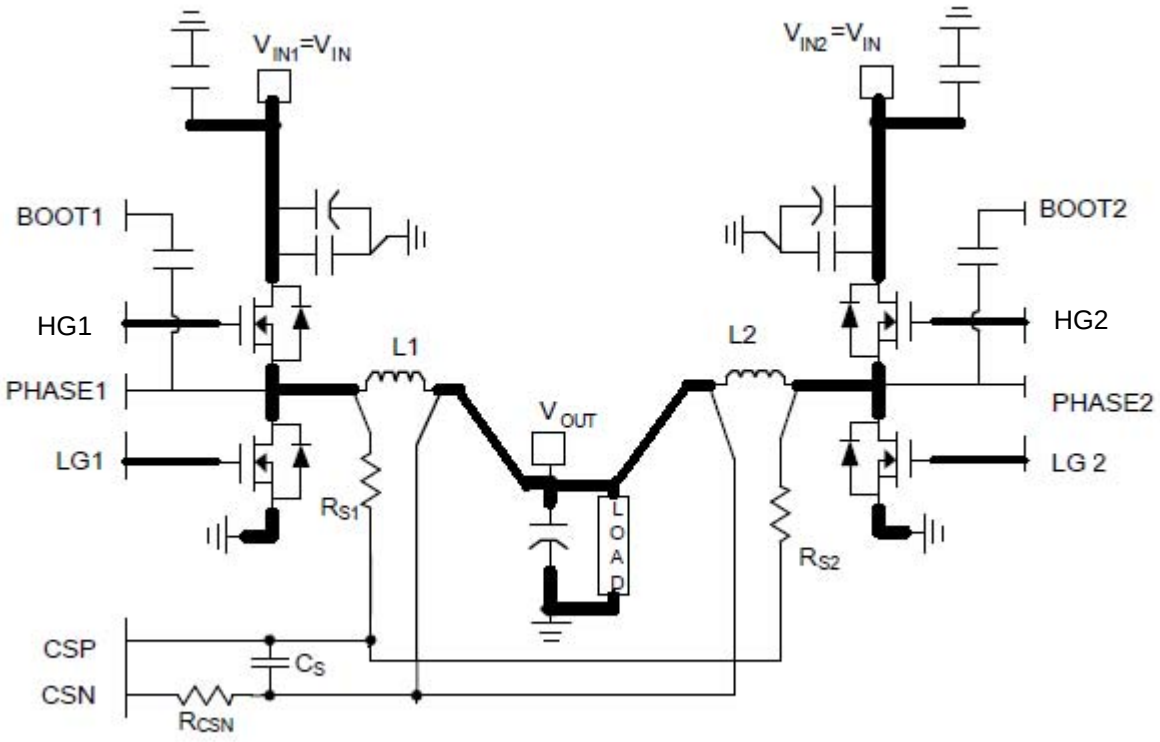
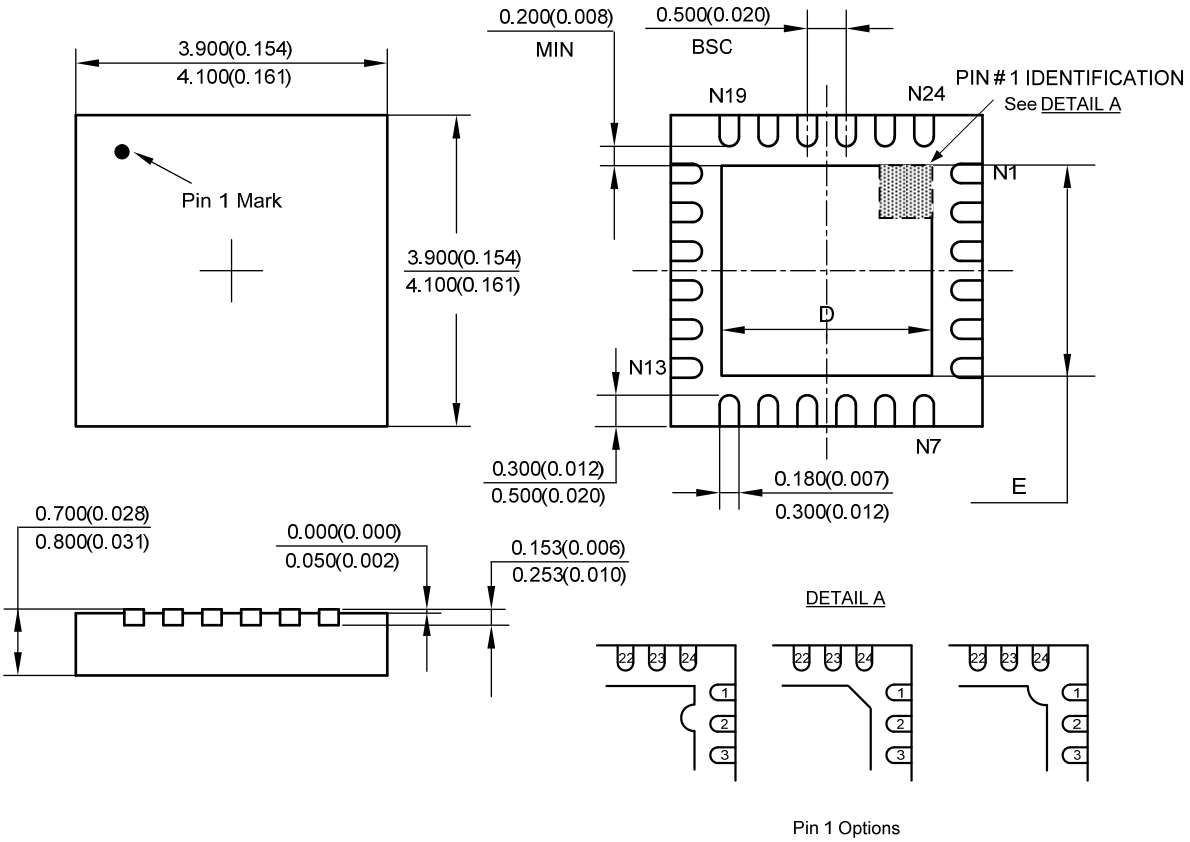


Figure 34. The Layout of AP3595

Mechanical Dimensions

QFN-4×4-24 **Unit: mm(inch)**



Pin 1 Options

Symbol	D				E			
	min(mm)	max(mm)	min(inch)	max(inch)	min(mm)	max(mm)	min(inch)	max(inch)
Option1	2.600	2.800	0.102	0.110	2.600	2.800	0.102	0.110
Option2	2.350	2.550	0.093	0.100	2.350	2.550	0.093	0.100

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