

500V N-Channel Enhancement Mode MOSFET

Description

The AP38N50MP is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.

General Features

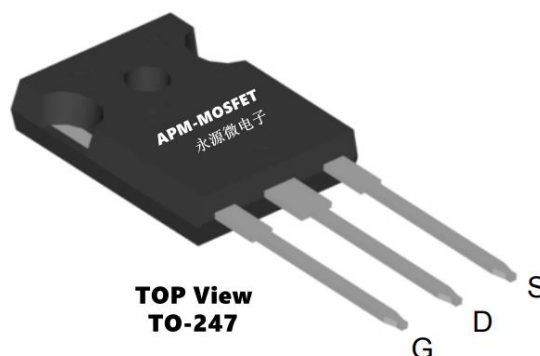
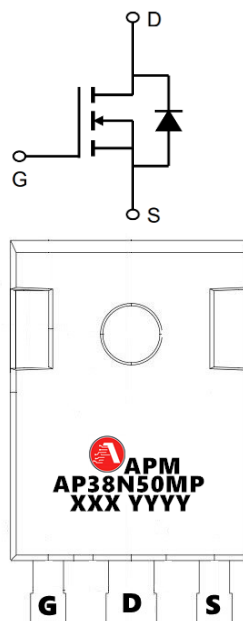
$V_{DS} = 500V$ $I_D = 38A$

$R_{DS(ON)} < 160m\Omega$ @ $V_{GS}=10V$ (Type: 130m Ω)

Application

Uninterruptible Power Supply(UPS)

Power Factor Correction (PFC)



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP34N50MP	TO-247-3L	AP34N50MP XXX YYYY	360

Absolute Maximum Ratings ($T_C=25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage ($V_{GS} = 0V$)	500	V
$I_{D@TC=25^{\circ}C}$	Continuous Drain Current	30	A
$I_{D@TC=100^{\circ}C}$	Continuous Drain Current	38	A
I_{DM}	Pulsed Drain Current (note1)	120	A
V_{GS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy (note2)	3391	mJ
I_{AR}	Avalanche Current (note1)	30	A
P_D	Power Dissipation ($T_C = 25^{\circ}C$)	695	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	$-55 \sim +150$	$^{\circ}C$
R_{thJC}	Thermal Resistance, Junction-to-Case	0.3	$^{\circ}C/W$
R_{thJA}	Thermal Resistance, Junction-to-Ambient	62.5	$^{\circ}C/W$

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Electrical Characteristics ($T_J=25^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V(BR)DSS	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	500	550	--	V
IDSS	Zero Gate Voltage Drain Current	$V_{DS} = 500V, V_{GS} = 0V, T_J = 25^{\circ}\text{C}$	--	--	1	μA
IGSS	Gate-Source Leakage	$V_{GS} = \pm 30V$	--	--	± 100	nA
VGS(th)	Gate-Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.0	3.2	5.0	V
RDS(on)	Drain-Source On-Resistance (Note3)	$V_{GS} = 10V, I_D = 18A$	--	130	180	m Ω
Ciss	Input Capacitance	$V_{GS} = 0V,$ $V_{DS}=25V, f=1.0\text{MHz}$	--	3275	--	pF
Coss	Output Capacitance		--	390	--	
Crss	Reverse Transfer Capacitance		--	7.8	--	
Qg	Total Gate Charge	$V_{DS}=400V, I_D=30A,$ $V_{GS}=10V$	--	60	--	nC
Qgs	Gate-Source Charge		--	17	--	
Qgd	Gate-Drain Charge		--	21	--	
td(on)	Turn-on Delay Time	$V_{DD}=250V, I_D=30A,$ $R_G = 25\Omega$	--	23	--	ns
tr	Turn-on Rise Time		--	57	--	
td(off)	Turn-off Delay Time		--	40	--	
tf	Turn-off Fall Time		--	9	--	
Is	Continuous Body Diode Current	$T_C = 25^{\circ}\text{C}$	--	--	38	A
ISM	Pulsed Diode Forward Current		--	--	136	
VSD	Body Diode Voltage	$T_J = 25^{\circ}\text{C}, I_{SD} = 30A, V_{GS} = 0V$	--	--	1.4	V
trr	Reverse Recovery Time	$V_{GS} = 0V, I_S = 30A, di_F/dt = 100A/\mu s$	--	240	--	ns
Qrr	Reverse Recovery Charge		--	1.0	--	μC

Note :

- 1、The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、The EAS data shows Max. rating . L=0.5 IAS=30A, VDD=50V, RG=25 Ω , Starting $T_J = 25^{\circ}\text{C}$
- 3、The test condition is Pulse Test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 1\%$
- 4、The power dissipation is limited by 150°C junction temperature
- 5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics

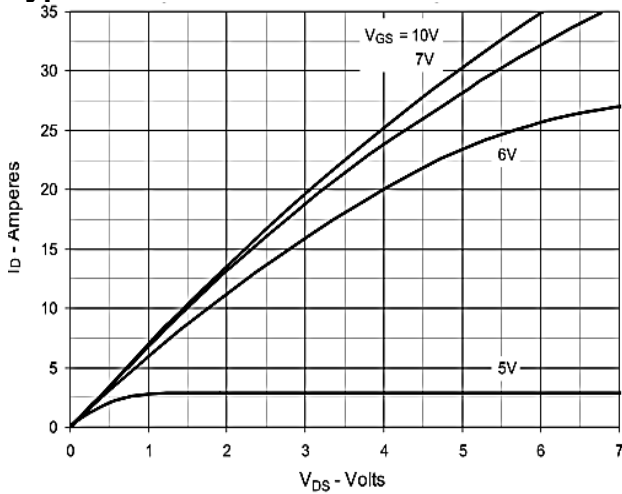


Figure 1. Output Characteristics

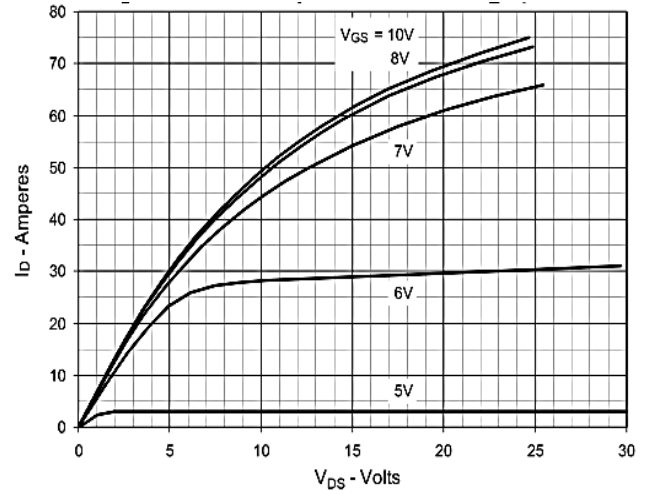


Figure 2. Extended Output Characteristics

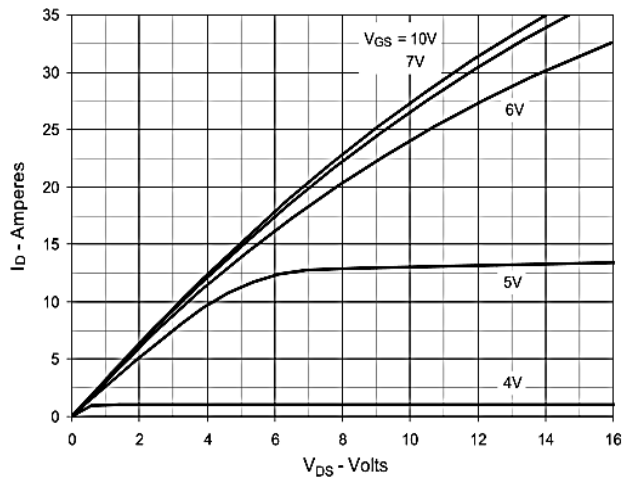


Figure 3. Output Characteristics

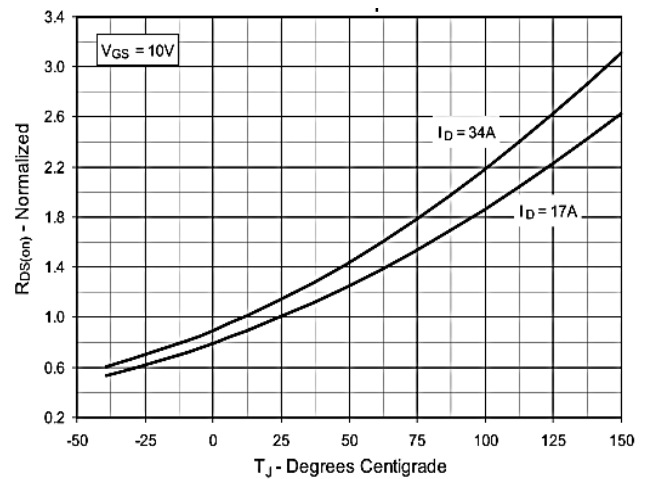


Figure 4. RDS(on) Normalized to ID=17A Value vs.

Junction Temperature

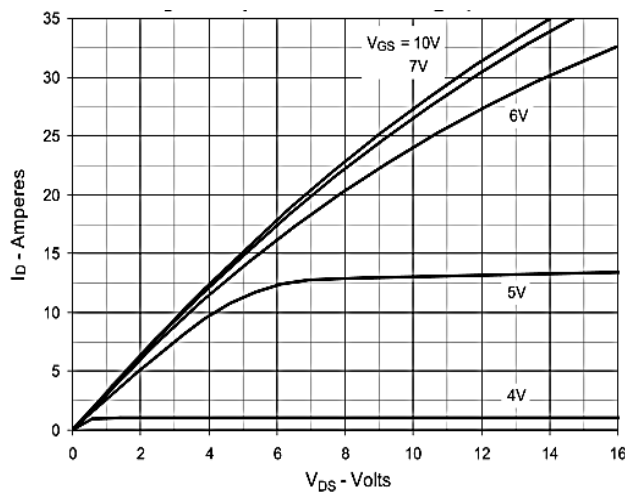


Figure 5. RDS(on) Normalized to ID = 17A Value vs. Current

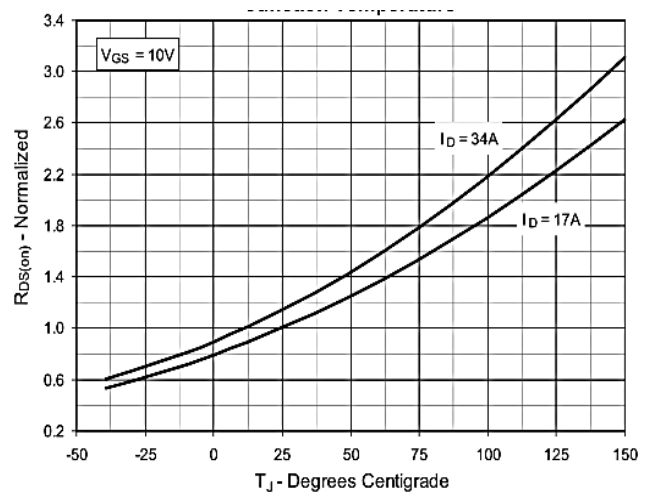


Figure 6. Maximum Drain Current vs. Case Drain Temperature

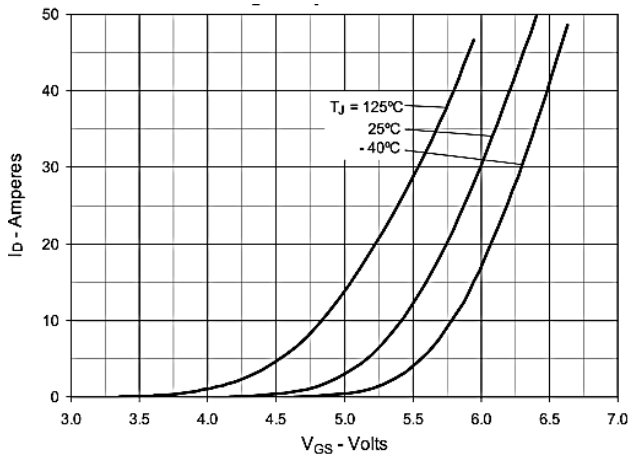


Figure 7. Input Admittance

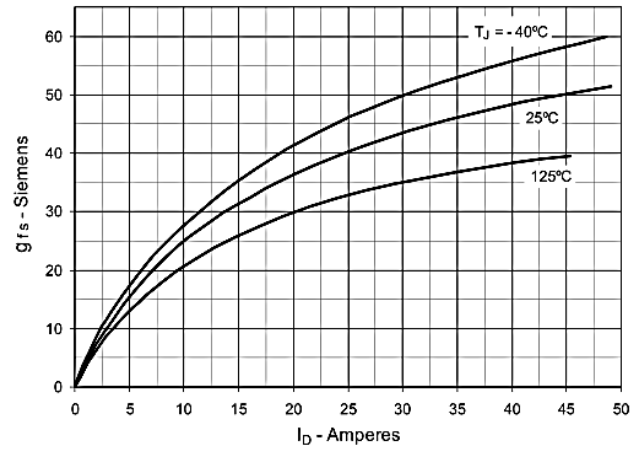


Figure 8. Transconductance

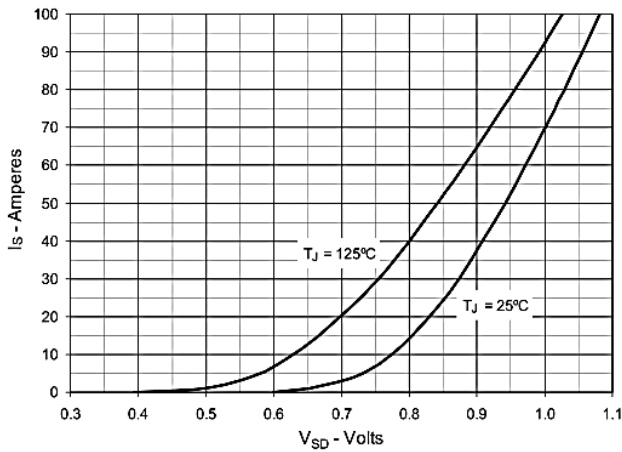


Figure 9. Forward Voltage Drop of Intrinsic Diode

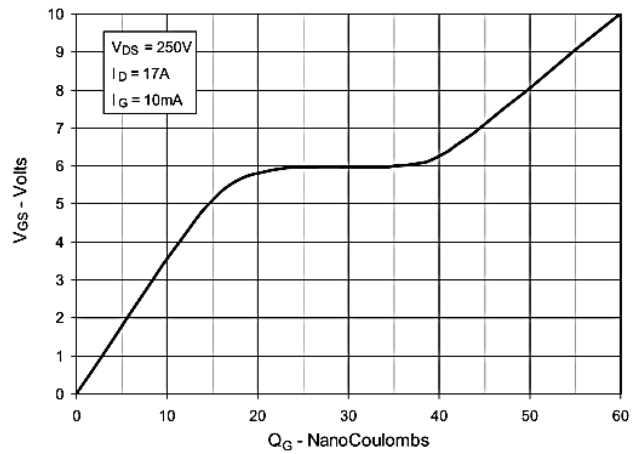


Figure 10. Gate Charge

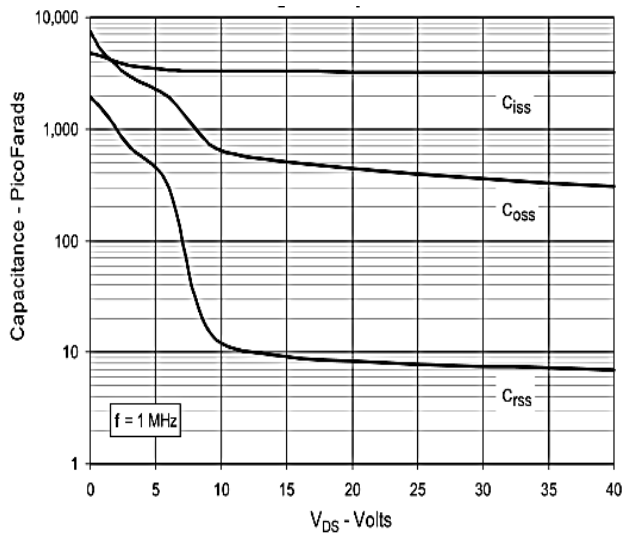


Figure 11 Capacitance

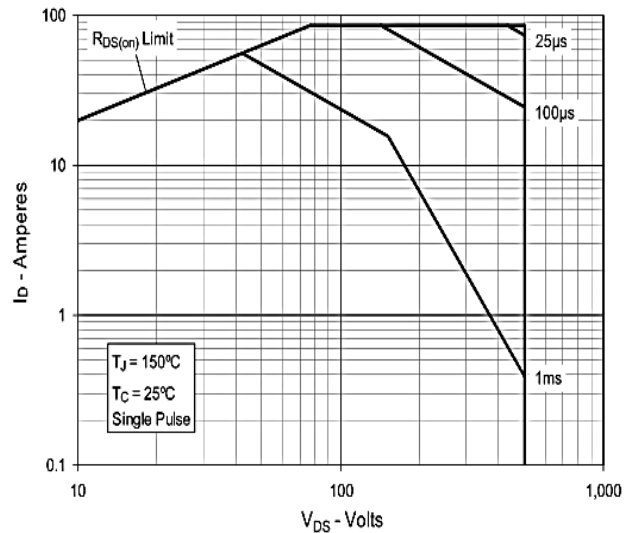


Figure 12. Forward-Bias Safe Operating Area

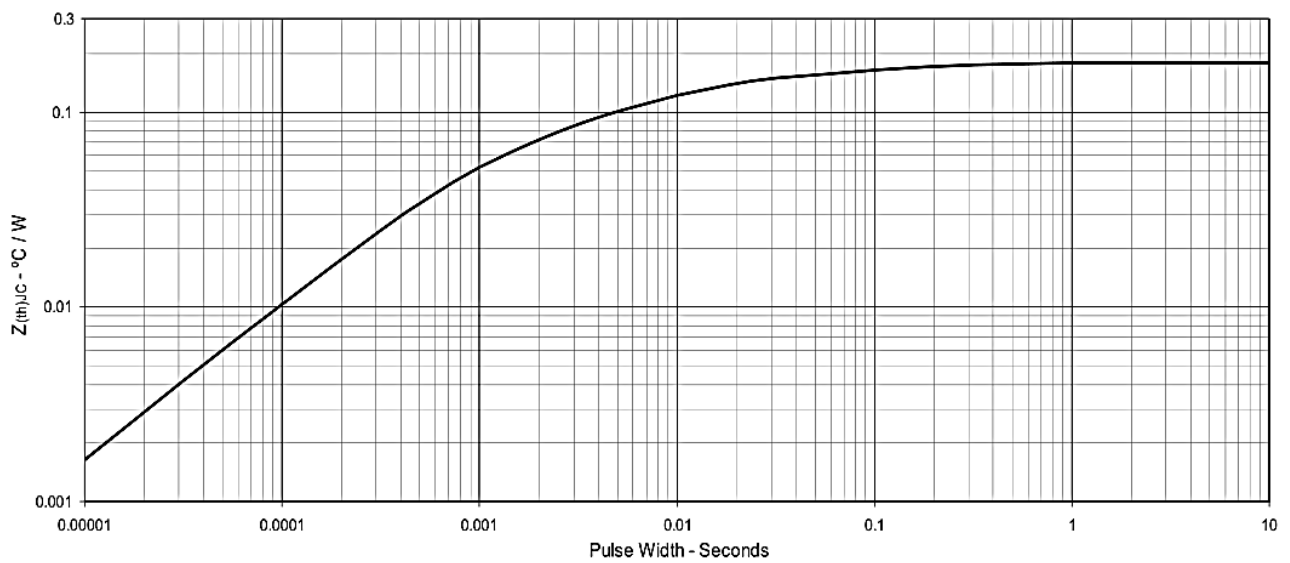
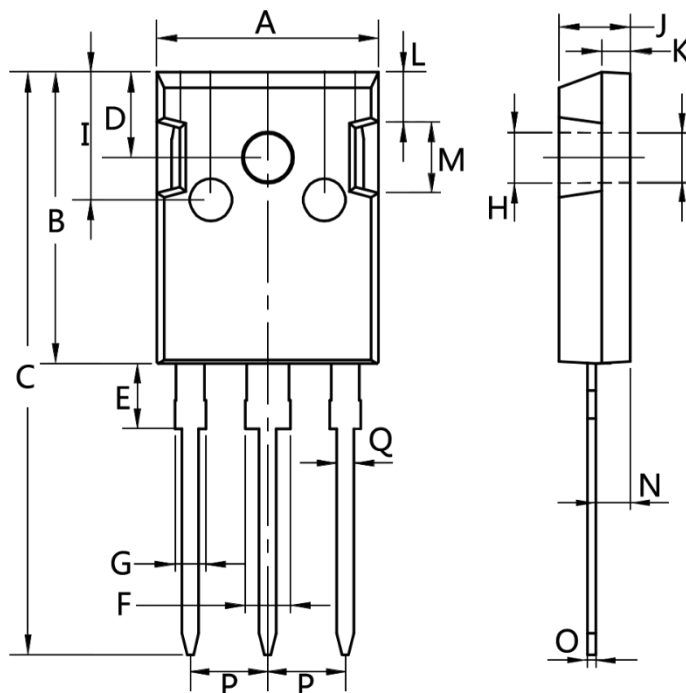


Figure 13, Maximum Transient Thermal Impedance

Package Mechanical Data-TO-247-3L



Dim.	Min.	Max.
A	15.0	16.0
B	20.0	21.0
C	41.0	42.0
D	5.0	6.0
E	4.0	5.0
F	2.5	3.5
G	1.75	2.5
H	3.0	3.5
I	8.0	10.0
J	4.9	5.1
K	1.9	2.1
L	3.5	4.0
M	4.75	5.25
N	2.0	3.0
O	0.55	0.75
P	Typ 5.08	
Q	1.2	1.3

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Edition	Date	Change
REV1.0	2023/1/31	Initial release

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