NEW PRODUCT

Description

The AP3983R is a power switcher for power supplies with better conversion efficiency, better voltage & current accuracy, and improved protection functions. Typical applications include chargers and adapters. The AP3983R with built-in MOSFET, regulates the output voltage and current in the primary side by piecewise Pulse Frequency Modulation (p-PFM) in discontinuous conduction mode (DCM). The system operating frequency reduces linearly from heavy load to light load in each interval of the p-PFM, and enters constant current mode when the load current equals to the maximum system output current.

The AP3983R provides accurate constant voltage (CV), constant current (CC) and outstanding dynamic performance without requiring an opto-coupler. It also eliminates the need for loop compensation circuitry while maintaining stability.

The AP3983R has a built-in fixed cable voltage drop compensation of 8% and adjustable line-voltage compensation.

The AP3983R achieves excellent regulation and high average efficiency, less than 2s startup time for 75mW standby power solution. When the AP3983R is adopted with APR3415, good undershoot performances can be achieved.

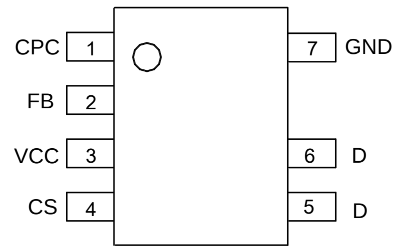
The AP3983R is packaged in SO-7.

Applications

- Adapters/Chargers
- Standby and Auxiliary Power Supplies

Pin Assignments

(Top View)



SO-7 (M Package) For AP3983R

Features

- Built-in N Channel MOSFET with 700 BV_{DSS}
- Less than 75mW Standby Power Consumption
- Meet Efficiency Requirement of COC Trier 2
- Valley Turn-on to Reduce Switching Loss and Improve EMI
- Piecewise Frequency Reduction to Enhance Conversion Efficiency and Suppress Audio Noise
- Overvoltage Protection (OVP)
- Over-Temperature Protection (OTP)
- Short Circuit Protection (SCP) with Hiccup
  Operating Frequency Jitter Function for Conductive EMI Suppression
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. “Green” Device (Note 3)**

Notes: 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated’s definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green” products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit

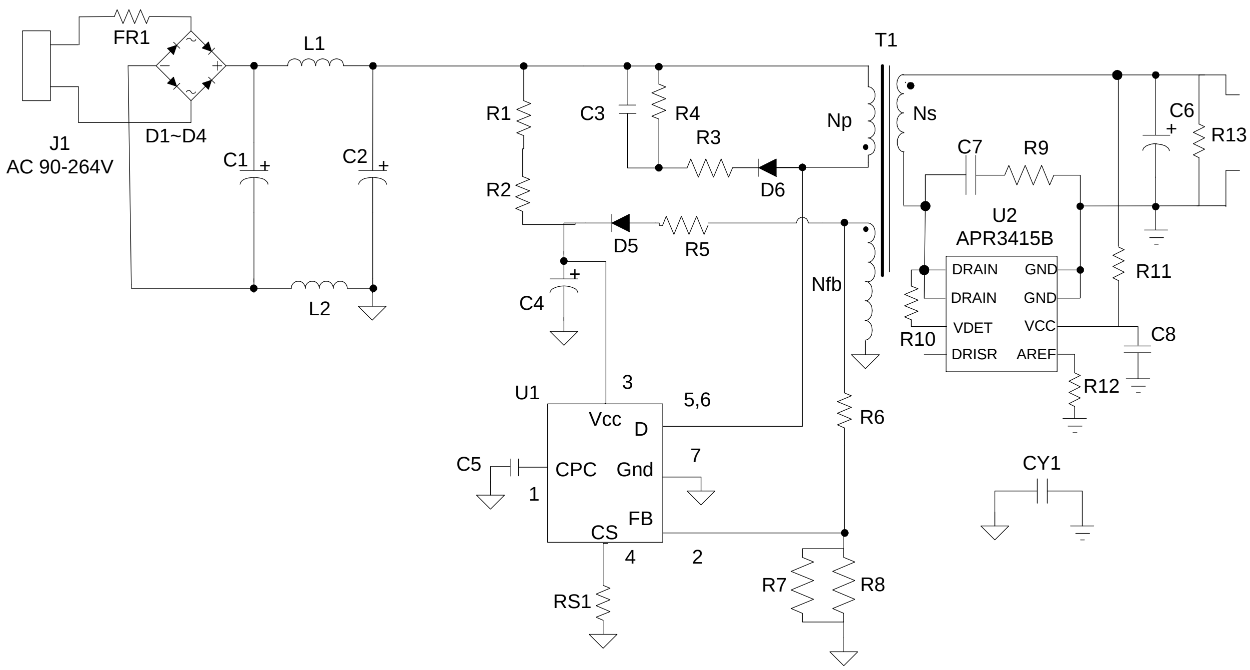
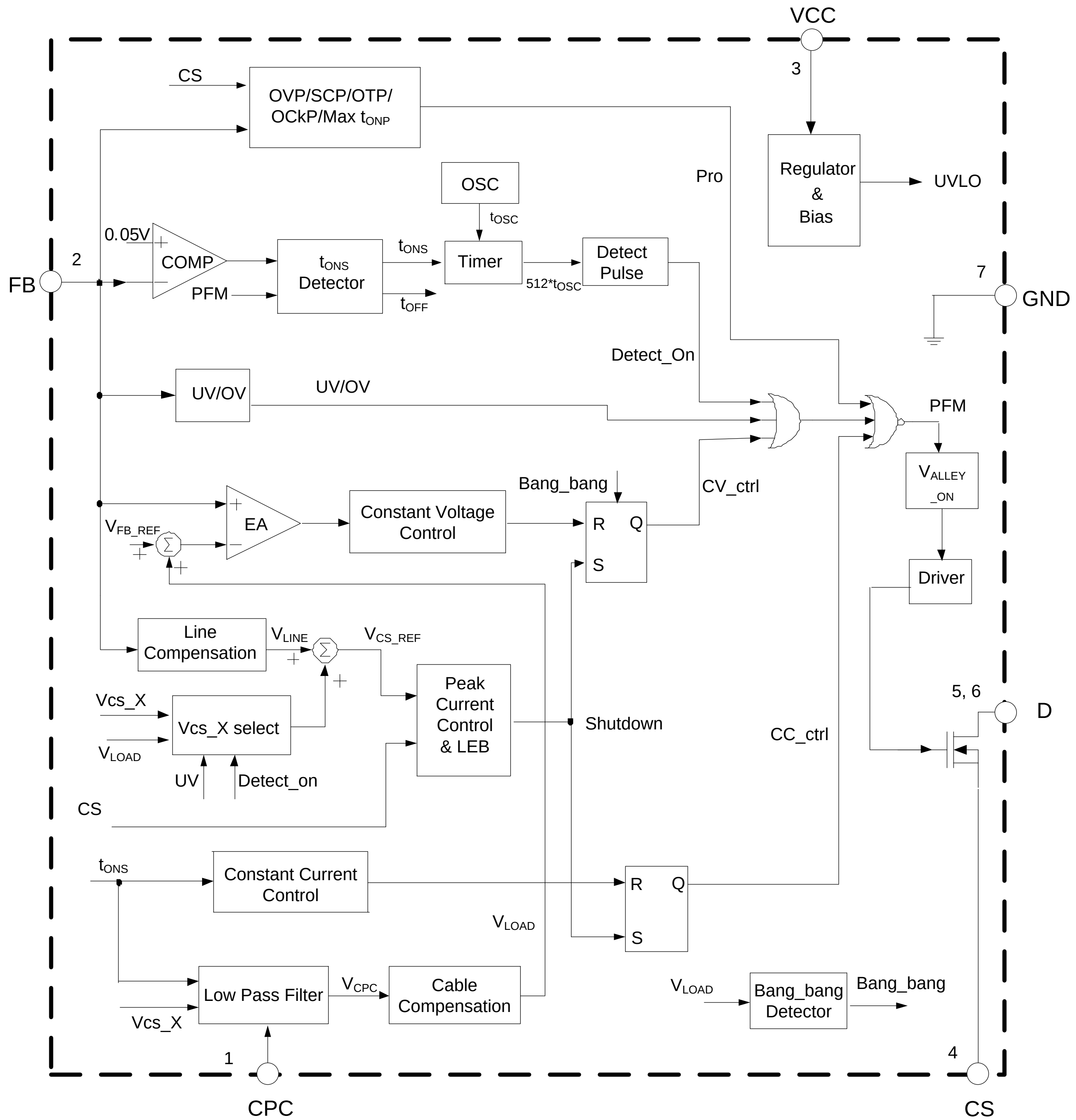


Figure 1 Typical Application Circuit of AP3983R

Pin Descriptions

Pin Number	Pin Name	Function
1	CPC	A capacitor about 50nF should be connected to this pin. The voltage of CPC pin is linear to load of the system and it is used for the functions of cable voltage drop compensation and audio noise suppression
2	FB	The CV and CC regulation are realized based on the voltage sampling of this pin
3	VCC	The VCC pin supplies the power for the IC. In order to get the correct operation of the IC, a capacitor should be placed as close as possible to the VCC pin
4	CS	The CS is the current sense pin of the IC. The IC will turn off the power MOSFET according to the voltage on the CS pin
5, 6	Drain	High Voltage of MOSFET
7	GND	The ground of the switcher

Functional Block Diagram



NEW PRODUCT

Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating	Unit
V_{CC}	Supply Voltage	-0.3 to 35	V
V_{CS}, V_{CPC}	Voltage on CS, CPC Pin	-0.3 to 7	V
V_{FB}	FB Input Voltage	-0.4 to 10	V
I_{SOURCE}	Source Current from OUT Pin	Internally Limited	A
T_J	Operating Junction Temperature	-40 to +150	°C
T_{STG}	Storage Temperature	-65 to +150	°C
BV_{DSS}	Drain Voltage (T_J = +25°C)	700	V
I_D	Drain Continuous Current (T_J = +25°C)	4	A
T_{LEAD}	Lead Temperature (Soldering, 10 sec)	+300	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	200	°C/W
ESD	ESD (Human Body Model)	2,000	V
	ESD (Charged Device Model)	200	V

Note: 4. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

Electrical Characteristics (@V_{CC}=15V, T_A=+25°C, unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
STARTUP AND UVLO SECTION						
V_{TH_ST}	Startup Threshold	–	13	15.5	18	V
$V_{OPR(MIN)}$	Minimal Operating Voltage	–	6	6.8	7.6	V
STANDBY CURRENT SECTION						
I_{ST}	Startup Current	V_{CC}=V_{TH_ST}-1V before startup	0.01	0.2	0.6	µA
I_{CC_OPR}	Operating Current	Static current @ no load	300	450	600	
OPERATING FREQUENCY SECTION (LL MODE TO FULL LOAD)						
$f_{S(MAX)}$	Maximum Operating Frequency	$I_{O(MAX)}$ (Note 5)	–	–	80	kHz
t_{SAMPLE_H}	Sample Time	37% to 100% $I_{O(MAX)}$	3.8	4.2	4.6	µs
t_{SAMPLE_L}		0% to 37% $I_{O(MAX)}$ (Note 6)	2.15	2.4	2.65	µs
OPERATING FREQUENCY SECTION (LL MODE)						
$V_{CPC(EN)}$	CPC Pin Voltage to Enter LL Mode	–	18	20	22	mV
$V_{CPC(EX)}$	CPC Pin Voltage to Exit LL Mode	–	36	40	44	mV
$t_{OFF(EN)}$	Off Time to Enter LL Mode	From the end of t_{ONS}	230	256	282	µs
$t_{OFF(EX)}$	Off Time to Exit LL Mode	From the end of t_{ONS}	230	256	282	µs

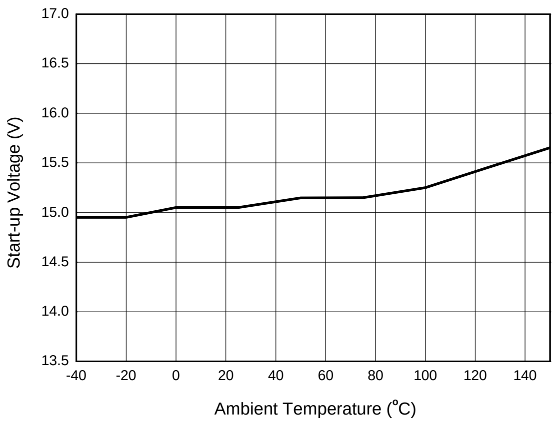
Electrical Characteristics (continued) (@V_{CC} =15V, T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
FREQUENCY JITTER						
$\Delta V_{CS}/V_{CS}$	V_{CS} Modulation	6.5% to 100% $I_{O(MAX)}$	4.5	5	5.5	%
f_{MOD}	V_{CS} Modulation Frequency		3.6	4	4.4	kHz
CURRENT SENSE SECTION						
V_{CS_H}	Peak Current Sense Threshold Voltage	37% to 100% $I_{O(MAX)}$	828	900	972	mV
V_{CS_L}		0% to 37% $I_{O(MAX)}$	460	500	540	mV
R_{LINE}	Built-in Line Compensation Resistor	(Note 7)	245	260	275	Ω
t_{LEB}	Leading Edge Blanking	(Note 6)	400	500	600	ns
CONSTANT VOLTAGE SECTION						
V_{FB}	Feedback Threshold Voltage	Closed loop test of V_{OUT}	3.95	4.01	4.07	V
R_{FB}	FB Pin Input Resistance	V_{FB} = 4V	560	700	840	kΩ
V_{CABLE}/V_{OUT}	Cable Compensation Ratio	V_{FB} @FULLLOAD-VFB)/VFB	7	8	9	%
CONSTANT CURRENT SECTION						
t_{ONS}/t_{SW}	Secondary Winding Conduction Duty	V_{FB} = 4V	0.47	0.5	0.53	–
VALLEY-ON SECTION						
$t_{VAL\text{-}ON}$	Valid Off Time of Valley-on	From the end of t_{ONS}	14.4	16	17.6	µs
DYNAMIC SECTION						
$V_{TRIGGER}$	Trigger Voltage for Dynamic Function	–	74	83	92	mV
t_{DELAY}	Delay Time for Dynamic Function	From the end of t_{ONS}	115	128	141	µs
V_{UV_H}	Undervoltage of FB Pin for V_{CS_H}	–	3.82	3.89	3.96	V
POWER MOSFET SECTION						
BV_{DSS}	Drain-Source Breakdown Voltage	–	700	–	–	V
$R_{DS(ON)}$	On State Resistor	–	–	–	1.4	Ω
PROTECTION FUNCTION SECTION						
$V_{FB(OVP)}$	Overvoltage Protection at FB Pin	–	7.1	7.5	7.9	V
$V_{CC(OVP)}$	Overvoltage Protection at VCC Pin	–	28	30	32	V
$t_{ONP(MAX)}$	Maximum Turn-on Time	–	13	19	25	µs
$V_{FB(SCP)}$	Short Circuit Protection	V_{FB} @ Hiccup	2.45	2.6	2.75	V
t_{SCP}	Maximum Time Under $V_{FB(SCP)}$	–	115	128	141	ms
T_{OTP}	Shutdown Temperature	–	+144	+160	+176	°C
T_{HYS}	Temperature Hysteresis	–	+36	+40	+44	°C

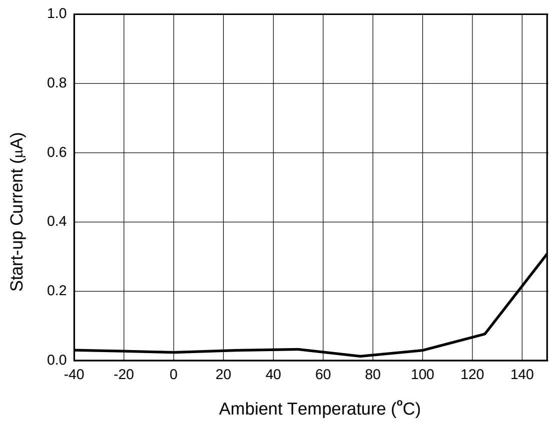
Notes: 5. The output constant-current design value, generally set to 110% to 120% of full load.
6. Guaranteed by design.
7. Line compensation voltage on CS reference: $\Delta V_{CS\_REF} = 0.438 \times \frac{R_{LINE}}{R_{FB1} + R_{LINE}} \times V_{AUX}$.

Performance Characteristics

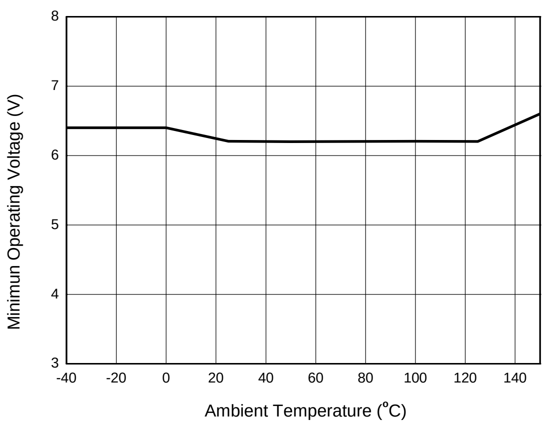
Start-up Voltage vs. Ambient Temperature



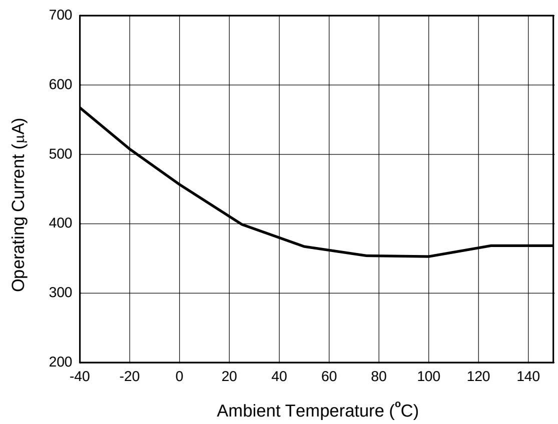
Start-up Current vs. Ambient Temperature



Minimal Operating Voltage vs. Ambient Temperature

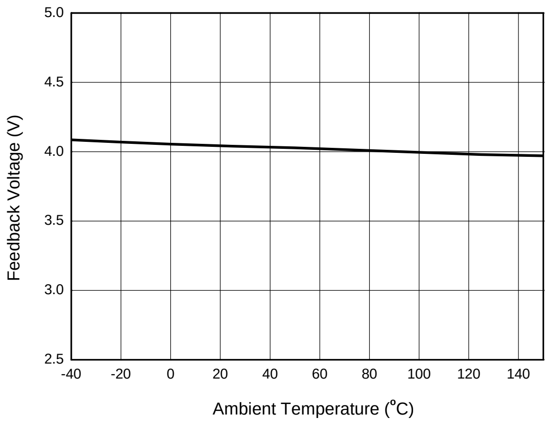


Operating Current vs. Ambient Temperature

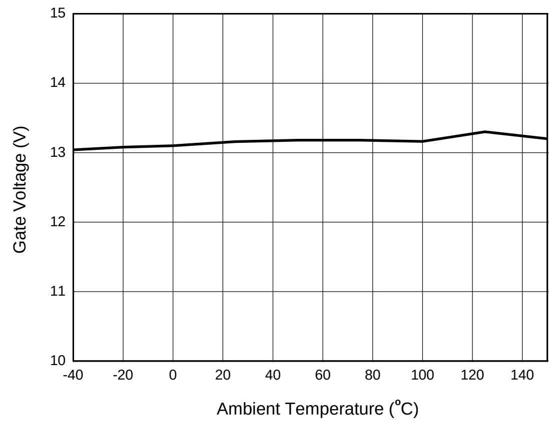


Performance Characteristics (Cont.)

Feedback Voltage vs. Ambient Temperature



Gate Voltage vs. Ambient Temperature



Operation Principle Description

Figure 1 is the typical application circuit of the AP3983R, which is a conventional flyback converter with a 3-winding transformer--primary winding (N_P), secondary winding (N_S) and auxiliary winding (N_{AUX}). The auxiliary winding is used for providing V_{CC} supply voltage for IC and sensing the output voltage feedback signal to FB pin.

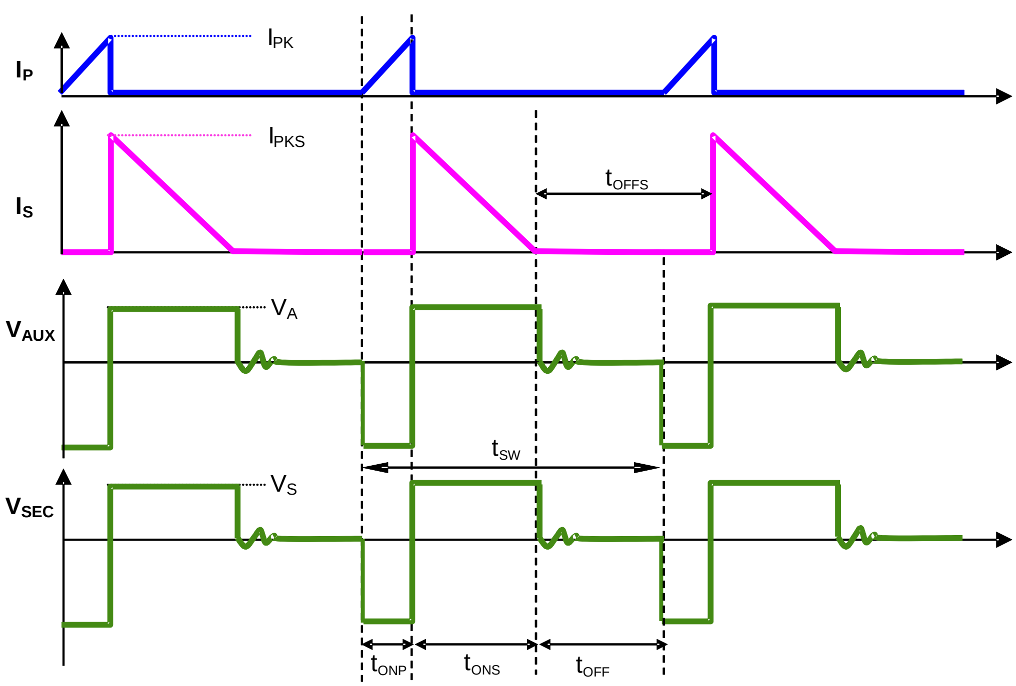


Figure 2 The Operation Waveform of Flyback PSR System

Operation Principle Description (Cont.)

Figure 2 shows the typical waveforms which demonstrate the basic operating principle of the AP3983R application. And the parameters are defined as the following.

I_P---The primary side current
I_S ---The secondary side current
I_{PK}---Peak value of primary side current
I_{PKS}---Peak value of secondary side current
V_{SEC}---The transient voltage at secondary winding
V_S---The stable voltage at secondary winding when rectification diode is in conducting status, which equals the sum of output voltage V_{OUT} and the forward voltage drop of diode
V_{AUX}---The transient voltage at auxiliary winding
V_A--- The stable voltage at auxiliary winding when rectification diode is in conducting status, which equals the sum of voltage VCC and the forward voltage drop of auxiliary diode
t_{SW} ---The period of switching frequency
t_{ONP} ---The conduction time when primary side switch is “ON”
t_{ONS} ---The conduction time when secondary side diode is “ON”
t_{OFF} ---The dead time when neither primary side switch nor secondary side diode is “ON”
t_{OFFS} --- The time when secondary side diode is “OFF”

For primary-side regulation, the primary current ip(t) is sensed by a current sense resistor R_{CS} (as shown in Figure 1).The current rises up linearly at a rate of:

$$\frac{dip(t)}{dt} = \frac{V_{IN}(t)}{L_M} \quad (1)$$

As illustrated in Figure 2, when the current ip(t) rises up to I_{PK}, the switch Q1 turns off. The constant peak current is given by:

$$I_{PK} = \frac{V_{CS}}{R_{CS}} \quad (2)$$

The energy stored in the magnetizing inductance L_M each cycle is therefore:

$$E_G = \frac{1}{2} \times L_M \cdot I_{PK}^2 \quad (3)$$

So the power transferring from the input to the output is given by:

$$P = \frac{1}{2} \times L_M \times I_{PK}^2 \times f_{SW} \quad (4)$$

Where, the f_{SW} is the switching frequency. When the peak current I_{PK} is constant, the output power depends on the switching frequency f_{SW}.

Constant Voltage Operation
As to constant-voltage (CV) operation mode, the AP3983R detects the auxiliary winding voltage at FB pin to regulate the output voltage. The auxiliary winding voltage is coupled with secondary side winding voltage, so the auxiliary winding voltage at D1 conduction time is:

$$V_{AUX} = \frac{N_{AUX}}{N_S} \times (V_O + V_D) \quad (5)$$

Where V_D is the diode forward voltage drop.

NEW PRODUCT

Operation Principle Description (Cont.)

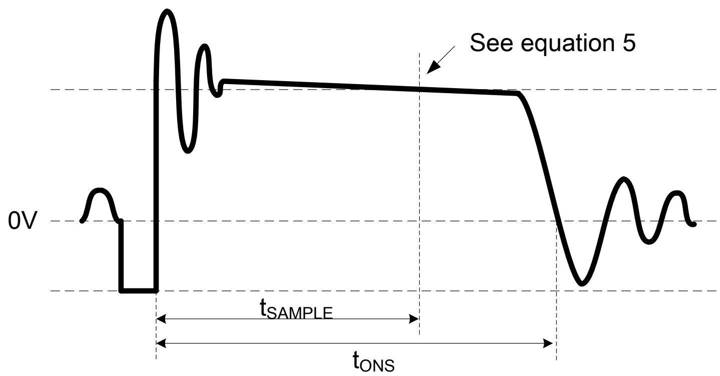


Figure 3 Auxiliary Voltage Waveform

The voltage detection point is at a constant delay time of the D1 on-time. The constant delay time is changed with the different primary peak current. The CV loop control function of the AP3983R then generates a D1 off-time to regulate the output voltage.

Constant Current Operation

The AP3983R can work in constant-current (CC) mode. Figure 2 shows the secondary current waveforms.

In CC operation mode, the CC control loop of the AP3983R will keep a fixed proportion between D1 on-time t_{ONS} and D1 off-time t_{OFFS}. The fixed proportion is:

$$\frac{t_{ONS}}{t_{OFFS}} = \frac{4}{4} \quad (6)$$

The relationship between the output constant-current and secondary peak current Ipks is given by:

$$I_{O(MAX)} = \frac{1}{2} \times I_{PKS} \times \frac{t_{ONS}}{t_{ONS} + t_{OFFS}} \quad (7)$$

As to tight coupled primary and secondary winding, the secondary peak current is:

$$I_{PKS} = \frac{N_P}{N_S} \times I_{PK} \quad (8)$$

Thus the output constant-current is given by:

$$I_{O(MAX)} = \frac{1}{2} \times \frac{N_P}{N_S} \times I_{PK} \times \frac{t_{ONS}}{t_{ONS} + t_{OFFS}} = \frac{2}{8} \times \frac{N_P}{N_S} \times I_{PK} \quad (9)$$

Therefore, the AP3983R can realize CC mode operation by constant primary peak current and fixed diode conduction duty cycle.

Multiple Segment Constant Peak Current

As to the original PFM PSR system, the switching frequency decreases with output current decreasing, which will encounter audible noise issue since switching frequency decreases to audio frequency range, about less than 20kHz.

In order to avoid audible noise issue, the AP3983R uses 2-segment constant primary peak current control method. At constant voltage mode, the current sense threshold voltage is of multiple segments with different loading, as shown in Figure 4, which are V_{CS_H} for high load, V_{CS_L} for light load and LL Mode. At constant current mode, the current sense threshold voltage is always V_{CS_H}.

Operation Principle Description (Cont.)

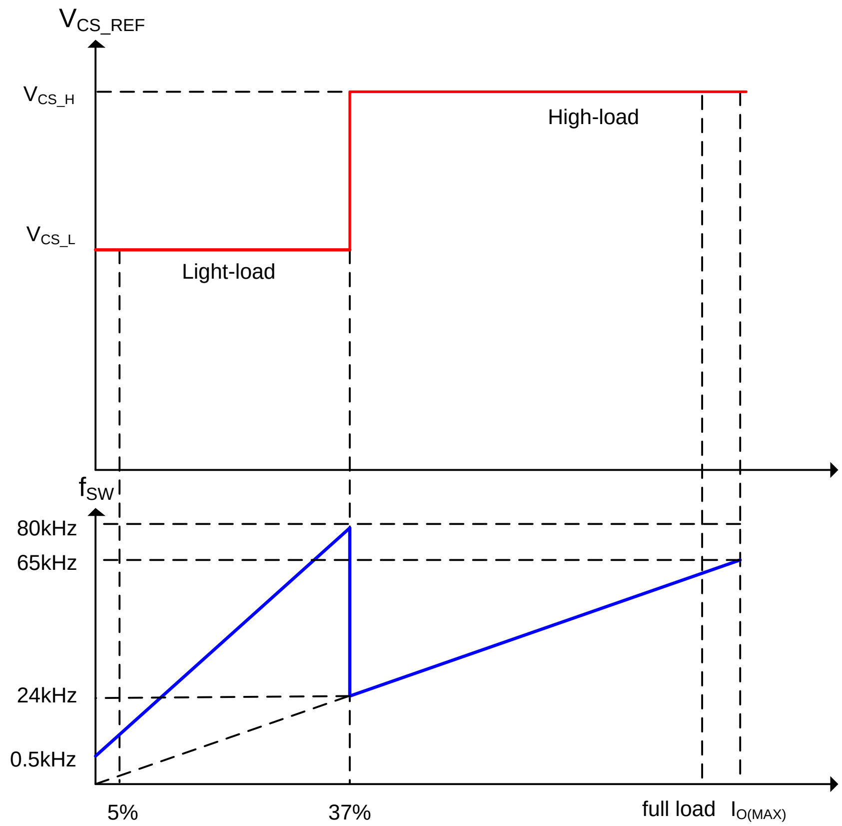


Figure 4 Multiple Segment Peak Current at CV Mode

It can be seen from Figure 4, with multiple segment peak current control, the AP3983R power system can keep switching frequency above 24kHz at whole heavy load and most of light load to guarantee the audible noise-free performance.

Constant Voltage Operation in LL Mode and Dynamic Response

In primary side regulation of the AP3983R application, APR3415 must be used at secondary side as the output voltage regulator, low standby power and excellent dynamic response can be achieved. When the output voltage detected by APR3415 is lower than its trigger voltage, APR3415 outputs periodical signals which will be coupled to auxiliary side. When the AP3983R detects the signal which is valid that the signal voltage is higher than $V_{TRIGGER}$ and t_{OFF} is longer than t_{DELAY}, the AP3983R will begin an operating pulse, then primary switch immediately turns on to provide one energy pulse to output terminal and primary V_{CC}.

By fast response and cooperation, the APR3415 and AP3983R can maintain a constant output voltage with very low operating frequency in LL mode and also can effectively improve dynamic performance for primary side regulation power systems.

The conditions of entering LL mode---V_{CPC}<20mV and t_{OFF}>256μs.
The condition of exiting LL mode---V_{CPC} ≥40mV or t_{OFF}<256μs.
The critical point of the LL mode is generally about 5% $I_{O(MAX)}$.

3-Segment Drive Current for Radiative EMI Suppression

When the power switch is turned on, a turn-on spike will occur, that worsens the radiative EMI. It is an effective way to decrease drive current before gate voltage gets to miller platform. The AP3983R uses 3-segment drive current for radiative EMI suppression, as shown in Figure 5. When gate voltage gets to 6V, the AP3983R drive current switches from low current (43mA) to high current (110mA). When the gate voltage gets to 10V, the drive current will decrease gradually to 0mA until the gate voltage goes up to the clamp voltage (13V).

Operation Principle Description (Cont.)

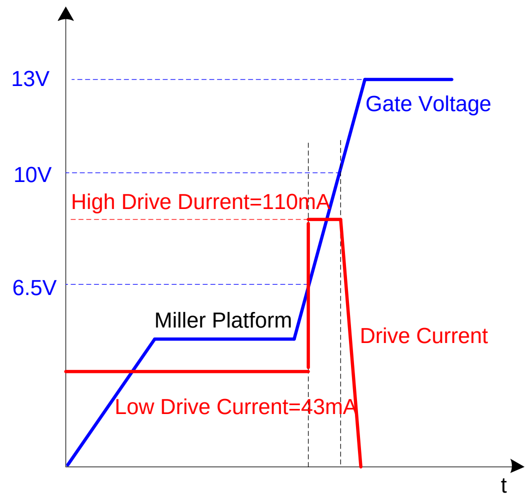


Figure 5 Drive Current and Gate Voltage

Leading Edge Blanking (LEB) Time

When the power switch is turned on, a turn-on spike will occur on the sense resistor. To avoid false turn off switch, a leading-edge blanking is built in. During this blanking time, the current sense comparator is disabled and the external power switch cannot be turned off.

Adjustable Line Compensation and Fixed Cable Compensation

The AP3983R power system can adjust line compensation by changing the upper resistor at FB pin. The line compensation capability is increased by decreasing the resistance of the upper FB resistor.

Cable compensation is fixed in the AP3983R.

Valley Turn-On

When the off time (t_{OFF}) is lower than 16µs, the AP3983R power system can work with valley turn-on. It can reduce MOSFET switching-on power losses which is resulted from the equivalent output capacitance. At the same time, because of valley turn-on, the switching frequency has the random jitter feature, which will be beneficial for conductive EMI performance. And valley turn-on can also reduce the power switch turn-on spike current and then result in the better radiative EMI performance.

Frequency Jitter

Even though the valley turn-on function can lead the random frequency jitter feature, an active frequency jitter function is added to the AP3983R to ensure the frequency jitter performance in the whole loading condition. By adjusting the V_{CS_REF} with deviation of 5.0% every 256µs cycle, the active frequency jitter can be realized.

Short Circuit Protection (SCP)

Short Circuit Protection (SCP) detection principle is similar to the normal output voltage feedback detection by sensing FB pin voltage. When the detected FB pin voltage is below $V_{FB(SCP)}$ for a duration of about 128ms, the SCP is triggered. Then the AP3983R enters hiccup mode that the IC immediately shuts down and then restarts, so that the V_{CC} voltage changes between V_{TH_ST} and UVLO threshold until $V_{FB(SCP)}$ condition is removed.

As to the normal system startup, the time duration of FB pin voltage below $V_{FB(SCP)}$ should be less than t_{SCP} to avoid entering SCP mode. However, for the output short condition or the output voltage below a certain level, the SCP mode will be triggered.

Operation Principle Description (Cont.)

Figure 6 is the AP3983R normal start-up waveform that the voltage of FB pin is above $V_{FB(SCP)}$ during t_{SCP} after V_{CC} gets to the V_{TH_ST}, which doesn't enter the SCP mode. As shown in Figure 7, V_{OUT} is short and the voltage of FB pin is lower than $V_{FB(SCP)}$ during t_{SCP}, the AP3983R triggers the SCP and enter the hiccup mode.

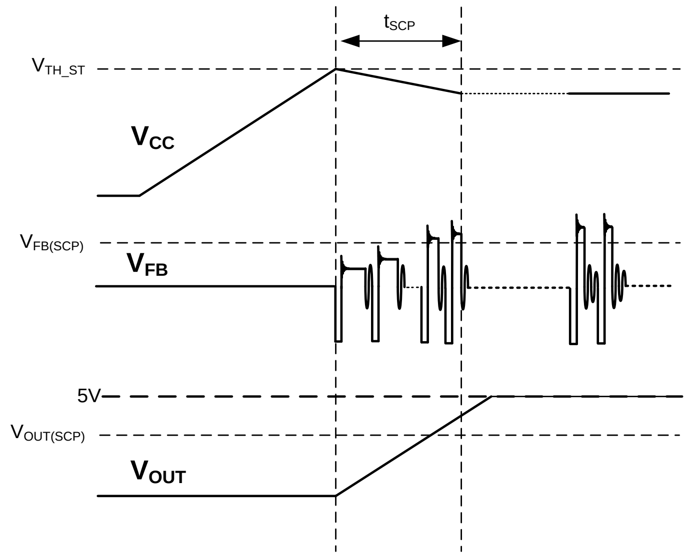


Figure 6 Normal Start-up

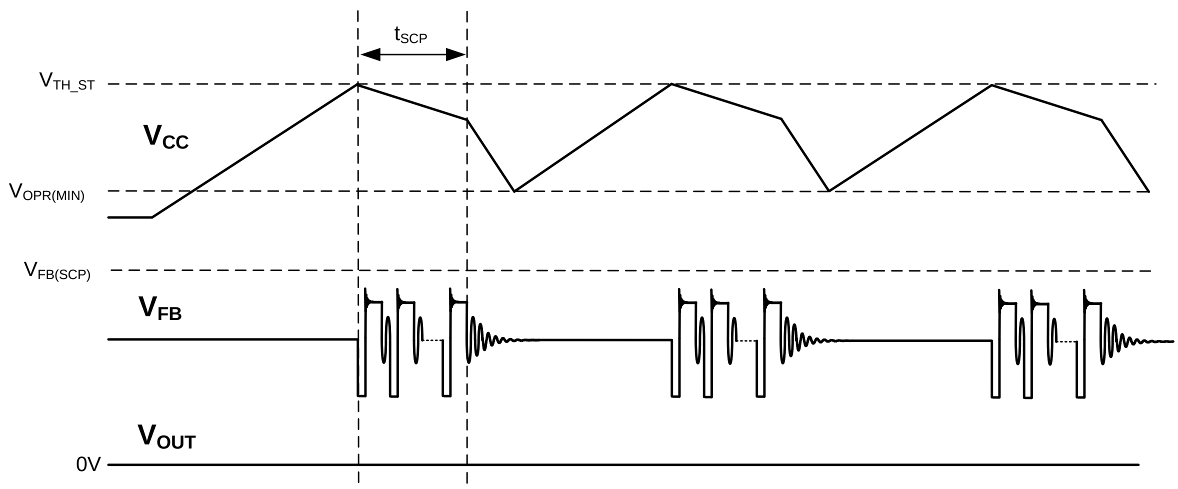


Figure 7 Short Circuit Protection (SCP) and Hiccup Mode

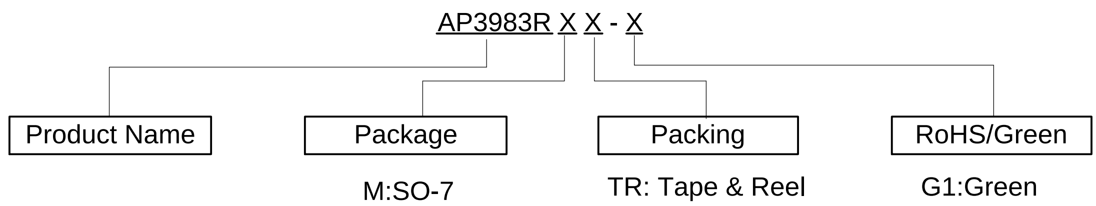
OVP

The AP3983R includes output overvoltage protection (OVP). If the voltage at FB pin exceeds $V_{FB(OVP)}$, the AP3983R immediately shuts down and keeps the internal circuitry enabled to discharge the V_{CC} capacitor to the UVLO turn-off threshold. After that, the device returns to the start state and a start-up sequence ensues.

OTP

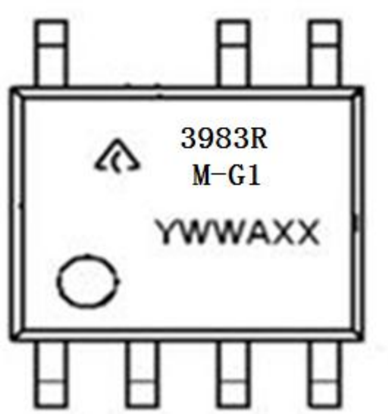
If the junction temperature reaches the threshold of +160°C, the AP3983R shuts down immediately. Before V_{CC} voltage decreases to UVLO, if the junction temperature decreases to +120°C, the AP3983R can recover to normal operation. If not, the power system enters restart Hiccup mode until the junction temperature decreases below +120°C.

Ordering Information



Product	Package	Temperature Range	Cable Compensation Voltage	Part Number	Marking ID	Packing
AP3983R	SO-7	-40 to +85°C	8%	AP3983RMTR-G1	3983RM-G1	4,000/Tape & Reel

Marking Information

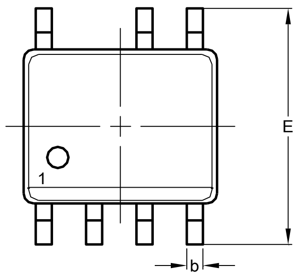


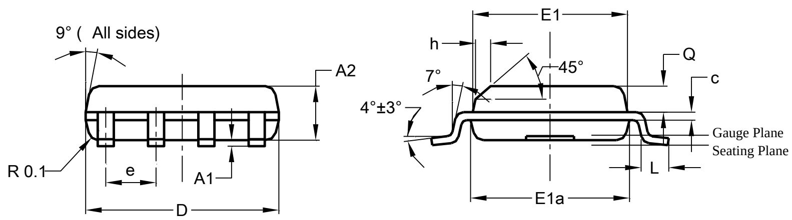
First and Second Lines: Logo and Marking ID
Third Line: Date Code
Y: Year
WW: Work Week of Molding
A: Assembly House Code
XX: 7th and 8th Digits of Batch No

Package Outline Dimensions (All dimensions in mm. (inch).)

Please see http://www.diodes.com/package-outlines.html for the latest version.

SO-7



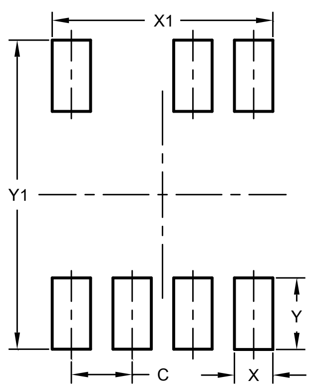


SO-7			
Dim	**Min**	**Max**	**Typ**
A2	1.40	1.50	1.45
A1	0.10	0.20	0.15
b	0.30	0.50	0.40
c	0.15	0.25	0.20
D	4.85	4.95	4.90
E	5.90	6.10	6.00
E1	3.80	3.90	3.85
E1a	3.85	3.95	3.90
e	-	-	1.27
h	-	-	0.35
L	0.62	0.82	0.72
Q	0.60	0.70	0.65
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

SO-7



Dimensions	Value (in mm)
C	1.270
X	0.802
X1	4.612
Y	1.505
Y1	6.500