

30V N+N-Channel Enhancement Mode MOSFET

Description

The AP40H03DF2 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS}=30V$ $I_D=40A$

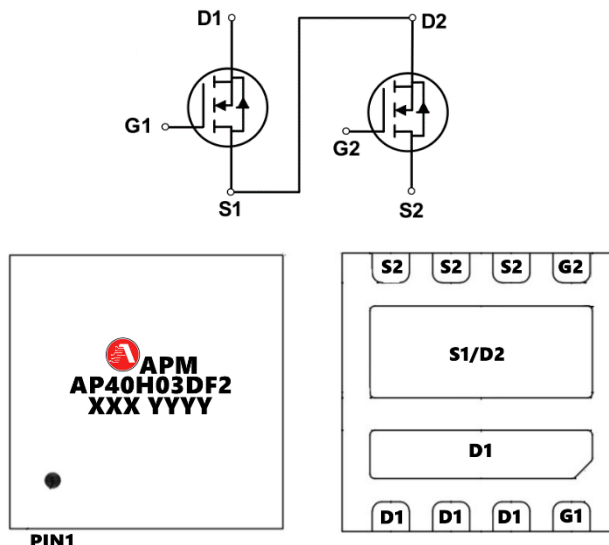
$R_{DS(ON)} < 10m\Omega$ @ $V_{GS}=10V$ (Type: 7.8m Ω)

Application

Battery protection

Load switch

Uninterruptible power supply

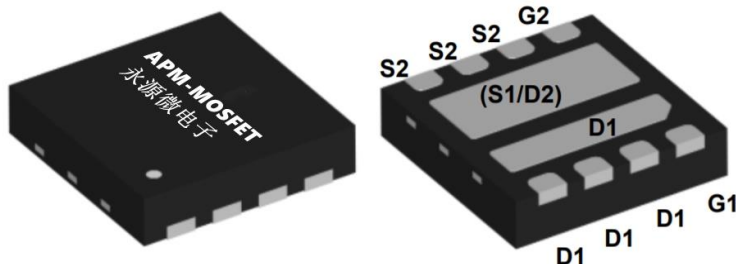


PIN1

DFN3X3B

Top View

Bottom View



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP40H03DF2	DFN3*3B-8L	AP40N03DF2 XXXX YYYY	5000

Absolute Maximum Ratings ($T_C=25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V^1$	40	A
$I_D@T_C=100^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V^1$	23	A
IDM	Pulsed Drain Current ²	120	A
$P_D@T_C=25^{\circ}C$	Total Power Dissipation	137.5	W
TSTG	Storage Temperature Range	-55 to 150	$^{\circ}C$
T_J	Operating Junction Temperature Range	-55 to 150	$^{\circ}C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	85	$^{\circ}C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	4	$^{\circ}C/W$

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Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	30	33	---	V
VGS(th)	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.2	1.6	2.5	V
RDS(ON)	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=30A$	---	7.8	10	mΩ
		$V_{GS}=4.5V, I_D=15A$	---	11	18	
IDSS	Drain-Source Leakage Current	$V_{DS}=24V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	uA
		$V_{DS}=24V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	5	
IGSS	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
gfs	Forward Transconductance	$V_{DS}=5V, I_D=30A$	---	34	---	S
R _g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	1.8	---	Ω
Q _g	Total Gate Charge (4.5V)	$V_{DS}=15V, V_{GS}=4.5V, I_D=15A$	---	9.8	---	nC
Q _{gs}	Gate-Source Charge		---	4.2	---	
Q _{gd}	Gate-Drain Charge		---	3.6	---	
Td(on)	Turn-On Delay Time	$V_{DD}=15V, V_{GS}=10V, R_G=3.3\Omega, I_D=15A$	---	4	---	ns
T _r	Rise Time		---	8	---	
Td(off)	Turn-Off Delay Time		---	31	---	
T _f	Fall Time		---	4	---	
C _{iss}	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1\text{MHz}$	---	940	---	pF
C _{oss}	Output Capacitance		---	131	---	
C _{rss}	Reverse Transfer Capacitance		---	109	---	
I _S	Continuous Source Current ^{1,5}	$V_G=V_D=0V, \text{Force Current}$	---	---	43	A
ISM	Pulsed Source Current ^{2,5}		---	---	112	A
VSD	Diode Forward Voltage ²	$V_{GS}=0V, I_S=1A, T_J=25^\circ\text{C}$	---	---	1	V
t _{rr}	Reverse Recovery Time	$I_F=30A, dI/dt=100A/\mu s, T_J=25^\circ\text{C}$	---	8.5	---	nS
Q _{rr}	Reverse Recovery Charge		---	2.2	---	nC

Note :

- 1、The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3、The EAS data shows Max. rating . The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.1\text{Mh}, I_{AS}=28A$
- 4、The power dissipation is limited by 175°C junction temperature
- 5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics

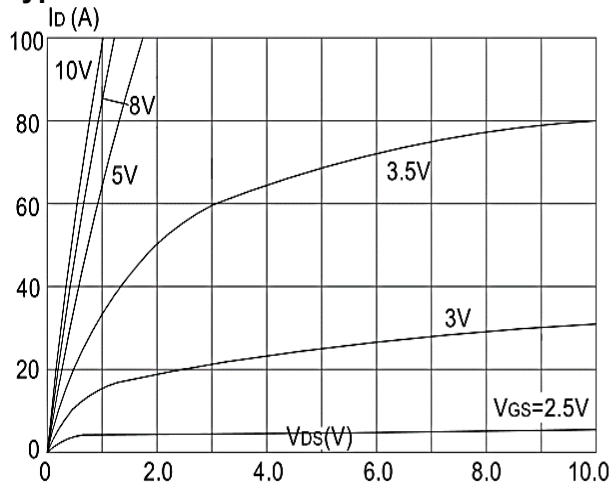


Figure 1: Output Characteristics

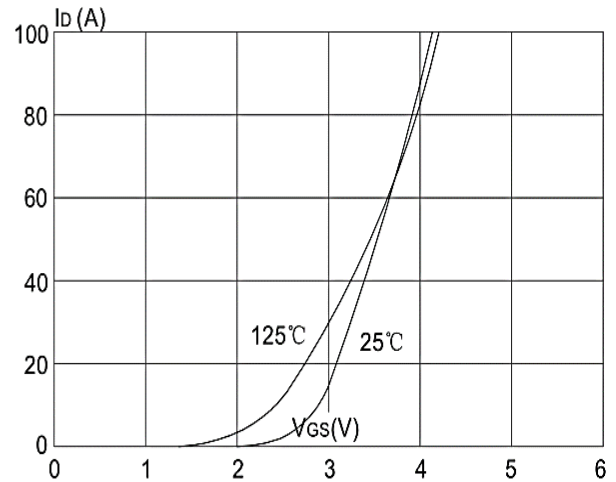


Figure 2: Typical Transfer Characteristics

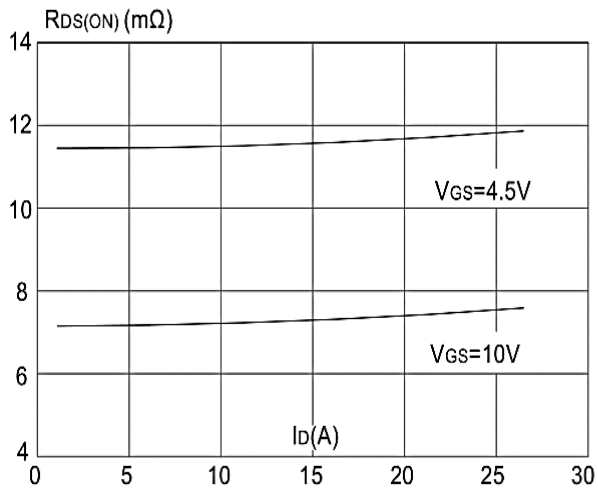


Figure 3: On-resistance vs. Drain Current

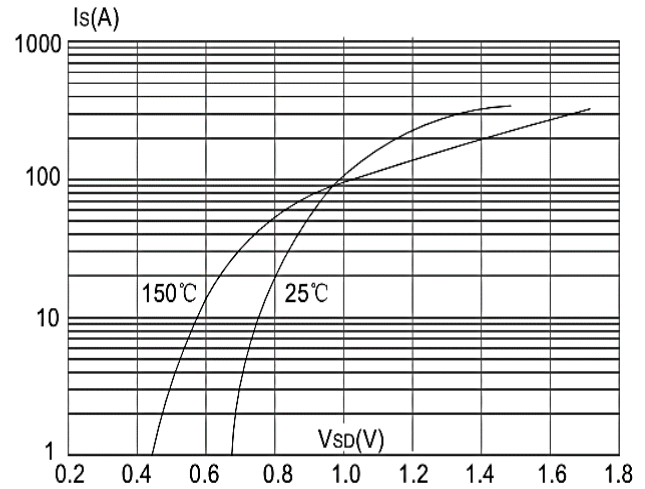


Figure 4: Body Diode Characteristics

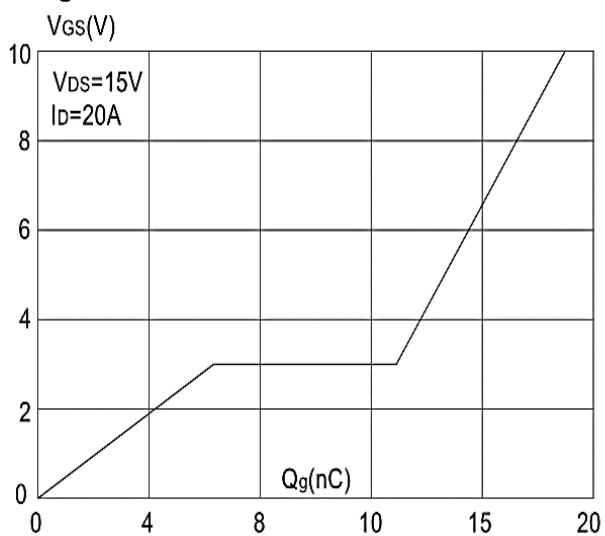


Figure 5: Gate Charge Characteristics

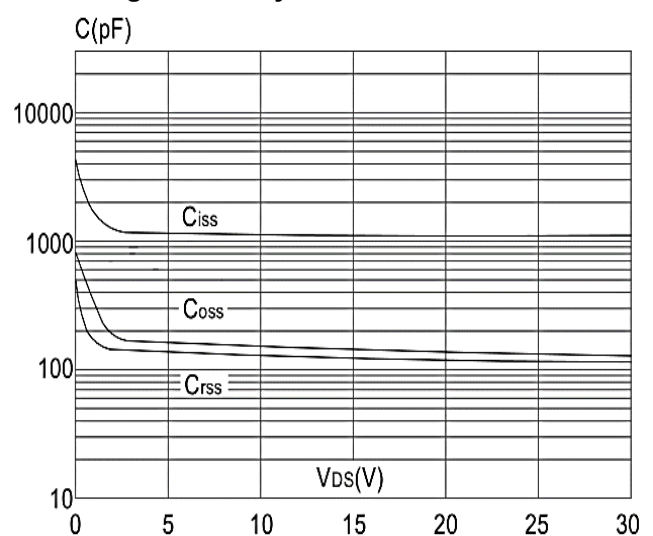


Figure 6: Capacitance Characteristics

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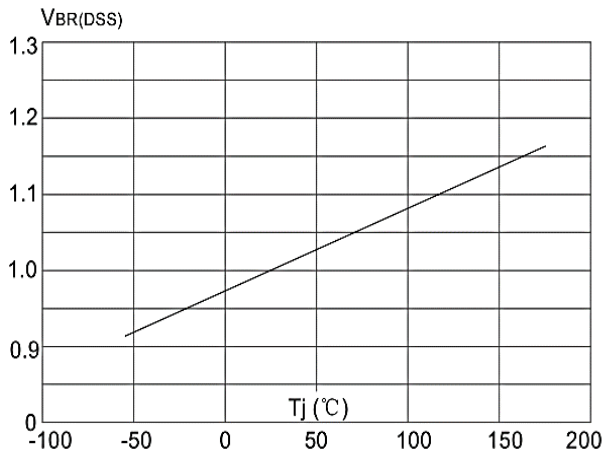


Figure 7: Normalized Breakdown Voltage vs Junction Temperature

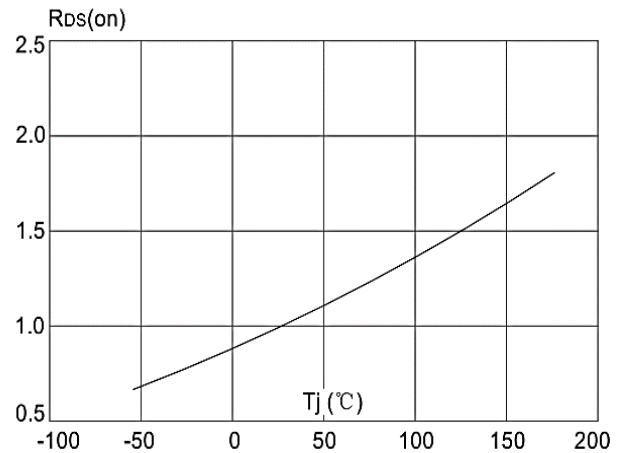


Figure 8: Normalized on Resistance vs. Junction Temperature

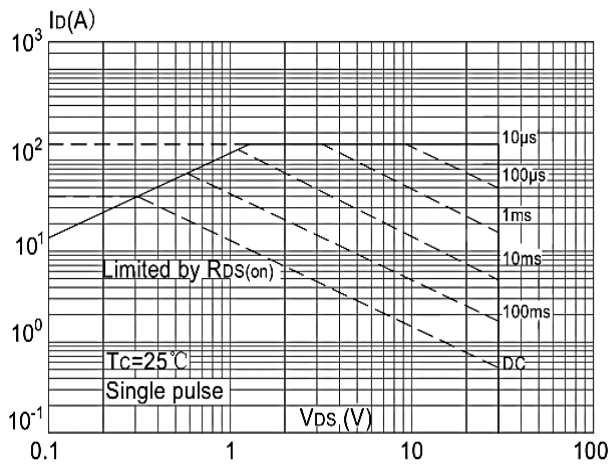


Figure 9: Maximum Safe Operating Area Temperature

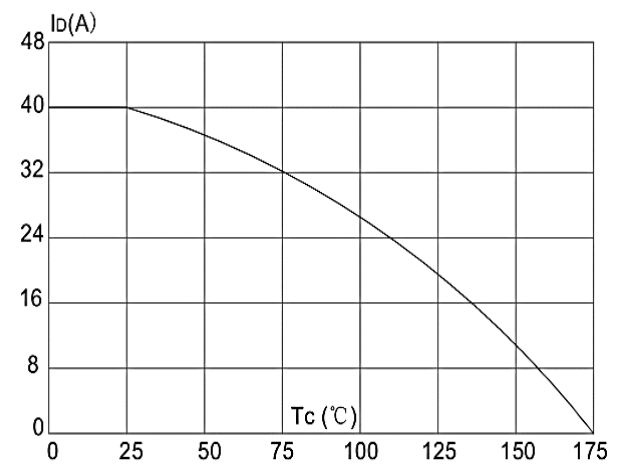


Figure 10: Maximum Continuous Drain Current vs. Ambient

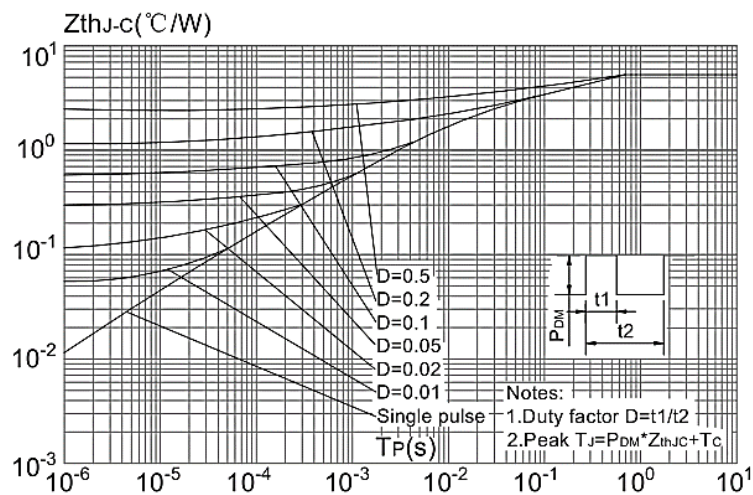
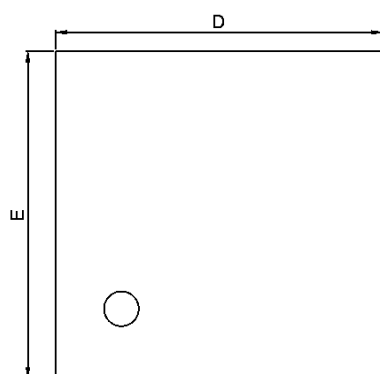
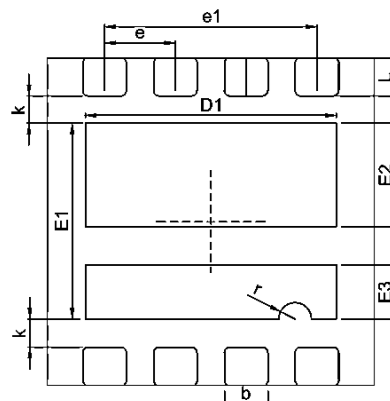


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambien

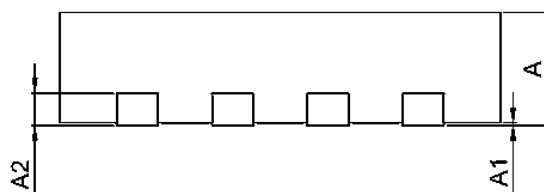
Package Mechanical Data-DFN3*3B-8L Double



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Symbol	Common(mm)		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.35	0.40	0.40
A2	0.203BSC		
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D1	2.25	2.30	2.35
E2	0.09	0.95	1.00
E3	0.45	0.50	0.55
e	0.65BSC		
e1	1.95 BSC		
K	0.20	0.25	0.30
L	0.30	0.35	0.40
r	0.15REF		

30V N+N-Channel Enhancement Mode MOSFET**Attention**

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Edition	Date	Change
REV1.0	2024/1/31	Initial release

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