



**Advanced Power
Electronics Corp.**

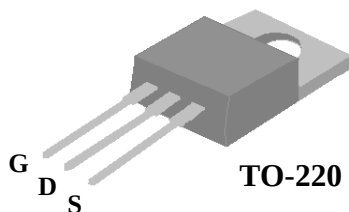
AP40N03GP-HF

Halogen-Free Product

N-CHANNEL ENHANCEMENT MODE

POWER MOSFET

- ▼ Low Gate Charge
- ▼ Simple Drive Requirement
- ▼ Fast Switching Characteristic
- ▼ RoHS Compliant & Halogen-Free

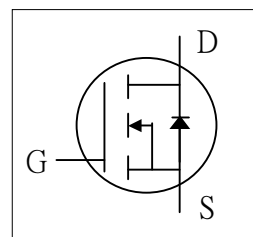


BV_{DSS}	30V
$R_{DS(ON)}$	17m Ω
I_D	40A

Description

AP40N03 series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The TO-220 package is widely preferred for all commercial-industrial through hole applications. The low thermal resistance and low package cost contribute to the worldwide popular package.



Absolute Maximum Ratings@ $T_J=25^{\circ}\text{C}$ (unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	+20	V
$I_D@T_C=25^{\circ}\text{C}$	Drain Current, V_{GS} @ 10V	40	A
$I_D@T_C=100^{\circ}\text{C}$	Drain Current, V_{GS} @ 10V	30	A
I_{DM}	Pulsed Drain Current ¹	169	A
$P_D@T_C=25^{\circ}\text{C}$	Total Power Dissipation	50	W
	Linear Derating Factor	0.4	W/ $^{\circ}\text{C}$
T_{STG}	Storage Temperature Range	-55 to 150	$^{\circ}\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^{\circ}\text{C}$

Thermal Data

Symbol	Parameter	Value	Unit
Rthj-c	Maximum Thermal Resistance, Junction-case	2.5	$^{\circ}\text{C}/\text{W}$
Rthj-a	Maximum Thermal Resistance, Junction-ambient	62	$^{\circ}\text{C}/\text{W}$



AP40N03GP-HF

Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	30	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =20A	-	14	17	mΩ
		V _{GS} =4.5V, I _D =16A	-	20	23	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	1	-	3	V
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =20A	-	26	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =30V, V _{GS} =0V	-	-	1	uA
	Drain-Source Leakage Current (T _j =125°C)	V _{DS} =24V, V _{GS} =0V	-	-	250	uA
I _{GSS}	Gate-Source Leakage	V _{GS} = ±20V, V _{DS} =0V	-	-	±100	nA
Q _g	Total Gate Charge	I _D =20A	-	17	-	nC
Q _{gs}	Gate-Source Charge	V _{DS} =24V	-	3	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =5V	-	10	-	nC
t _{d(on)}	Turn-on Delay Time	V _{DS} =15V	-	7.2	-	ns
t _r	Rise Time	I _D =20A	-	60	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =3.3Ω, V _{GS} =10V	-	22.5	-	ns
t _f	Fall Time	R _D =0.75Ω	-	10	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	800	-	pF
C _{oss}	Output Capacitance	V _{DS} =25V	-	380	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	133	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I _S	Continuous Source Current (Body Diode)	V _D =V _G =0V , V _S =1.3V	-	-	40	A
I _{SM}	Pulsed Source Current (Body Diode) ¹		-	-	169	A
V _{SD}	Forward On Voltage ²	T _j =25°C, I _S =40A, V _{GS} =0V	-	-	1.3	V

Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

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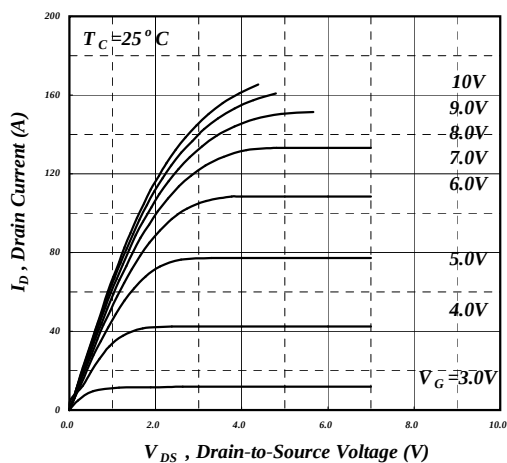


Fig 1. Typical Output Characteristics

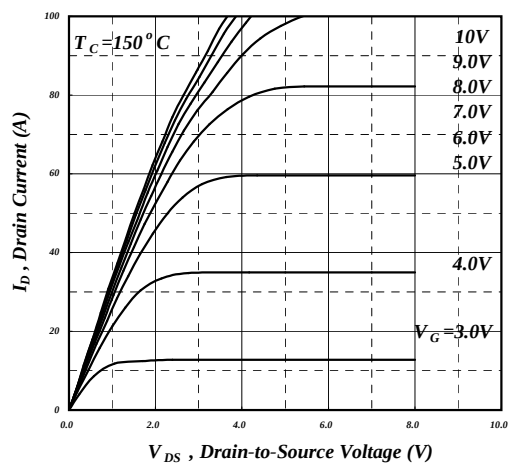


Fig 2. Typical Output Characteristics

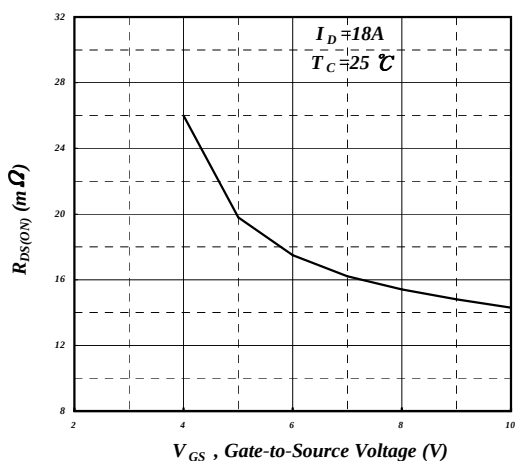


Fig 3. On-Resistance v.s. Gate Voltage

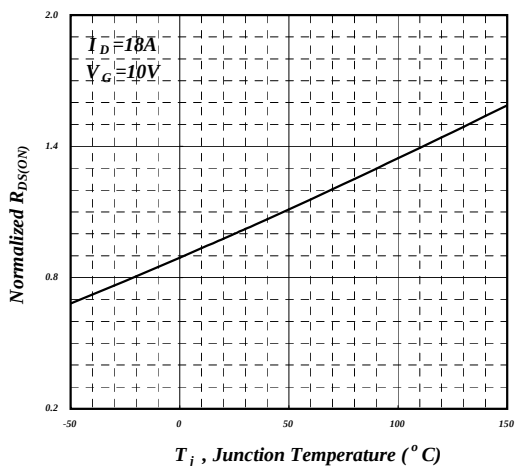


Fig 4. Normalized On-Resistance v.s. Junction Temperature

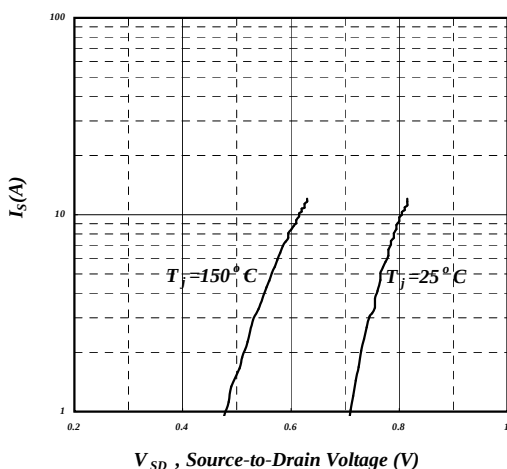


Fig 5. Forward Characteristic of Reverse Diode

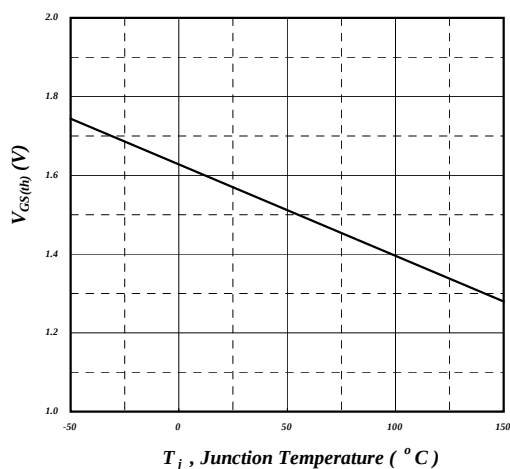


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

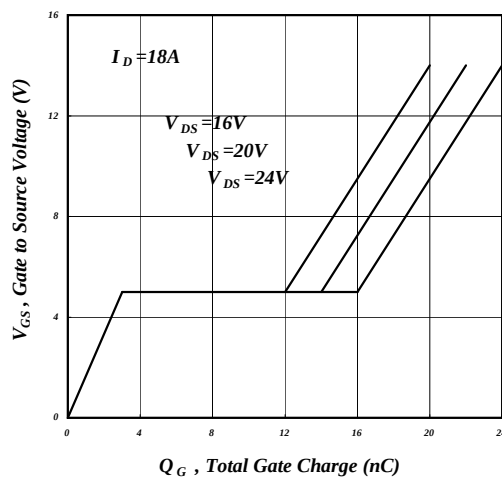


Fig 7. Gate Charge Characteristics

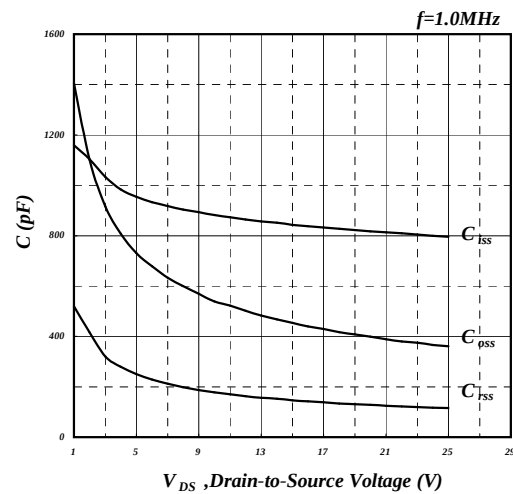


Fig 8. Typical Capacitance Characteristics

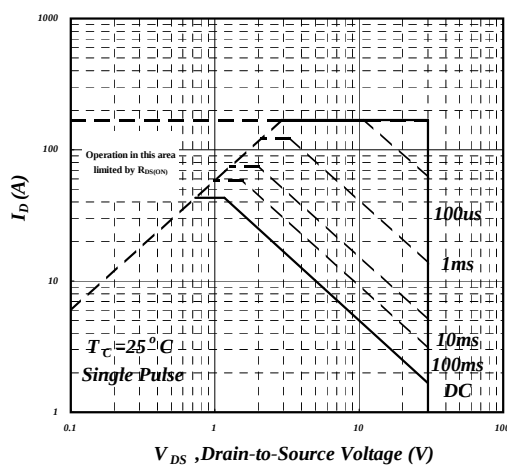


Fig 9. Maximum Safe Operating Area

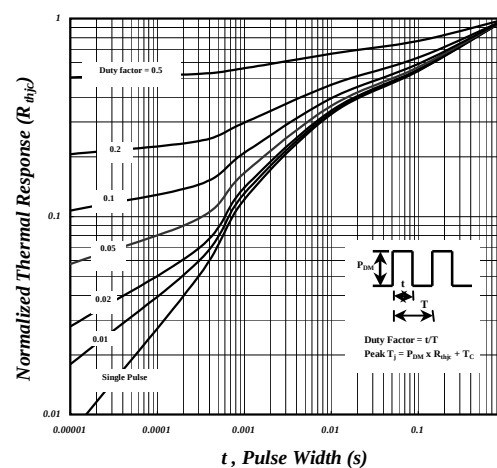


Fig 10. Effective Transient Thermal Impedance

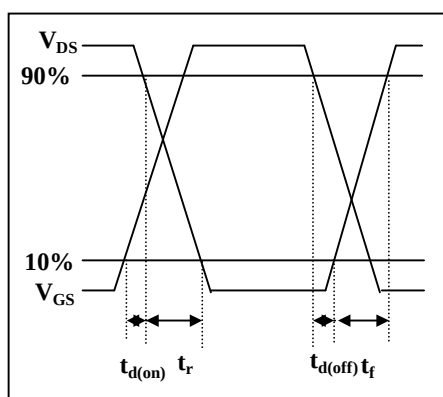


Fig 11. Switching Time Waveform

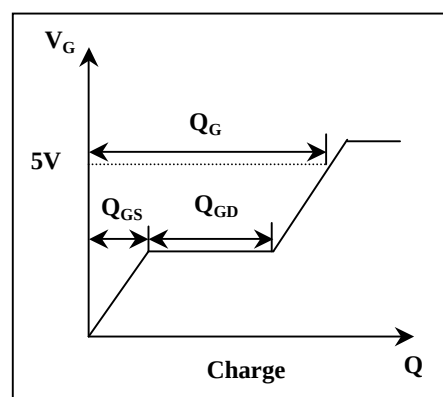


Fig 12. Gate Charge Waveform



MARKING INFORMATION

