AP4202

9ch 100mA LED Driver IC

1. General Description

The AP4202 is a 9 channel LED Driver that supports 2 types of serial interfaces (SCI serial interface or serial F/F cascade interface) to program LED lighting. The built-in 100mA drivable power MOSFET is used to shut off the LED current, and LEDs are controlled by a PWM method in accordance with the LED gradation data that is programmed into the device. Constant current output and Open drain output are selectable by DRSET setting pin. To reduce wirings in the system, voltage on anode side of LEDs can be communized. A maximum of 32 devices can be connected on a single BUS to a common master device; furthermore, each AP4202 retains its own programmed commands allowing continuous autonomous lighting. The internal UVLO function prevents the LEDs from incorrect operations when the supply voltage is 4V or less. An internal over current protection function and a thermal protection function are also integrated.

2. Features

- Power Supply Voltage 8.0V~24.0V
  4.5V~5.5V (connect VIN pin and VDC1 pin)
- Oprating Temperature 0 ~ 70°C
- Absolute Maximum Voltage 30V (VIN, LEDR0~2, LEDG0~2, LEDB0~2)
- 2 Types of Serial Interface for Setting Lighting Data
  - 4-wire SCI interface (maximum communication clock: 5MHz)
  - Serial-F/F cascade (maximum communication clock: 10MHz)
  - Applicable to both 3.3V and 5.0V input signal (output is fixed to 5.0V)
- LED Current maximum 100mA/ch
  - Constant Current Output 50mA/ch
  - Open Drain Output 100mA/ch

(Each channel current is less than the value when 9 channels are set simultaneously)

- LED Gradation 8-bit PWM gradation method (256 gradation)
- Built-in PWM Generator, Adjustable PWM Period
- Simultaneous lighting-off function (SCI interface)
- Protection Function
  - Under voltage lock our (UVLO)
  - Over current protection (timer latch recovery type)
  - Thermal shutdown (automatic recovery)
- Package 30-pin VSOP
- Application A LED loading machine for the decoration

3. Table of Contents

4. Block Diagram and Functions

■ Block Diagram

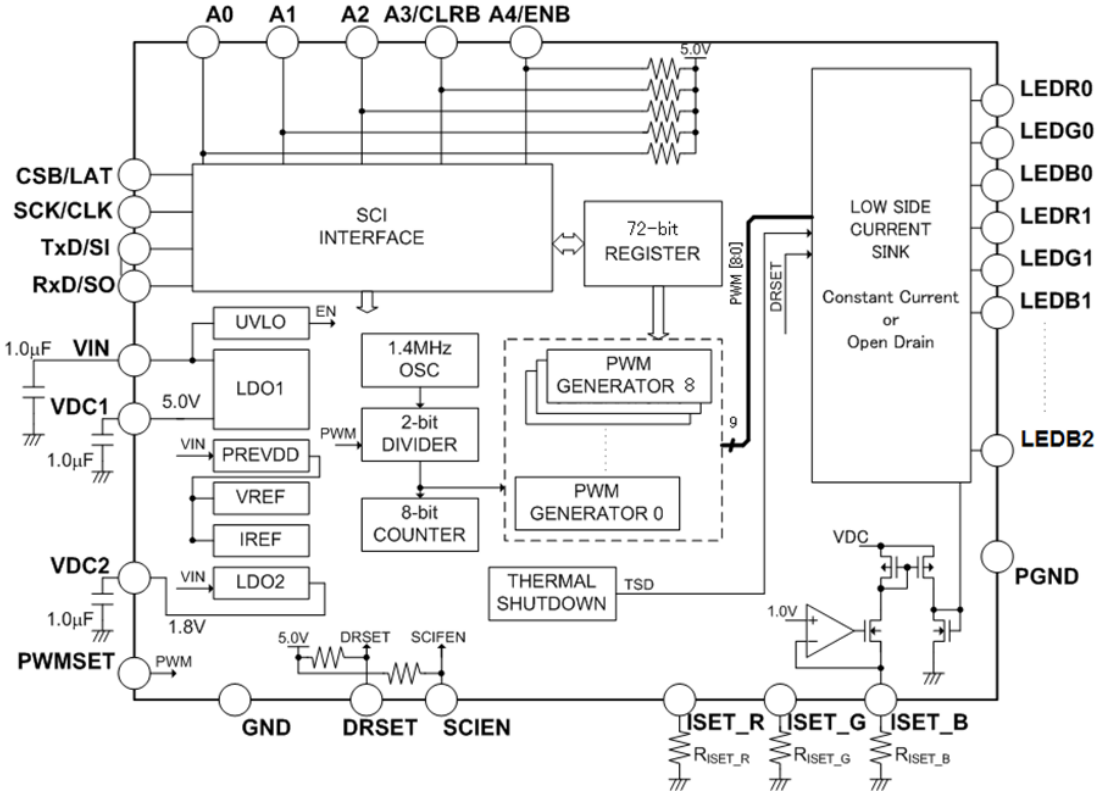


Figure 1.Block Diagram

■ Function

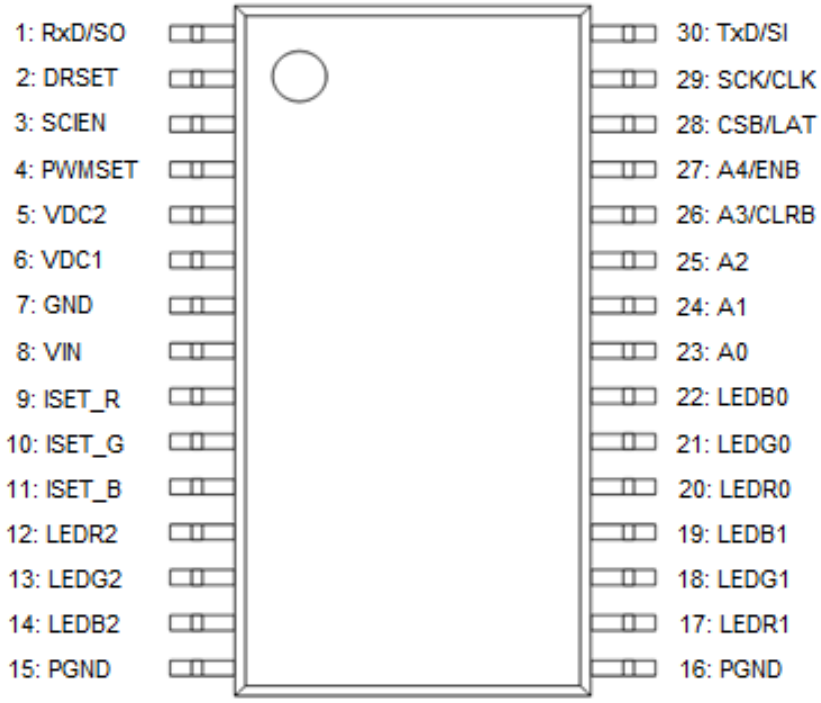
No	Block	Function
1	SCI INTERFACE	In case of SCI: hold the setting data of the PWM gradation. In case of serial F/F: hold the PWM gradation data.
2	CONTROL LOGIC	Detect SCI instruction, control the operation mode.
3	“72-bit” REGISTER	Hold the 8-bit PWM gradation data of LEDR0~2, LEDG0~2 and LEDB0~2.
4	PWM	Compare PWM gradation with counter and generate PWM wave.
5	1.4MHz OSC	Generate 1.4MHz clock.
6	“2-bit” DIVIDER	Divide 1.4MHz clcok to 256 gradation clock.
7	“8-bit” COUNTER	Count with the 256 gradation clock within PWM period.
8	UVLO	Generate reset signal for preventing unstable operating when input power voltage
9	LDO1	Generate an internal 5 voltage. It can supply less than 30mA for driving external
10	LDO2	Generate an internal 1.8 voltage. Driving external circuit is forbidden.
11	VREF	Generate a reference voltage.
12	IREF	Generate a reference current.
13	POR	Generate reset signal at power start up.
14	LOW SIDE CURRENT SINK	LED output driver which can set to current source or open drain output. Over current protection circuit is built in.
15	THERMAL SHUTDOWN	Shut down the LED current and set the VDC1,VDC2 pins to 0 voltage when internal temperature is more than setting value.

5. Ordering Guide

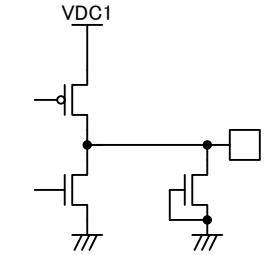
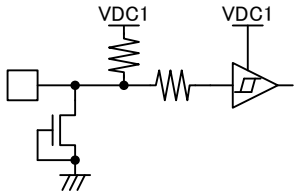
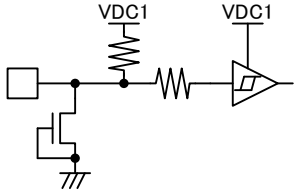
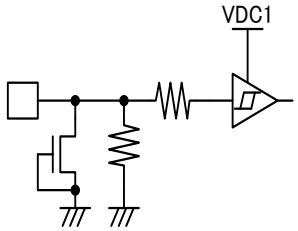
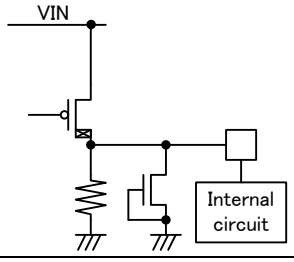
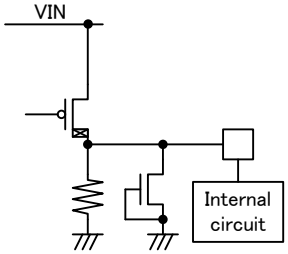
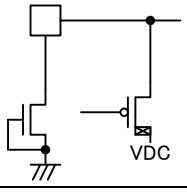
AP4202	0°C～70°C	30-pin VSOP

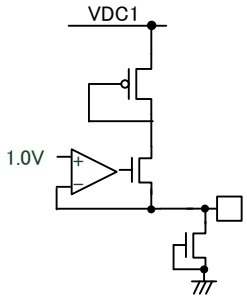
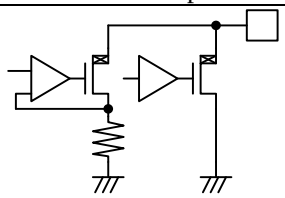
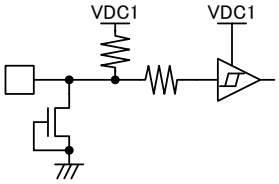
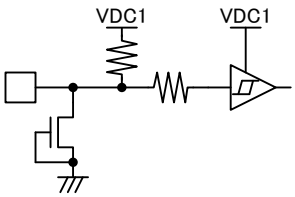
6. Pin Configurations and Functions

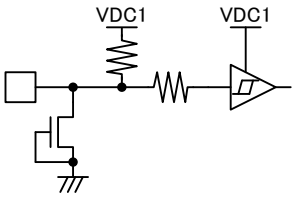
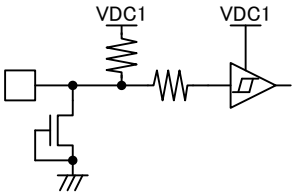
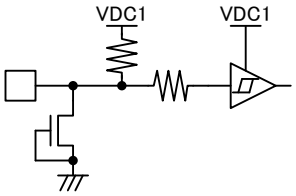
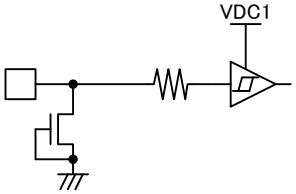
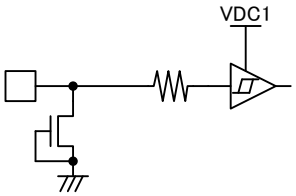
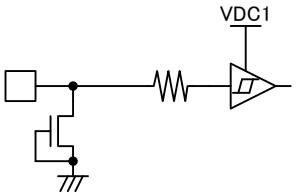
■ **Pin Layout**



■ **Function**

No.	Name	Equivalent circuit	Explanation
1	RxD/SO		Data signal output pin for SCI. To output reading data. Outputs Hi-Z except when data is output. SO output pin for serial F/F. To output data signal of shift register. Output from F/F which determine LEDR2 lighting data.
2	DRSET		Switching pin which can switch to driver output current source or open drain (100kohm pull up) Connect to GND or set to open. If connect to GND, it can work as open drain mode.
3	SCIEN		Enable pin for serial interface. (100kohm pull up) Connect to GND or set to open. If connect to GND, it can work as serial F/F control mode. If open this pin, it can work as SCI control mode.
4	PWMSET		PWM period setting pin. (100kohm pull down) Connect to VDC1 pin or set to open. If connect to GND (or open), PWM gradation period= low speed 546µs(typ.) If connect to VDC1 pin, PWM gradation period= high speed 364µs(typ.)
5	VDC2		Internal 1.8V LDO output pin. Drive external circuit is prohibited. Connect a 1.0µF capacitor between the VDC2 pin and GND.
6	VDC1		Internal 5V LDO output pin. External current capability is 30mA maximum. Connect a 1.0µF capacitor between the VDC terminal and GND.
7	GND	-	Ground
8	VIN		IC power input pin. Internal 5V LDO's output and 1.8V output. Connect a 1.0µF capacitor between the VDC terminal and GND.

No.	Name	Equivalent circuit	Explanation
9	ISET_R		Current setting pin for LEDR0~2. Connect an external resistor between this pin and GND.
10	ISET_G	Same as 9-pin	The pin which set the current of LEDG0~2. (same as 9 pin)
11	ISET_B	Same as 9-pin	The pin which set the current of LEDB0~2. (same as 9 pin)
12	LEDR2		R2 pin (connect to LED cathode). Current source/open drain output. Control the internal MONFET to drive LED with lighting setting.
13	LEDG2	Same as 12-pin	G2 pin (connect to LED cathode). Current source/open drain output. Control the internal MONFET to drive LED with lighting setting.
14	LEDB2	Same as 12-pin	B2 pin (connect to LED cathode). Current source/open drain output. Control the internal MONFET to drive LED with lighting setting.
15	PGND	-	Ground pin for LED current.
16	PGND	-	Ground pin for LED current.
17	LEDR1	Same as 12-pin	R1 pin (connect to LED cathode).Current source/open drain output. Control the internal MONFET to drive LED with lighting setting.
18	LEDG1	Same as 12-pin	G1 pin (connect to LED cathode).Current source/open drain output. Control the internal MONFET to drive LED with lighting setting.
19	LEDB1	Same as 12-pin	B1 pin (connect to LED cathode).Current source/open drain output. Control the internal MONFET to drive LED with lighting setting.
20	LEDR0	Same as 12-pin	R0 pin (connect to LED cathode).Current source/open drain output. Control the internal MONFET to drive LED with lighting setting.
21	LEDG0	Same as 12-pin	G0 pin (connect to LED cathode).Current source/open drain output. Control the internal MONFET to drive LED with lighting setting.
22	LEDB0	Same as 12-pin	B0 pin (connect to LED cathode).Current source/open drain output. Control the internal MONFET to drive LED with lighting setting.
23	A0		IC address input pin 0 (Built in 100kΩ pull up resistor) Configure by connecting to GND or OPEN.
24	A1		IC address input pin 1 (Built in 100kΩ pull up resistor) Configure by connecting to GND or OPEN.

No.	Name	Equivalent circuit	Explanation
25	A2		IC address input pin 2 (Built in 100kΩ pull up resistor) Configure by connecting to GND or OPEN.
26	A3/CLRB		IC address input pin 3 (built in 100kohm pull-up resistor). Configure by connecting to GND or open. CLRB input pin used for serial F/F. Data clear pin used for shift register.
27	A4/ENB		IC address input pin 4 (built in 100kohm pull-up resistor). Configure by connecting to GND or open. ENB input pin used for serial F/F. Control the shift resister data which reflect to PWM data or not.
28	CSB/LAT		Strobe signal input pin for SCI. Respective orders are accepted when the CSB terminal goes "L" level. The CSB terminal always needs to be "L" level while commands are entered or data are transferred. If the CSB pin goes "H" level when data are transferred, the commands are disregarded. LAT signal input pin used for serial F/F. Input LAT signal for shift register.
29	SCK/CLK		Clock signal input for SCI. Writing data is entered from the TxD pin at the SCK rising edge, reading data is output to RxD pin at the SCK falling edge. It is not always necessary to supply a clock signal to the SCK pin. CLK signal input pin used for serial F/F. CLK signal for shift register.
30	TxD/SI		Data signal input pin. To input commands, writing data. SI input pin for serial F/F. To input data signal of shift register. Input to F/F which determine LEDB0 lighting data.

Note 1. Handling of unused pins. (complementary): Set all unused pins open when the either interface for LED gradation data is selected. There is no need to connect unused pin to GND. Since No. 28~30 pins are always used, the circuit for unused status is not built-in to these pins. It is necessary to control these pins to not become Hi-Z state while the power is supplied.

Note 2. The PGND pin and the GND pin are not connected internally. Therefore these pins must be connected externally.

Note 3.  symbol means high voltage tolerance MOS, the pin with this MOS can tolerate high voltage.

7. Absolute Maximum Rating

Parameter	Symbol	min	max	Unit
VIN voltage	V_{IN}	-0.3	30	V
LEDR0-2, LEDG0-2, LEDB0-2 voltage	V_{LED}	-0.3	30	V
CSB/LAT, SCK/CLK, TxD/SI, A0-2, A3/CLRB, A4/ENB, RxD/SO, DRSET voltage (Note 7)	-	-0.3	V_{DC1} + 0.3	V
VDC2 Voltage	-	-0.3	1.98	V
PWMSET, VDC1, ISET_R, ISET_G, ISET_B voltage	-	-0.3	5.5	V
Power Dissipation (Note 5, Note 6)	P_D		800	mW
Storage Temperature	T_{STG}	-40	150	°C

Note 4. All voltages are with respect to GND pin (GND, PGND) as zero (reference) voltage.

Note 5. P_D is decreased at the rate of 8mW/°C when Ta≥25°C. (Mounted on 100 mm × 103 mm t=1.0mm double side FR-4 board.)

Note 6. When calculating thermal design, please include the heat generated by the internal regulator along with the LED pins.

- The case of fixed current output:

IC power consumption
= LED pins power consumption (LED current*LED pin voltage) * LED numbers
+Internal LDO power consumption [(VIN-VDC1) * (VDC1 output current+IC consumption (4.5mA))]
+VDC1*IC consumption (4.5mA)

- The case of open drain output:

IC power consumption
= LED pins power consumption (LED current*LED current*LED ON-resistor 9.3ohm)*LED numbers
+Internal LDO power consumption [(VIN-VDC1) * (VDC1 output current+IC consumption(2mA))]
+VDC1*IC consumption (2mA)

Note 7. The maximum value is limited to 5.5V when the VDC1 exceeds 5.2V.

WARING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

8. Recommended Operating Conditions

Parameter	Symbol	min	typ	max	Unit	Conditions
Input Voltage 1	V_{IN1}	8.0	12.0	24.0	V	Not connect VIN pin and VDC1 pin
Input Voltage 2 (Note 8)	V_{IN2}	4.5	5.0	5.5	V	Connect VIN pin and VDC1 pin
Maximum LDO1 output current	I_{DC}	-	-	30	mA	VIN=12V
Maximum LED pin voltage	V_{LEDOFF}	-	-	24.0	V	LED pin= off setting
Operation Temperature	Ta	0	-	70	°C	

Note 8. Input range (VIN pin voltage) = 5.5V~8.0V is prohibited.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

9. Electrical Characteristics

(VIN=12V, GND=PGND=0V, Ta=+25 °C, Capacitor at VIN, VDC1 and VDC2 pins = 1.0µF . DRSET=High (fixed current), RISET_R=RISET_G=RISET_B= 33.3kΩ; Recommend Parts, unless otherwise specified)

Parameter	Symbol	min	typ	max	Unit	Conditions
Power Consumption	I_{DD1}	-	1.2	2.0	mA	DRSET="L" (open drain) PWM duty= 0%
	I_{DD2}	-	1.3	2.0		DRSET="L" (open drain) PWM duty=50%
	I_{DD3}	-	2.0	4.0		DRSET="H" (fixed current) PWM duty= 0%
	I_{DD4}	-	2.5	4.5		DRSET="L" (fixed current) PWM duty= 50%
VIN Reset Voltage	VIN_{RST}	-	3.6	4.2	V	Activated by decreasing VIN from normal state.
VIN Hysteresis Width	VIN_{HYS}	-	0.2	-	V	Hysteresis between VINrst and VIN set voltage (VINset) (VINset>VINrst)
LDO1 Output Voltage	V_{DC1}	4.75	5.0	5.25	V	V_{IN}=12V, I_{DC1}=-30mA (Note 9)
LDO2 Output Voltage	V_{DC2}	-	1.8	-	V	V_{IN}=12V, I_{DC2}=-0mA
LED Current Capability per Channel	I_{LEDO}	-	-	100	mA	DRSET="L" (open drain)
	I_{LEDC}	-	-	50	mA	DRSET= "H" (fixed current)
LED current switching MOS-FET ON resistance	R_{LED}	-	6	9.3	Ω	DRSET="L" (open drain) LED current= +100mA
LED pin Voltage (for all 15 channels)	R_{LED}	1.4	-	(Note 10)	V	DRSET="H" (fixed current) LED current= +50mA R_{ISET}= 20kΩ
		0.5	-	(Note 10)	V	DRSET="H" (fixed current) LED current= +15mA R_{ISET}= 66.7kΩ
LED Current Accuracy 1	I_{LEDC1}	28.05	30.0	31.95	mA	DRSET="H" (fixed current)
LED Current Accuracy 2	I_{LEDC2}	13.95	15.0	16.05	mA	DRSET="H" (fixed current) R_{ISET}= 66.7kΩ
LED Current Mismatch	ΔI_{LED}	-4	-	4	%	DRSET="H" (fixed current) (Note 11)
LED pin off-lead Current	I_{LEAK_LED}		-	1.0	µA	LED pin voltage= 24V
PWM Period Accuracy	T_{PWM}	-10	-	+10	%	All setting value
PWM Setting Range	D_{PWM}	0	-	100	%	All setting value
PWM Setting Error		-	±1	-	LSB	PWMSET="L"
		-	±1	-	LSB	PWMSET="H"
Input High-level Voltage	V_{IH}	2.5	-	5.5	V	
Input Low-level Voltage	V_{IL}	-0.2	-	0.5	V	
Output High-level Voltage	V_{OH}	3.7	-	5.3	V	I_O=-500µA
Output Low-level Voltage	V_{OL}	0	-	0.8	V	I_O=+500µA
Input Leak Current	I_{LI}	-1.0	-	1.0	µA	CSB, SCK, TxD pins
Output Leak Current	I_{LO}	-1.0	-	1.0	µA	

Note 9. I_{DC1}=-30mA means that internal 5V LDO1 (VDC1 pin) can drive external circuit less than 30mA.

Note 10. V_{LED} identifies the voltage range. There is a range that cannot be set even less than absolute maximum voltage (30V) because of the maximum power dissipation. Please refer to "10.8 Protection Functions".

Note 11. $\triangle I_{LED}(\%) = \frac{I_{LEDxxMAX} - I_{LEDxxMIN}}{I_{LEDxxMAX} + I_{LEDxxMIN}} \times 100$

■ SCI Interface (AC timing)

Table 1. SCI Timing

Parameter	Symbol	min	typ	max	Unit	Condition
SCK Period	t_{SCKP}	200	-	-	ns	
SCK Pulse Width	t_{SCKW}	60	-	-	ns	
CSB Set-up Time	t_{CSS}	50	-	-	ns	
CSB Hold Time	t_{CSH}	70	-	-	ns	
Data Set-up Time	t_{DIS}	50	-	-	ns	
Data Hold Time	t_{DIH}	70	-	-	ns	
RxD pin Output Delay Time	t_{PD}	-	-	80	ns	C_L=100pF
		-	-	50	ns	C_L=20pF
CSB High-level Minimum Time	t_{CS}	100	-	-	ns	
RxD pin High-impedance Output Delay Time	t_{OZ}	-	-	250	ns	C_L=100pF
SCK, CSB, TxD Raising Time	t_{CSR}	-	-	t_{SCKW} × 15%	ns	t_{SCKW}<4000ns
		-	-	600	ns	t_{SCKW}≥4000ns
SCK, CSB, TxD Falling Time	t_{CSF}	-	-	t_{SCKW} × 15%	ns	t_{SCKW}<4000ns
		-	-	600	ns	t_{SCKW}≥4000ns

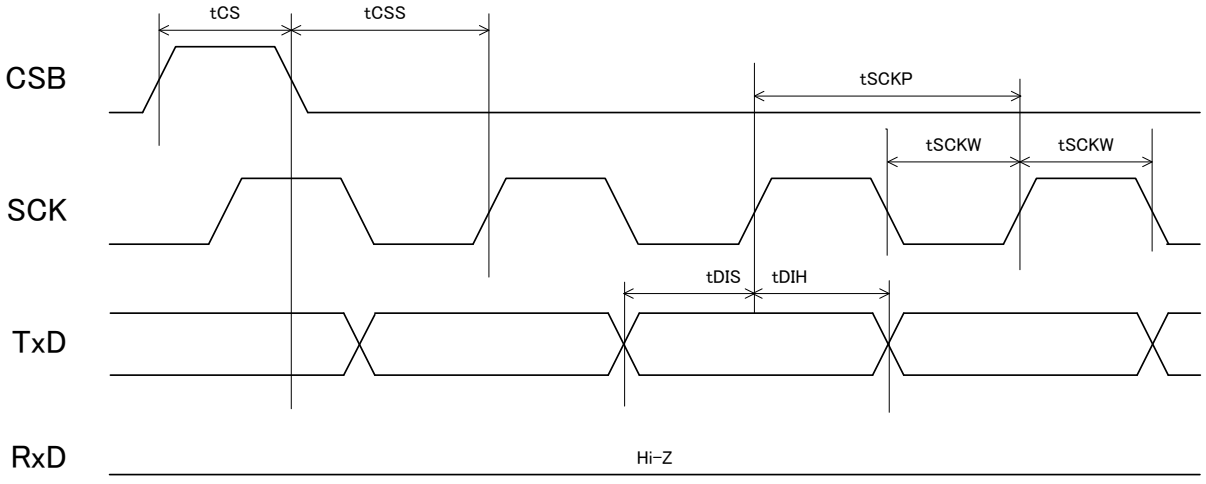


Figure 2. SCI Interface Timing Chart 1

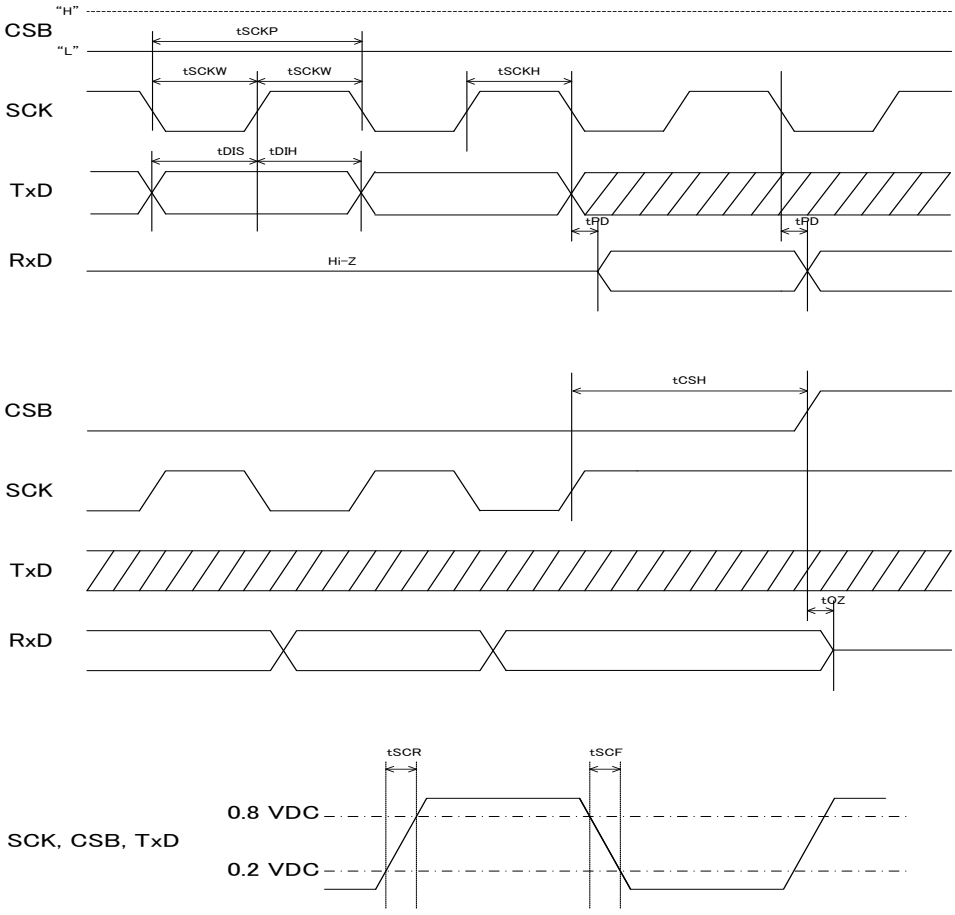


Figure 3. SCI Interface Timing Chart 2

■ Serial F/F Control (AC timing)

Table 2. SCI Serial F/F Control Timing

Parameter	Symbol	min	typ	max	Units	Condition
CLK Period	t_{CLP}	100	-	-	ns	
CLK Pulse Width	t_{CLW}	40	-	-	ns	
Data Set-up Time	t_{DIS}	25	-	-	ns	
Data Hold Time	t_{DIH}	40	-	-	ns	
LAT Pulse Width	t_{LAW}	2	-	-	µs	

The AC timings of CLK (SCK), LAT (CSB), SI (TxD) and SO (RxD) are the same as the SCI interface except data set-up time and data hold time. But the SO (RxD) pin output delay time is the value when C_L=20pF.

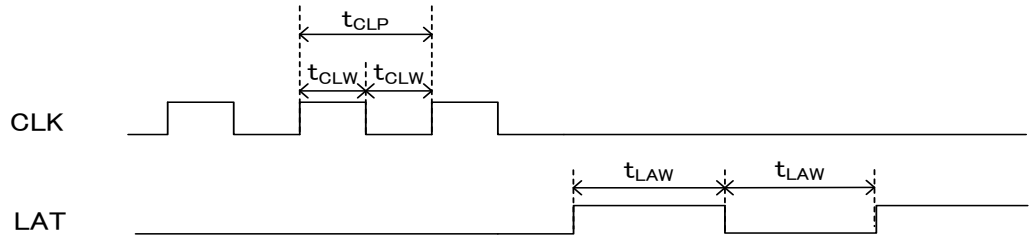


Figure 4. Serial F/F timing

10. Functional Descriptions

10.1. Operation Outline

The AP4202 controls external LED lights using the data that can be configured by two types of interfaces (4-wire SCI control, serial F/F control). Fixed current output or open drain can be selected by the DRSET pin setting. LED lighting is performed by switching the LED current using internal MOSFET controlled by the PWM method. In this case, LED current will be set by an external resistor which is connected to each LED pin when open drain is selected. When fixed current is selected, LED current will be set by an external resistor which is connected to each RGB line, and the all LED pins in the same color are set with the same value.
The AP4202 has an IC address configured by OPEN/SHORT setting of the A0 to A4 pins, and the LED pin addresses that are determined through the SCI interface. By using this IC address configuration, diversification of the LED lighting across multiple AP4202s in a single BUS can be achieved.
By using the OENB pin, all LEDs can be simultaneously turned off regardless of the signal from the SCI interface. However, this is not the lowest power consumption state because the LED gradation data is still being held even while all LEDs are turned off.

Table 3. Description Table for Setting Pins

DRSET pin	DRSET setting result	SCIEN pin	SCIEN setting result
Connect to GND (“L”)	Open drain output	Connect to GND (“L”)	Serial F/F control
OPEN (“H”)	Fixed current output	OPEN (“H”)	SCI control

PWMSET pin	Dimming PWM frequency[Hz] (same as period[μs]) (typ.)
Connect to GND (“L”)	1830Hz (546μs)
Connect to VDC1 (“H”)	2745Hz (364μs)

10.2. SCI Interface Command

Table 4. Command Description (Hereinafter initial “16-bit” data transmission is called command part)

Instruction Content	Function	Description
Instruction	Designate instruction contents by initial “4-bit”	-
“A4~A0”	Assign the IC address	Instructions for a different configured address (set by these pins) are ignored. (“H” display)
“RW”	“1”= Write “0”= Read	-
“ALL”	“1”= All LED pins (all RGB sets) “0”= Base on ch3~ch0 setting	Give the priority to the setting of “ch3~ch0”
“RST”	“1”= LED gradation PWM output stop “0”= Normal operation setting value	Set to “1” only in case of PWM output stopped Stopped in case of 「RW」= 「ALL」= 「RST」 = “1”
“ch3~ch0”	Assign RGB sets in case of ALL= “0”	-

Table 5. LED Line Address

LED line address				Channel (LED line)
ch3	ch2	ch1	ch0	
0	0	0	0	LEDR0, LEDG0, LEDB0
0	0	0	1	LEDR1, LEDG1, LEDB1
0	0	1	0	LEDR2, LEDG2, LEDB2
0	0	1	1	Setting is prohibited
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	

LED line address				Channel (LED line)
ch3	ch2	ch1	ch0	
1	0	0	0	Setting is prohibited
1	0	0	1	LEDR2~LEDR0 write to LEDR pins in order
1	0	1	0	LEDG2~LEDG0 write to LEDG pins in order
1	0	1	1	LEDB2~LEDB0 write to LEDB pins in order
1	1	0	0	LED*2~LED*0 write to LEDR,G,B pins with same data at the same time
1	1	0	1	LED** write to all LED pins with same data
1	1	1	0	Setting is prohibited
1	1	1	1	

Table 6. Command Table

Command	Instruction				IC address					RW	ALL	RST	LED address				Pin
SCL	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	SCK
Normal	1	0	1	0	A4	A3	A2	A1	A0	RW	ALL	RST	ch3	ch2	ch1	ch0	TxD
Unreflected	1	0	1	1													
Lach	0	0	0	0	Do Not Enter												

Note 12. Changing setting of the A4~A0 pins is prohibited when the CSB pin= “L” (during command input).
Note 13.

1. Normal Command: when the CSB pin is set “High” after executing a command, the state of the LED lighting reflects the PWM gradation data configured by the command.
2. Unreflected Command: when the CSB pin is set “High” after executing a command, the state of LED lighting does not reflect the PWM gradation data configured by the command. LED lighting is not changed by executing the command.
3. Latch Command: Latch Command simultaneously executes the LED lighting based on all the PWM gradation data in the IC when the CSB pin is set “High” after executing the Latch command.
4. When the latch command is executed, LEDs that are not set with PWM gradation data are turned off.
5. In case of the latch command, the CSB pin can be set “High” after entering the “4-bit” instruction.
6. When ALL= “0” is set, the PWM gradation data should be set for 1-RGB (=3 LED lines).
   e.g. In the case of ch3~ch0= “0010”, (R2D7~R2D0) (G2D7~G2D0) (B2D7~B2D0) should be set with the same command.
7. When ALL= “0” is set, there is a possibility that the AP4202 becomes shipping test status by setting a one LED line address to the “setting prohibited status” twice continuously. (It is necessary to supply the power again to recover from this shipping test status.)

Table 7. IC Address List

IC Address Data [A4~A0]: Command will be executed to the assigned IC address.			
00000 = Address 0	01000 = Address 8	10000 = Address 16	11000 = Address 24
00001 = Address 1	01001 = Address 9	10001 = Address 17	11001 = Address 25
00010 = Address 2	01010 = Address 10	10010 = Address 18	11010 = Address 26
00011 = Address 3	01011 = Address 11	10011 = Address 19	11011 = Address 27
00100 = Address 4	01100 = Address 12	10100 = Address 20	11100 = Address 28
00101 = Address 5	01101 = Address 13	10101 = Address 21	11101 = Address 29
00110 = Address 6	01110 = Address 14	10110 = Address 22	11110 = Address 30
00111 = Address 7	01111 = Address 15	10111 = Address 23	11111 = Address 31

Note 14. Set address 0~31 by the A4~A0 pin for IC address setting (connect to GND or OPEN).

Table 8. Normal Command Examples

Normal Command	Instruction				IC Address					RW	ALL	RST	LED Line Address				Pin
SCL(times)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	SCK
Case 1	0	0	1	0	A4	A3	A2	A1	A0	1	1	0	-	-	-	-	
Case 2	0	0	1	0	A4	A3	A2	A1	A0	1	0	0	0	0	1	0	
Case 3	0	0	1	0	A4	A3	A2	A1	A0	0	1	0	-	-	-	-	
Case 4	0	0	1	0	A4	A3	A2	A1	A0	0	0	0	0	0	1	0	TxD
Case 5	0	0	1	0	A4	A3	A2	A1	A0	1	1	1	-	-	-	-	
Case 6	0	0	1	0	A4	A3	A2	A1	A0	1	0	0	1	0	0	1	
Case 7	0	0	1	0	A4	A3	A2	A1	A0	1	0	0	1	1	0	0	

Note 15. 'Data' described below represents the PWM gradation data for each individual LED channel. The PWM gradation data is set in hexadecimal for the lighting ratio. "8-bit" data "10(H)" generates a light level of 16/255. (All-0= "00(H)"= turns all LEDs off)

Case 1: Write LED gradation data using an "8-bit" configuration to the IC assigned by an IC address.
In accordance with [ALL] = "1", write data to all the LED lines. In this case, LED line address data are ignored; however, the 4 clock pulses for the LED line addresses are still necessary. Following the initial "16-bit" command, "8-bit" x 9 LED lines = "72-bit" of data input are necessary.

Case 2: Write LED gradation data using an "8-bit" configuration to the IC assigned by an IC address.
In accordance with [ALL] = "0", write data to a specified 3 colors LED line(LEDR2, LEDG2, LEDB2). Following the initial "16-bit" command, "8-bit" x 3 LED lines = "24-bit" of data input are necessary.

Case 3: Read LED gradation data using an "8-bit" configuration from the IC assigned by an IC address. In accordance with [ALL] = "1", read data from all the LED lines. In this case, LED line address data are ignored; however, the 4 clock pulses for the LED line addresses are still necessary. Following the initial "16-bit" command, CLK pulses for "8-bit" x 9 LED lines = "72-bit" are necessary.

Case 4: Read LED gradation data using a "8-bit" configuration from the IC assigned by an IC address. In accordance with [ALL] = "0", read data from a specified 3 colors LED lines (LEDR2, LEDG2, LEDB2). In this case, Following the initial "16-bit" command, CLK pulses for "8-bit" x 3 LED lines = "24-bit" are necessary.

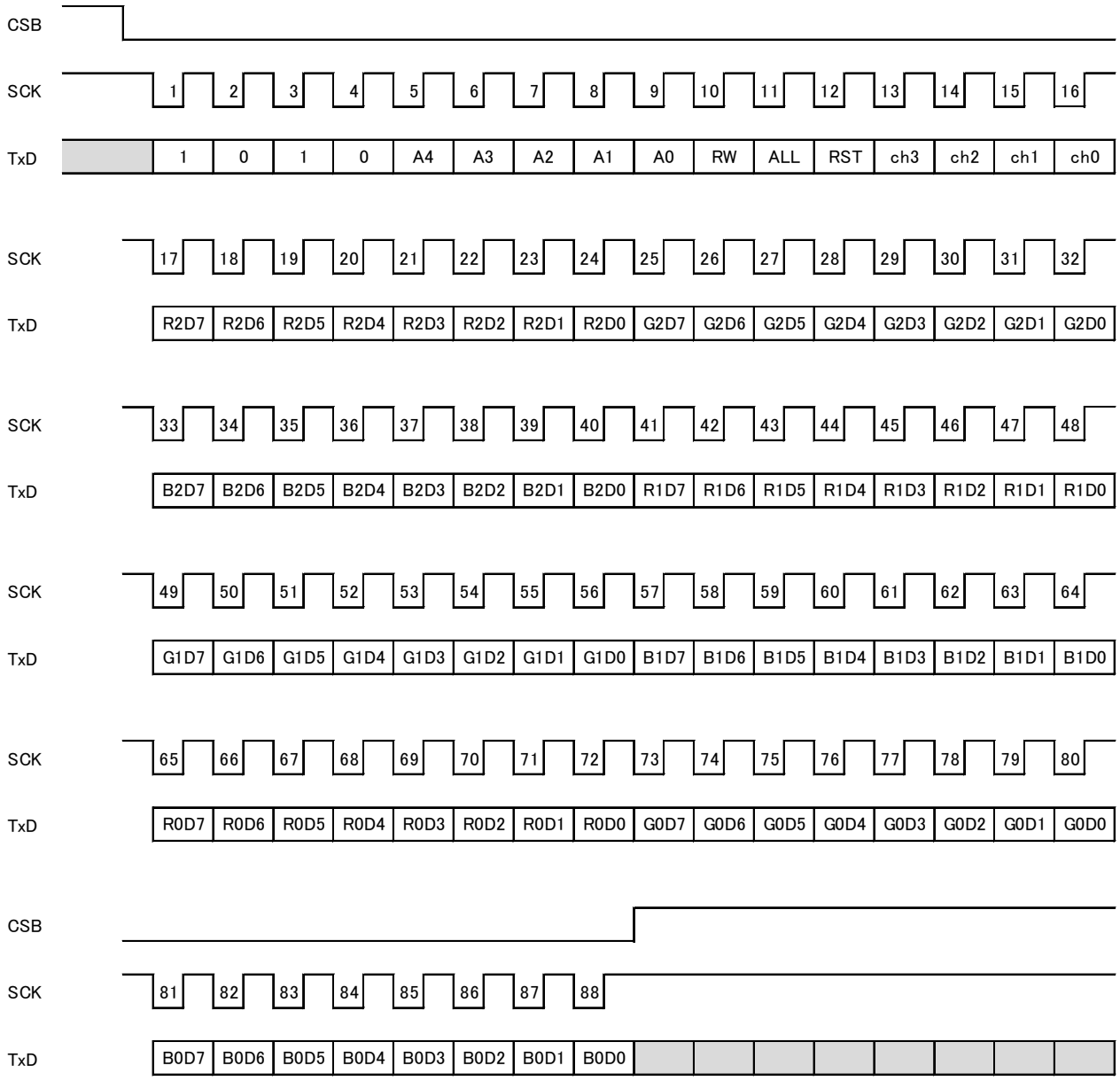
Case 5: This command means [turn off all at once].
In accordance with [RW]=[ALL]=[RST]= "1", turn off LEDs of the IC assigned by an IC address. This command is used to turn off all LED lines, the LED gradation data before turning off will be kept continually. Executing a latch command can relight the LEDs with the same gradation data. This command is valid when the instruction= [normal command], [RW]=[ALL]=[RST]= "1" and command length ≥ "16-bit" (need "16-bit" CLK pulse input). If [RST]= "1" is input when these conditions are not satisfied, [RST] command will be recognized as "0". (This command is used for LED dynamic and scanning drives.)

Case 6: Write LED gradation data by an "8-bit" configuration to an IC assigned by the IC address.
In accordance with [ALL]= "0" and LED line setting (ch3~ch0), only write [R] data to LED lines in the order as shown below.
(R2D7~R2D0) (R1D7~R1D0) • • • (R0D7~R0D0) ［Total "8-bit"×3LED lines = "24-bit" (bit number of data)］

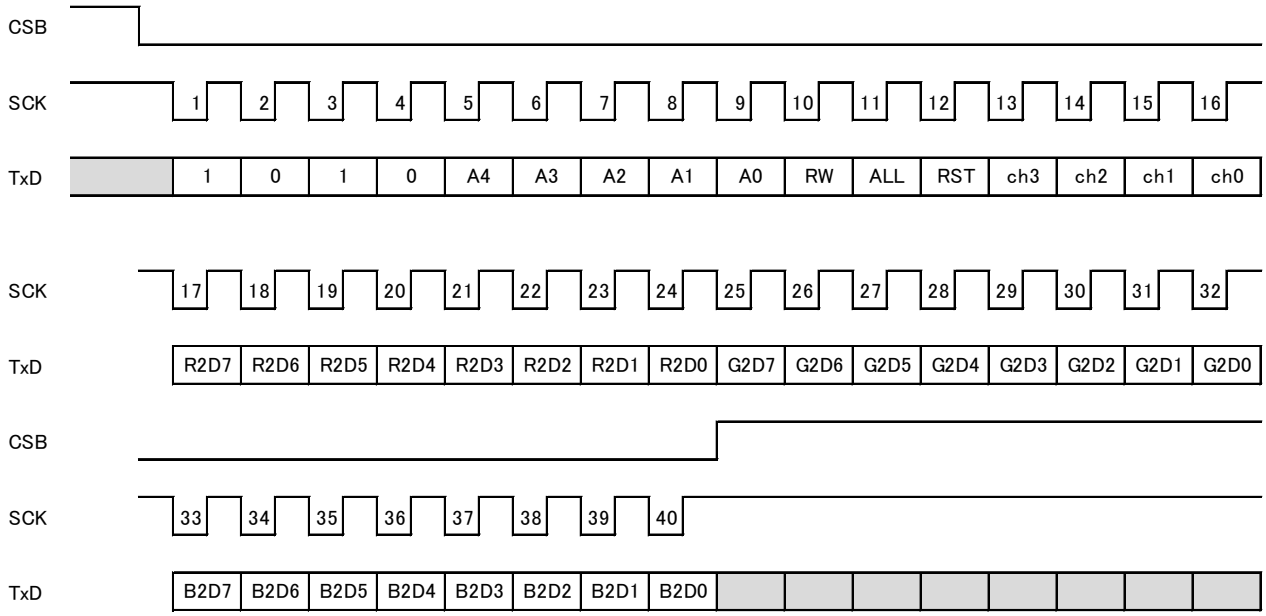
Case 7. Write LED gradation data using an "8-bit" configuration to an IC assigned the IC address.
In accordance with [ALL]= "0" and LED line setting (ch3~ch0), write data to one set of LED lines for three colors in the order as shown below.
(RxD7~RxD0) (GxD7~GxD0) (BxD7~BxD0) [Total "8-bit"×3LED lines = "24-bit" (bit number of data)]. For this setting, the data of one set of written LED lines for three colors is reflected to all LED lines.

・ Timing Diagram

RW= “1”, ALL= “1”, RST= “0”, ch3~ch0= “arbitrary value”(RxD outputs Hi-Z)

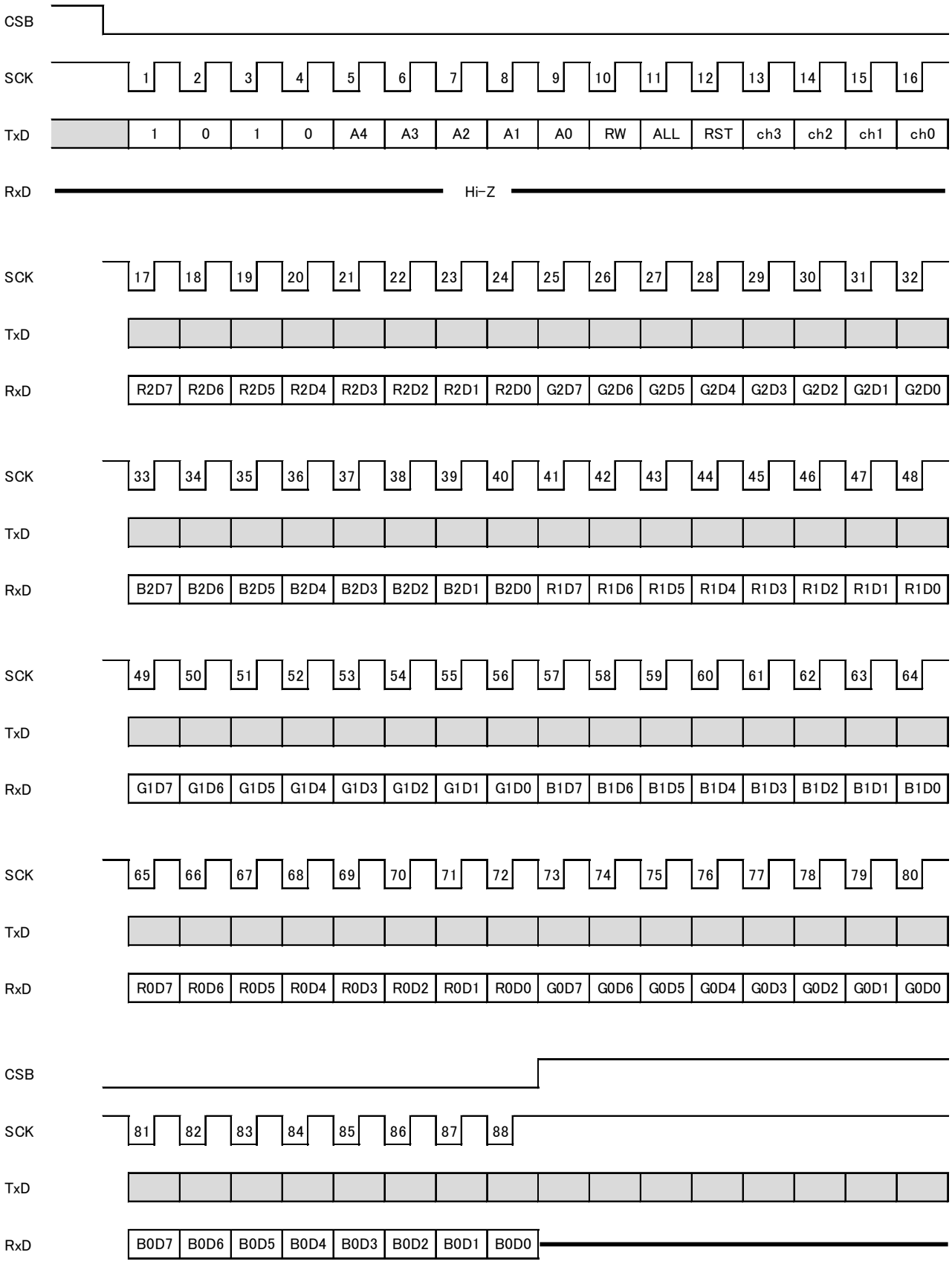


RW= “1”, ALL= “0”, RST= “0”, ch3~ch0= “0010” (RxD outputs Hi-Z)

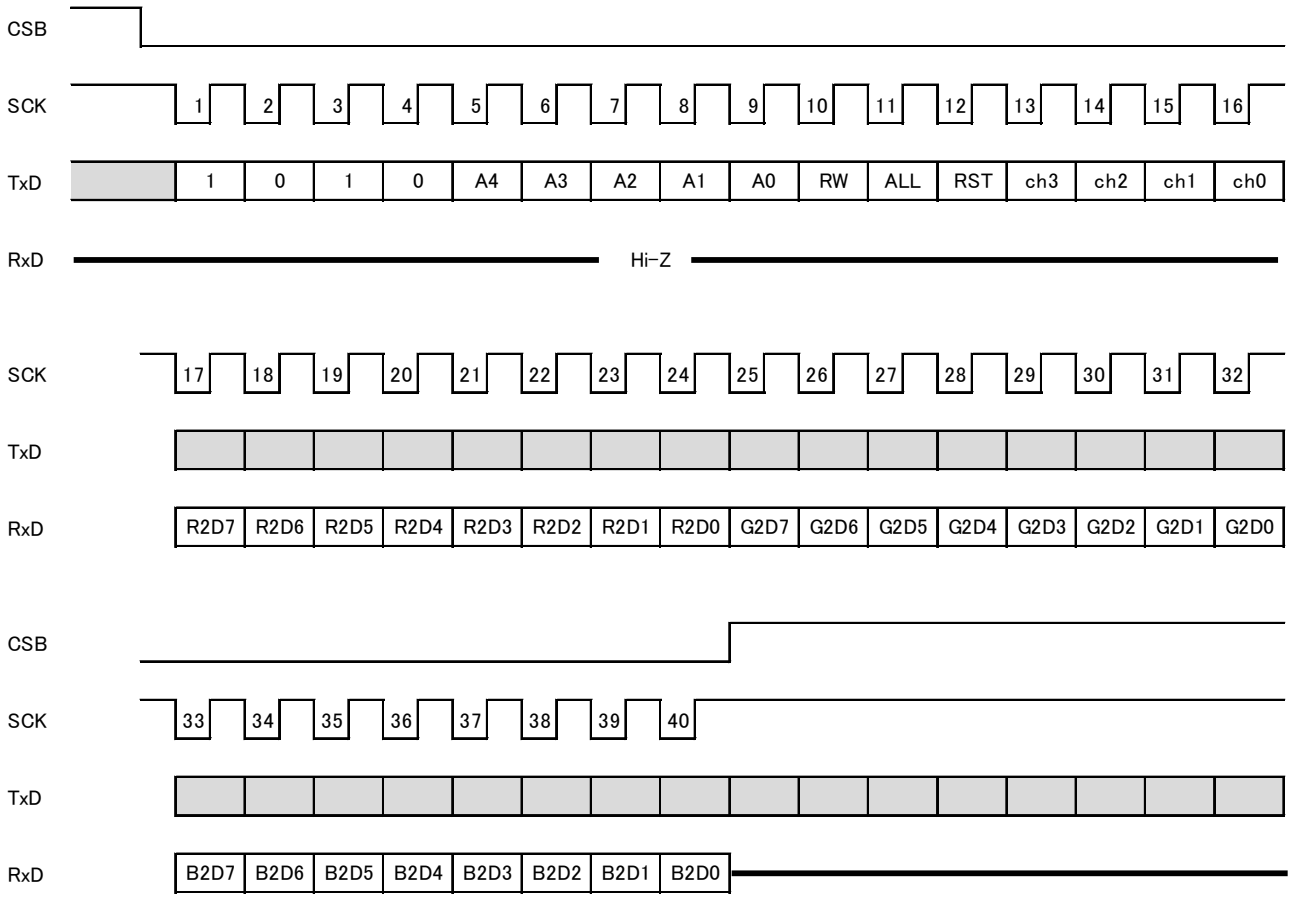


LED line (gradation data): R2、G2、B2
Data write order (MSB-first): R2D7, R2D6, …R2D1, R2D0, G2D7, G2D6, …G2D1, G2D0, B2D7, B2D6, …B2D1, B2D0

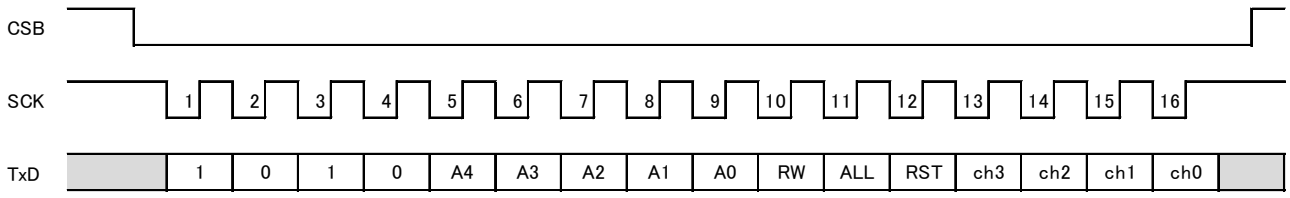
RW= “0”, ALL= “1”, RST= “0”, ch3~ch0= “random” (RxD outputs Hi-Z)



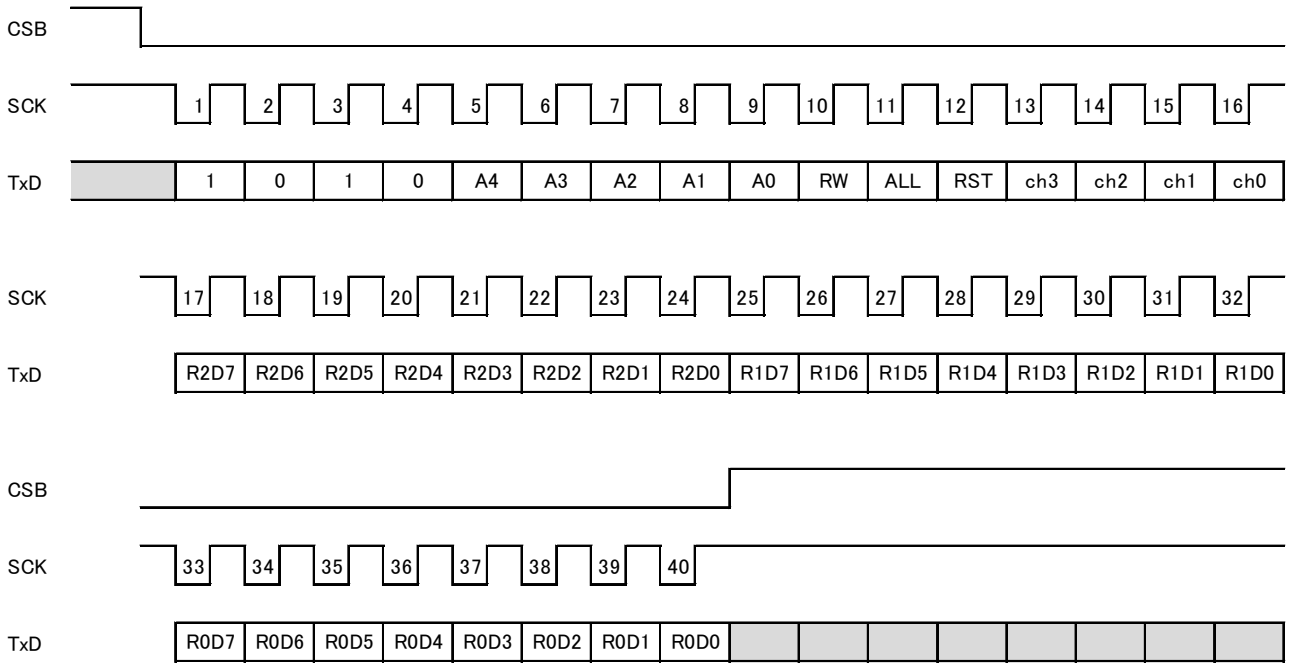
RW= “0”, ALL= “0”, RST= “0”, ch3~ch0= “0010” (RxD outputs Hi-Z)



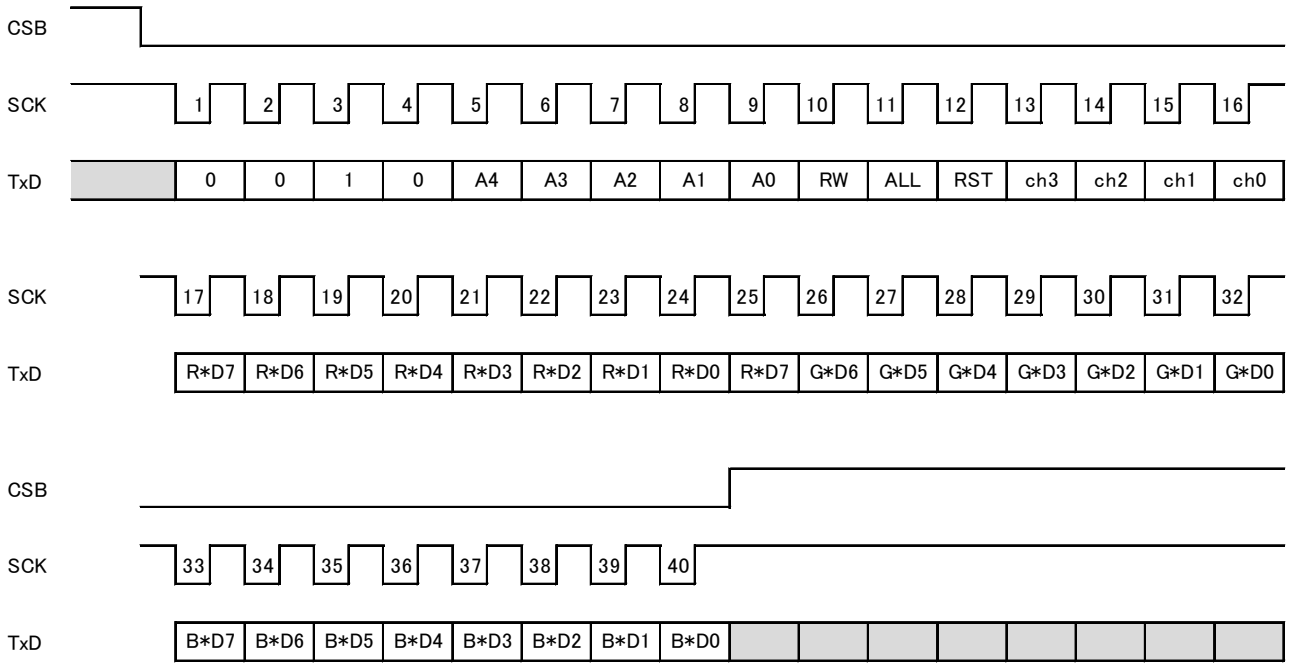
RW= “1”, ALL= “1”, RST= “1”, ch3~ch0= “random” (RxD output Hi-Z)



RW= “1”, ALL= “0”, RST= “0”, ch3~ch0= “1001” (RxD output Hi-Z)



RW= “1”, ALL= “0”, RST= “0”, ch3~ch0= “1100” (RxD output Hi-Z)



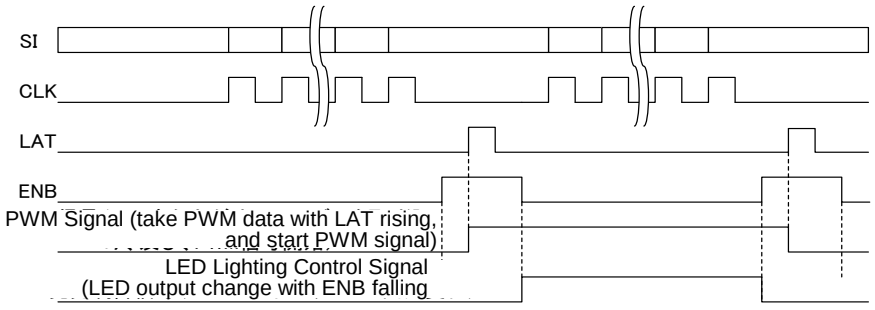
10.3. Serial F/F Cascade Control

Input LED gradation data serially (8 bits x 9ch= 72 bits) and set PWM data from internal shift register to control LEDs. Multiple AP4202s can be used to control LEDs with shift register by connecting the SO output pin to the next IC's SI pin.

Table 9. Serial F/F Cascade Control

Input				Shift register	Latch Data	LED pin
CLRB	CLK	LAT	ENB			
L	×	×	×	L	L	OFF
H	↓	L	H	Data shift (Note 16) SI→ PWM_B0→ PWM_G0→PWM_R0→ PWM_B1→ : : PWM_1R→ PWM_2B→PWM_2G→ PWM_2R→SO	Hold	OFF
H	↓	L	L	Data shift (Note 16) SI→PWM_B0→ PWM_G0→PWM_R0→ PWM_B1→ : : PWM_1R→ PWM_2B→PWM_2G→ PWM_2R→SO	Hold	ON at PWM signal = "1" OFF at PWM signal = "0"
H	L	↓	H	Not shift	Transfer	off
H	L	↓	L	Not shift	Transfer	ON at PWM signal = "1" OFF at PWM signal = "0"
H	×	×	L	—	—	ON at PWM signal = "1" OFF at PWM signal = "0"

Note 16. PWM_Rx, PWM_Gx, PWM_Bx (x=2~0) means shift each channel's PWM gradation data.
(same as CSI control, input with MSB order)
e.g.) PWM_B0: "B0D0→B0D1→B0D2→B0D3→B0D4→B0D5→B0D6→B0D7"
(B0D0 is the LSB gradation data of LEDB0, B0D7 is the MSB gradation data of LEDB0)



The SI input shift data can be taken by many chips with LAT rising.
Output each chip's LED lighting control signal when ENB= "0" (ENB= "1": all channel= "off")

Figure 5. Serial F/F Cascade Control

10.4. LED Current Setting (fixed current output)

LED current can be adjusted from 5mA to 50mA with an external resistor which is connected between the ISET pin and GND. Since the ISET pin is easily affected by a noise, RISET layout should take a shortest connection to avoid unstableness LED current. The ISET_R pin is used to set LEDR0~2 current, the ISET_G pin used to set LEDG0~2 current and the ISET_B pin used to set LEDB0~2 current. An approximate formula of ILED, that is LED current, and RISET resistor, which is connected to the ISET pin, and a relationship table between ILED and RISET are shown below. Please confirm actual values on your board when setting.

$$\mathrm{ILED(mA)} = \frac{1000}{\mathrm{R_{ISET}(k\Omega)}}$$

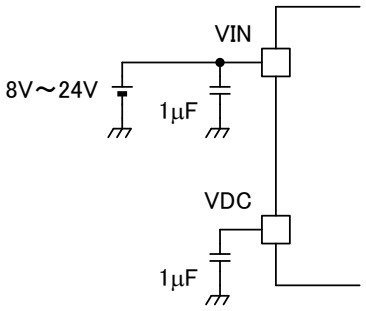
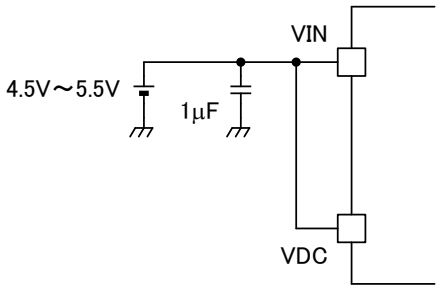
Table 10. Combination of ILED and R_{ISET}

RISET_R (kΩ) RISET_G (kΩ) RISET_B (kΩ)	ILEDRx (mA) ILEDGx (mA) ILEDBx (mA)	RISET_R (kΩ) RISET_G (kΩ) RISET_B (kΩ)	ILEDRx (mA) ILEDGx (mA) ILEDBx (mA)
200.0	5.0	35.7	28.0
166.7	6.0	34.5	29.0
142.9	7.0	33.3	30.0
125.0	8.0	32.3	31.0
111.1	9.0	31.3	32.0
100.0	10.0	30.3	33.0
90.9	11.0	29.4	34.0
83.3	12.0	28.6	35.0
76.9	13.0	27.8	36.0
71.4	14.0	27.0	37.0
66.7	15.0	26.3	38.0
62.5	16.0	25.6	39.0
58.8	17.0	25.0	40.0
55.6	18.0	24.4	41.0
52.6	19.0	23.8	42.0
50.0	20.0	23.3	43.0
47.6	21.0	22.7	44.0
45.5	22.0	22.2	45.0
43.5	23.0	21.7	46.0
41.7	24.0	21.3	47.0
40.0	25.0	20.8	48.0
38.5	26.0	20.4	49.0
37.0	27.0	20.0	50.0

10.5. Input Voltage Range (VIN)

Basically, the input voltage range is 8V~24V. It can be changed to 4.5~5.5V by shorting the VIN pin and the VDC1 pin when 5V power supply is used. In this case, a normal operation cannot be guaranteed with an input that is in the range of 5.5V~8V.

Table 11. Input Voltage Range

Input Voltage Range 1	Input Voltage Range 2
	

10.6. POR Operation (Power on Reset)

The internal POR circuit releases reset state after a specific period of time (t1) when a power supply more than 6V is applied to the VIN pin. Do not input a command code via the interface for specific period of time (t2) after releasing reset state for a certain stabilization of the internal oscillation frequency. The following figure shows the POR timing when power is applied. During the “t1” period, a command from the interface is not accepted. Please note, that a command accepted during the “t2” period may be interpreted incorrectly.

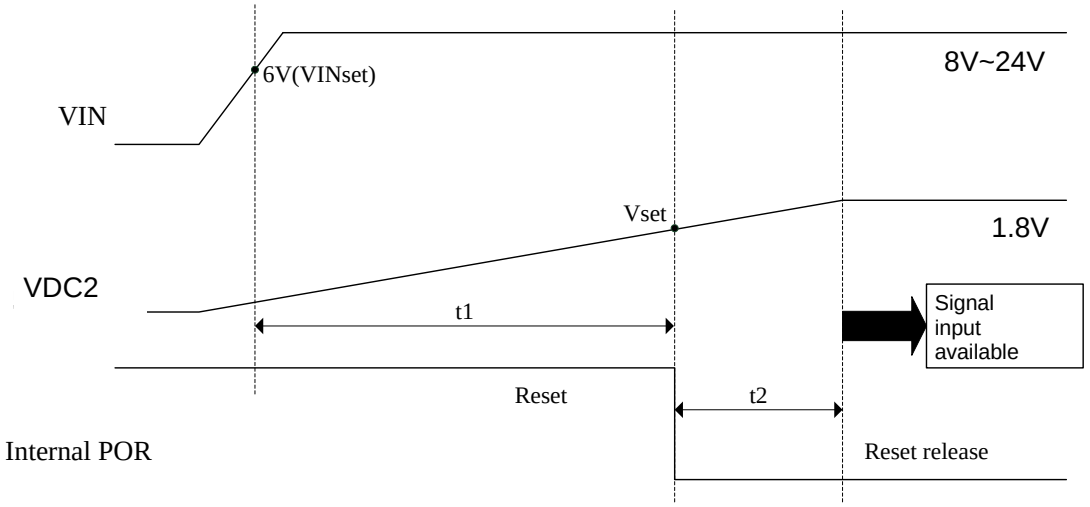


Figure 6. POR Operation (Power on Reset)

Table 12. POR Timing when Power Applied

Item	min	typ	max	Unit	Condition
t1	-	-	2800	μs	VIN pin voltage > 6V, IDC1= -30mA. Bypass capacitor between the VDC pin and GND CVDC=1.0μF.
t2	-	-	200	μs	Stabilization time of internal power

Note 17. As shown above, the AP4202 is in normal operation after 3msec at maximum from the time the VIN voltage reaches 6V. In the case of Input Voltage Range 2, the AP4202 is in normal operation after 3mec from the time the VIN voltage reaches 4.5V.

Note 18. A recovery time of when the internal POR circuit is reset by a decreasing VIN voltage also follows the prescribed times above (t1, t2) even if it is not the power-up sequence of the AP4202.

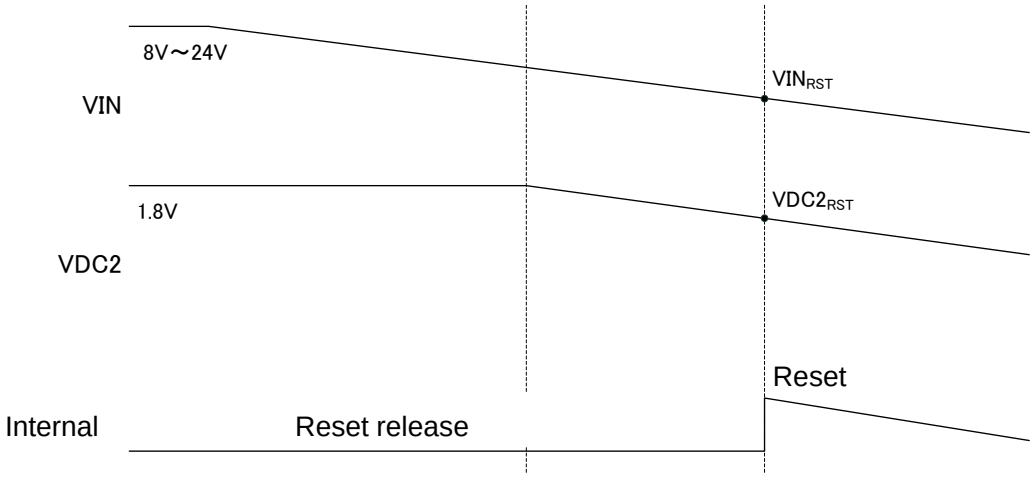


Figure 7. POR Operating Power Off

Table 13. POR Timing when VIN Decreases

Item	min	typ	max	Unit	Condition
VINrst	-	3.6	4.2	V	VIN reset voltage
VDC2rst	-	1.2	1.5	V	Internal 1.8V LDO reset voltage (reference value)

Note 19. This function executes reset when the supply voltage decreases, preventing instability. However, the reset may not be executed even the supply voltage becomes below the VINrst voltage such as when VIN decreases to near 0V instantaneously. Therefore, in the actual use, it is recommended to design the application in consideration with the VIN voltage to avoid activating this function by peripheral noise or voltage fluctuations.

Note 20. The IC is designed to work normally as possible, so sometimes LED gradation data can be hold even when VIN< VIN_{RST}, and LEDs turn off all at once. (Lighting setting is holding)

Note 21. As long as the VIN voltage (IC pin voltage) is more than the maximum VINrst voltage, continuous proper operation of the AP4202 is guaranteed (by design). However if the VIN voltage is out of recommend voltage range, the communication function via input signal is not guaranteed.

10.7. Reset State

Immediately after start up the AP4202 or after reset by decreasing power supply voltage, LED gradation data in the IC is all reset (all data= “0”). Therefore, LEDs will not light unless new gradation data is input via SCI interface. The AP4202 has all turn off function (in case of SCI interface control). It can be used as reset function. Reset types and reset states are shown below.

Table 14. Types of reset and status

	Types of Reset				
	VIN Input	VIN falls	VDC1 falls	VDC2 falls	LED All Off
LED lighting status	LED All Off				
LED gradation data input	Impossible				Possible
LED gradation data hold	—	Hold	Hold	Reset	Hold
LDO1(5V) Output	Undefined				Normal

10.8. Protection Functions

The AP4202 has an over current (LED current) protection and a thermal protection function in order to prevent damaging the IC. The LED current is shut off when these functions are activated and recovers automatically when the fault condition is removed.

Table 15. Protection Function (All values are guaranteed by design)

Protection Function	Over Current Protection	Thermal Protection
LED Current Shut-off Condition	LED Current per channel ≥ 190mA (typ.)	Junction Temperature ≥ 140°C (typ.)
LED Current Shut-off points	Objective LED line	All 9 Channels (also shut-off VDC1 output)
Recovery Type	Timer-latch type recovery Check if the overcurrent condition still exists after 0.3 second (typ) following LED current shut-off. After checking three times, if the over current condition still exists, LED current will be shut off continuously. (Latching)	Auto-recovery
Recovery Condition	Before Latch: Intended channel current ≥ 190mA (typ.) After Latch: Power Reboot	Junction Temperature ≥ 120°C (typ.)

Note 22. The over current protection function works when the LED is lighten by shutting off the LED current. In the case that LED channels are not set to light the LEDs, this protection will not work even if the LED pin voltage is high. This function is disabled in fixed current output mode.

Note 23. The thermal protection function is an auxiliary function for the worst case and it is not guaranteed to work reliably. Therefore, it is recommended that application is designed in consideration with heat generation in order to prevent activation of the thermal protection.

Note 24. When the VDC1 and VDC2 pins are shorted to GND, there is a case that thermal protection works because the internal LDO is overheated by high VIN voltage and there is a case that Power On Reset works because of the voltage at the VDC2 pin is decreased. The external current capability of the VDC1 pin is maximum 30mA.

Note 25. V_{LED} voltage and LED current settings according to the ambient temperature (Ta) are shown below.

Table 16. V_{LED} voltage and LED current setting (Condition: V_{IN}=12V, I_{DC1}=0mA)

Output setting	IC ambient temperature	LED pin voltage	LED current
DRSET	Ta [°C]	V_{LED} [V]	I_{LED} [mA]
Low (open drain)	25	—	I_{LEDTO}=96 [mA]
	55		I_{LEDTO}=80 [mA]
	70		I_{LEDTO}=70 [mA]
High (fixed current)	25	2.9	I_{LEDTC}=26 [mA]
		2.5	I_{LEDTC}=30 [mA]
		2.1	I_{LEDTC}=36 [mA]
		1.7	I_{LEDTC}=44 [mA]
	55	2.9	I_{LEDTC}=18 [mA]
		2.5	I_{LEDTC}=20 [mA]
		2.1	I_{LEDTC}=24 [mA]
		1.7	I_{LEDTC}=30 [mA]
	70	2.9	I_{LEDTC}=13 [mA]
		2.5	I_{LEDTC}=16 [mA]
		2.1	I_{LEDTC}=19 [mA]
		1.7	I_{LEDTC}=24 [mA]

11. Recommended External Circuits

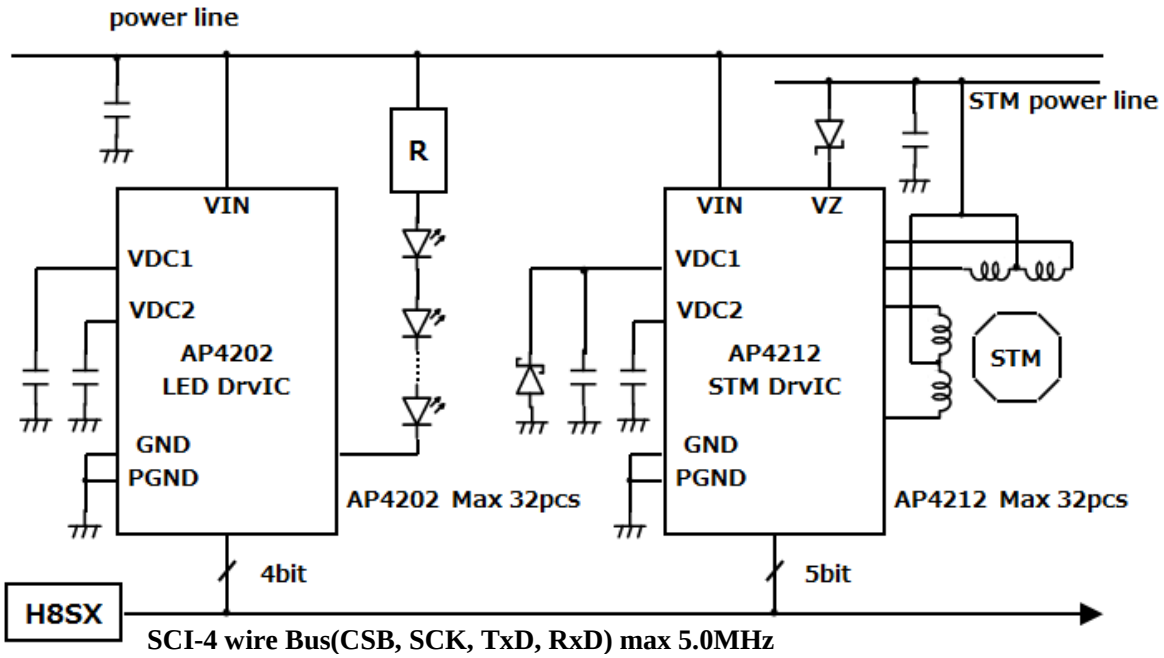


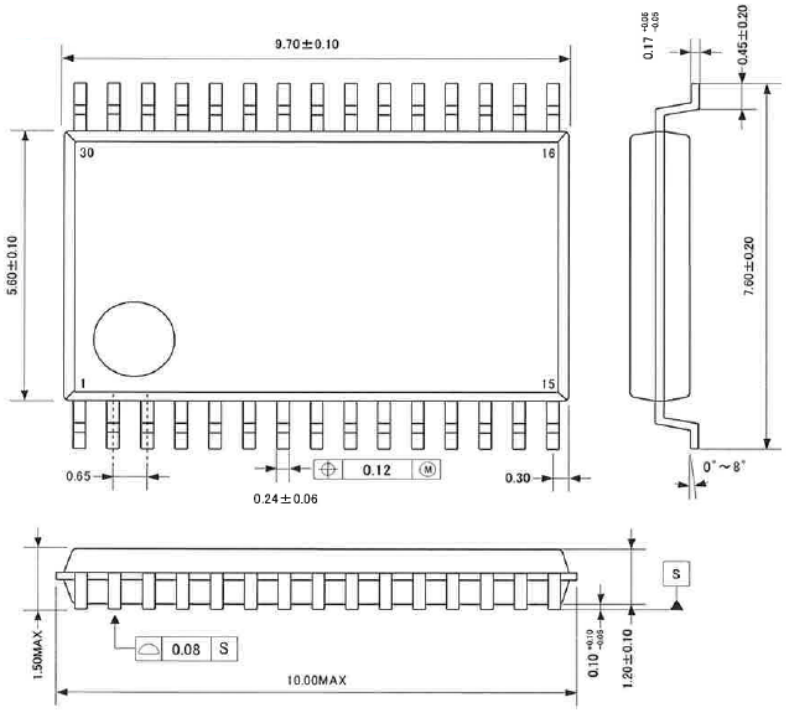
Figure 8. Recommended External Circuits

Note 26. If data on the AP4202/AP4212 application board will not be read, it is unnecessary to connect RxD of the SCI 4-wire BUS. The 4-wire BUS can be reduced to a 3-wire BUS. The RxD terminal is an output terminal, and it should be open when RxD is not used. When using the AP4202 as an open drain driver, external resistors for current setting can be removed. In this case, the ISET_R, G, B pins should also be open.

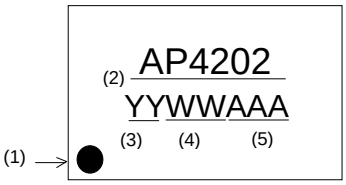
12. Package

■ Package

・30-pin VSOP (Unit : mm)



■ Marking



(1) 1pin Indication
(2) Market No.
(3) Year code (last 2 digits)
(4) Week code
(5) Management code

Note 27. Week code: the first Thursday of the week of the assembly year is marked to as 01, the second week is marked as 02 • • • and the 52nd week is marked as 52. (Compliance with ISO-8601)
Please contact to our sales office for more detailed marking specification. (example: marking size, marking print sample and etc.)

13. Revision History

Date (Y/M/D)	Revision	Page	Contents
17/01/13	00	-	First Edition

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