



**Advanced Power
Electronics Corp.**

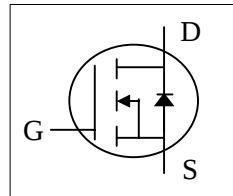
AP4420GH/J

Pb Free Plating Product

N-CHANNEL ENHANCEMENT MODE

POWER MOSFET

- ▼ Lower Gate Charge
- ▼ Simple Drive Requirement
- ▼ Fast Switching Characteristic
- ▼ RoHS Compliant

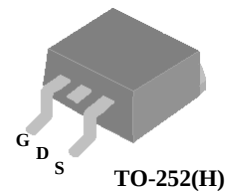


BV_{DSS}	35V
$R_{DS(ON)}$	10m Ω
I_D	52A

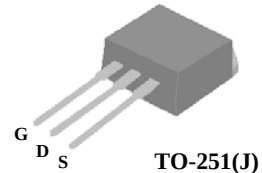
Description

The Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-252 package is universally preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters. The through-hole version (AP4420GJ) are available for low-profile applications.



TO-252(H)



TO-251(J)

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	35	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^\circ\text{C}$	Continuous Drain Current	52	A
$I_D@T_C=100^\circ\text{C}$	Continuous Drain Current	33	A
I_{DM}	Pulsed Drain Current ¹	200	A
$P_D@T_C=25^\circ\text{C}$	Total Power Dissipation	45	W
	Linear Derating Factor	0.35	W/ $^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Value	Units
Rthj-c	Thermal Resistance Junction-case	Max. 2.8	$^\circ\text{C}/\text{W}$
Rthj-a	Thermal Resistance Junction-ambient	Max. 110	$^\circ\text{C}/\text{W}$



AP4420GH/J

Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	35	-	-	V
ΔBV _{DSS} /ΔT _j	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I _D =1mA	-	0.01	-	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =30A	-	-	10	mΩ
		V _{GS} =4.5V, I _D =15A	-	-	24	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	1	-	3	V
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =30A	-	28	-	S
I _{DSS}	Drain-Source Leakage Current (T _j =25°C)	V _{DS} =35V, V _{GS} =0V	-	-	1	uA
	Drain-Source Leakage Current (T _j =150°C)	V _{DS} =28V, V _{GS} =0V	-	-	25	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V	-	-	±100	nA
Q _g	Total Gate Charge ²	I _D =30A	-	16	26	nC
Q _{gs}	Gate-Source Charge	V _{DS} =25V	-	6	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =4.5V	-	9.5	-	nC
t _{d(on)}	Turn-on Delay Time ²	V _{DS} =15V	-	9	-	ns
t _r	Rise Time	I _D =30A	-	74	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =3.3Ω, V _{GS} =10V	-	22.5	-	ns
t _f	Fall Time	R _D =0.5Ω	-	7.7	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	1520	2430	pF
C _{oss}	Output Capacitance	V _{DS} =25V	-	320	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	230	-	pF
R _g	Gate Resistance	f=1.0MHz	-	1.8	2.7	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ²	I _S =30A, V _{GS} =0V	-	-	1.2	V
t _{rr}	Reverse Recovery Time ²	I _S =20A, V _{GS} =0V,	-	27	-	ns
Q _{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	20	-	nC

Drain-Source Avalanche Ratings

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
E _{AS}	Drain-Source Avalanche Energy ³	I _D =15A, V _{DD} =35V, L=1mH	-	-	113	mJ
I _{AS}	Drain-Source Avalanche Current		-	15	-	A

Notes:

- 1.Pulse width limited by safe operating area.
- 2.Pulse width ≤300us , duty cycle ≤2%.
- 3.Single Pulse Test.

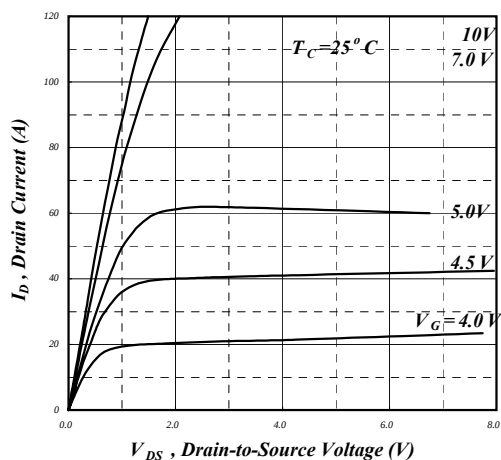


Fig 1. Typical Output Characteristics

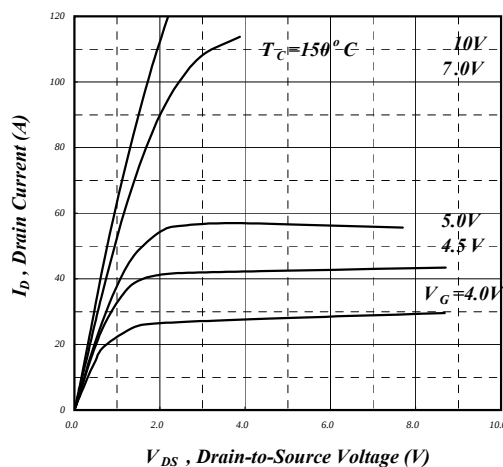


Fig 2. Typical Output Characteristics

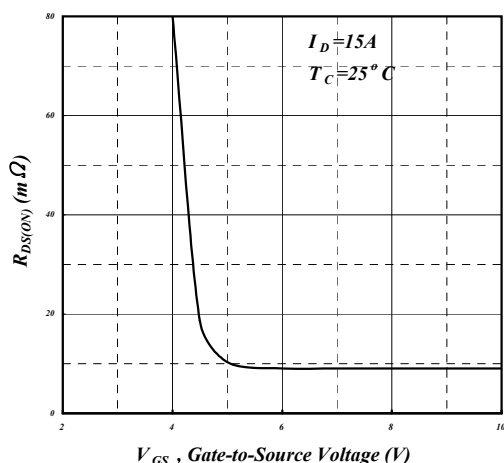


Fig 3. On-Resistance v.s. Gate Voltage

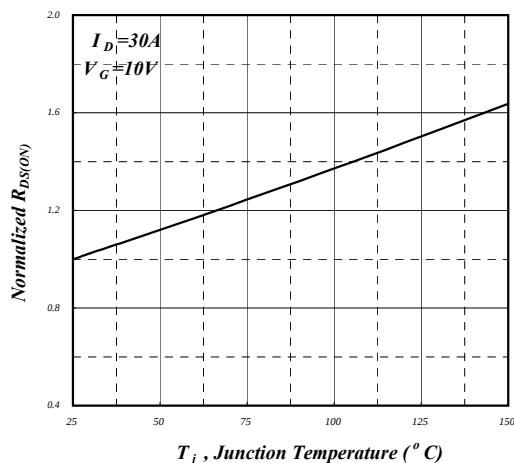


Fig 4. Normalized On-Resistance
v.s. Junction Temperature

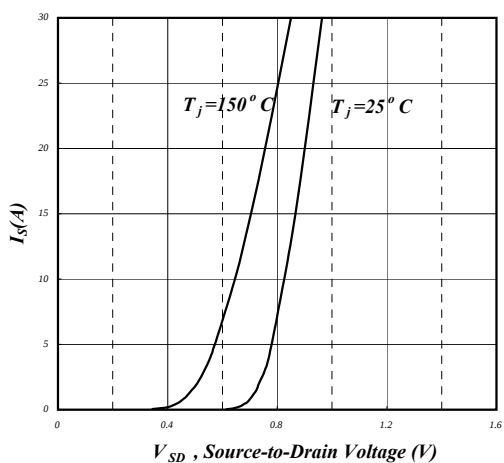


Fig 5. Forward Characteristic of
Reverse Diode

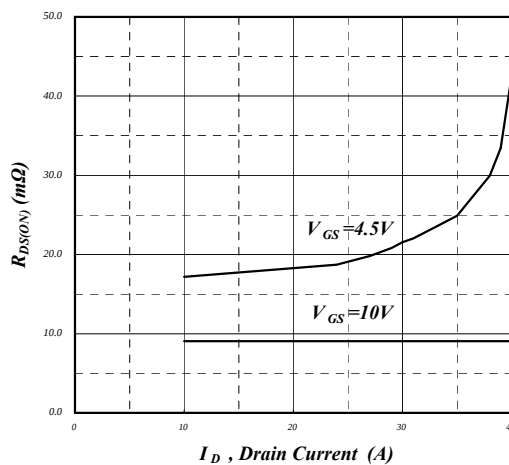


Fig 6. On-Resistance vs.
Drain Current

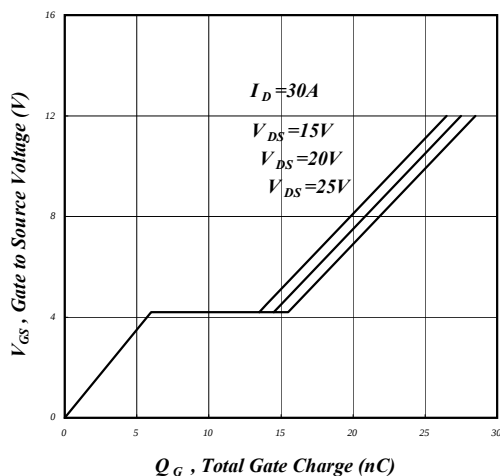


Fig 7. Gate Charge Characteristics

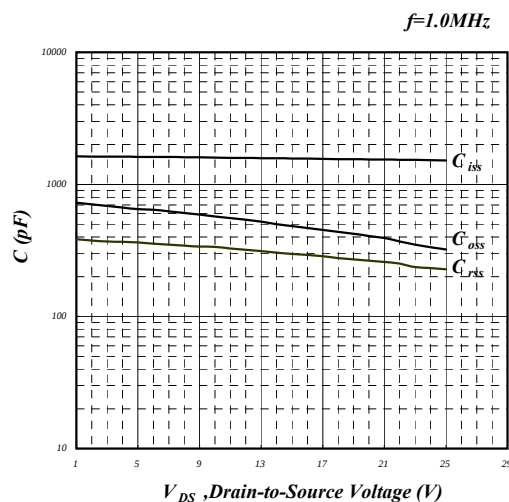


Fig 8. Typical Capacitance Characteristics

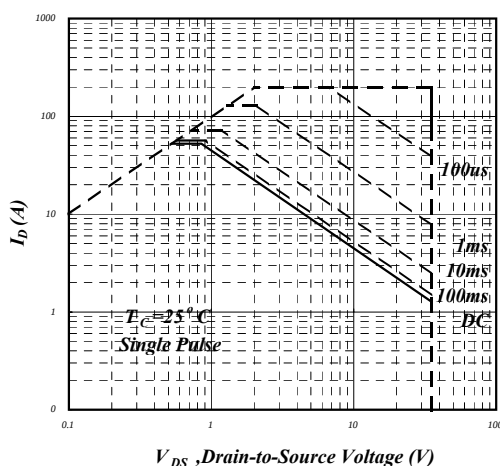


Fig 9. Maximum Safe Operating Area

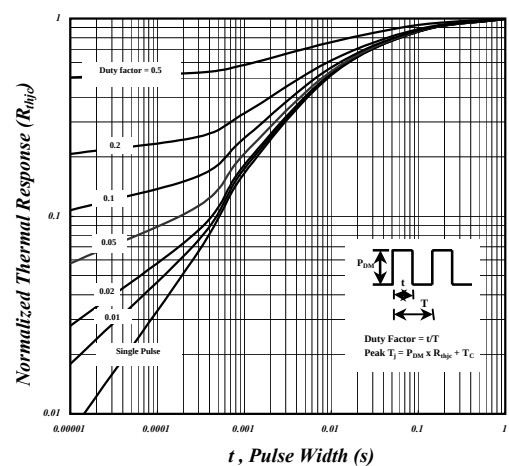


Fig 10. Effective Transient Thermal Impedance

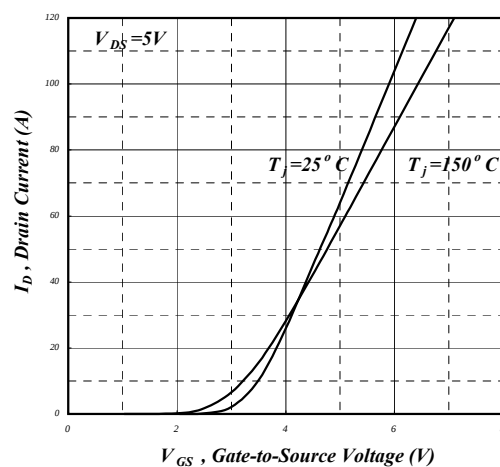


Fig 11. Transfer Characteristics

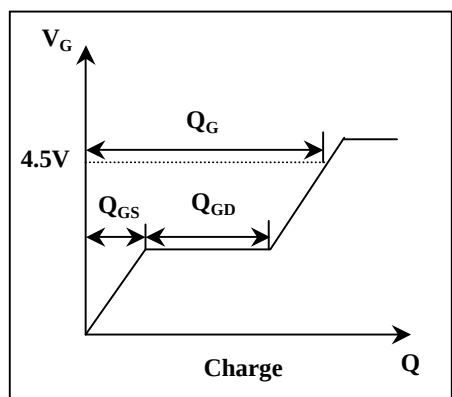


Fig 12. Gate Charge Waveform