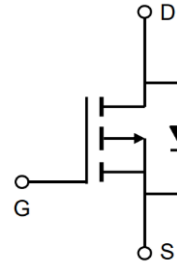


30V P-Channel Enhancement Mode MOSFET

Description

The AP4435A uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



General Features

$V_{DS} = -30V$ $I_D = -10.5A$

$R_{DS(ON)} < 16m\Omega @ V_{GS} = -10V$

Application

Lithium battery protection
 Wireless impact
 Mobile phone fast charging



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP4435A	SOP-8	AP4435A XXX YYYY	3000

Absolute Maximum Ratings (TC=25°C unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-10.5	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-8.6	A
IDM	Pulsed Drain Current ²	-50	A
EAS	Single Pulse Avalanche Energy ³	72.2	mJ
IAS	Avalanche Current	-38	A
$P_D @ T_A = 25^\circ C$	Total Power Dissipation ⁴	3.1	W
$P_D @ T_A = 70^\circ C$	Total Power Dissipation ⁴	2	W
TSTG	Storage Temperature Range	-55 to 150	°C
T_J	Operating Junction Temperature Range	-55 to 150	°C
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	75	°C/W
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹ ($t \leq 10s$)	40	°C/W
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	24	°C/W

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Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250uA	-30	-32	---	V
ΔBVDSS/ΔT _J	BV _{DSS} Temperature Coefficient	Reference to 25°C, I _D =-1mA	---	-0.022	---	V/°C
RDS(ON)	Static Drain-Source On-Resistance ²	V _{GS} =-10V, I _D =-10A	---	12	16	mΩ
		V _{GS} =-4.5V, I _D =-5A	---	18	24	
VGS(th)	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =-250uA	-1.0	-1.6	-2.5	V
ΔVGS(th)	V _{GS(th)} Temperature Coefficient		---	4.6	---	mV/°C
IDSS	Drain-Source Leakage Current	V _{DS} =-24V, V _{GS} =0V, T _J =25°C	---	---	-1	uA
		V _{DS} =-24V, V _{GS} =0V, T _J =55°C	---	---	-5	
IGSS	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
gfs	Forward Transconductance	V _{DS} =-5V, I _D =-5A	---	17	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	13	---	Ω
Q _g	Total Gate Charge (-4.5V)	V _{DS} =-15V, V _{GS} =-4.5V, I _D =-6A	---	30	---	nC
Q _{gs}	Gate-Source Charge		---	6	---	
Q _{gd}	Gate-Drain Charge		---	9	---	
Td(on)	Turn-On Delay Time	V _{DD} =-15V, V _{GS} =-10V, R _G =3.3Ω, I _D =-6A	---	10	---	ns
T _r	Rise Time		---	26	---	
Td(off)	Turn-Off Delay Time		---	35	---	
T _f	Fall Time		---	8	---	
Ciss	Input Capacitance	V _{DS} =-15V, V _{GS} =0V, f=1MHz	---	1800	---	pF
Coss	Output Capacitance		---	305	---	
Crss	Reverse Transfer Capacitance		---	216	---	
I _S	Continuous Source Current ^{1,5}	V _G =V _D =0V, Force Current	---	---	-10	A
I _{SM}	Pulsed Source Current ^{2,5}		---	---	-50	A
VSD	Diode Forward Voltage ²	V _{GS} =0V, I _S =-1A, T _J =25°C	---	---	-1.2	V
trr	Reverse Recovery Time	I _F =-6A, dI/dt=100A/μs, T _J =25°C	---	16.3	---	nS
Q _{rr}	Reverse Recovery Charge		---	5.9	---	nC

Note :

- 1、The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.
- 2、The data tested by pulsed, pulse width ≦ 300us, duty cycle ≦ 2%
- 3、The EAS data shows Max. rating. The test condition is VDD=-25V, VGS=-10V, L=0.1mH, IAS=-38A
- 4、The power dissipation is limited by 150°C junction temperature
- 5、The data is theoretically the same as ID and IDM, in real applications, should be limited by total power dissipation.

30V P-Channel Enhancement Mode MOSFET

Typical Characteristics

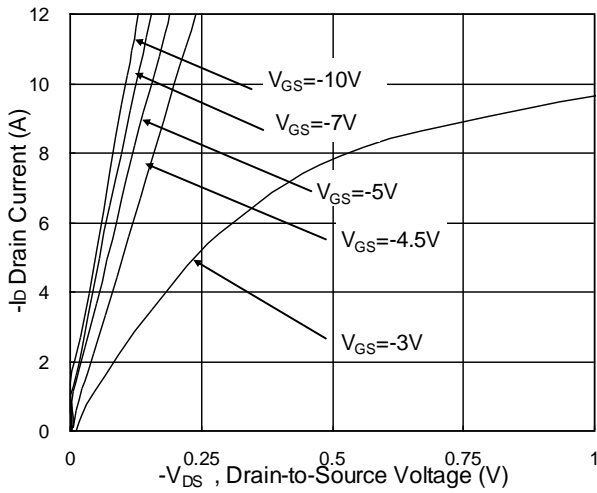


Fig.1 Typical Output Characteristics

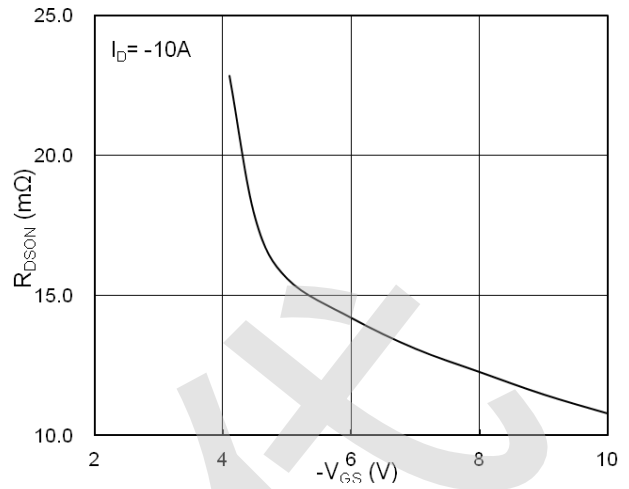


Fig.2 On-Resistance vs. G-S Voltage

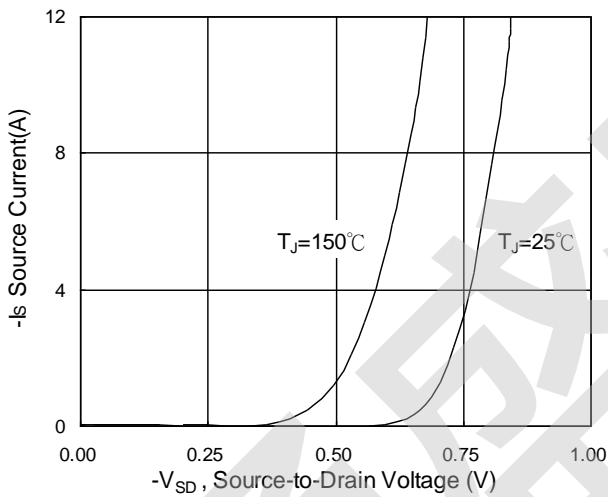


Fig.3 Forward Characteristics of Reverse

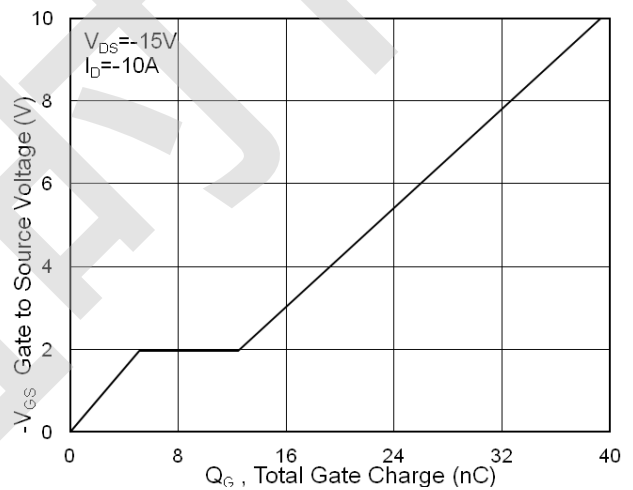


Fig.4 Gate-charge Characteristics

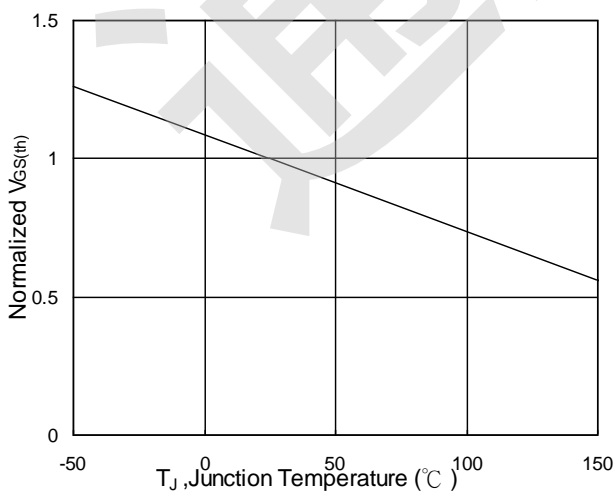


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

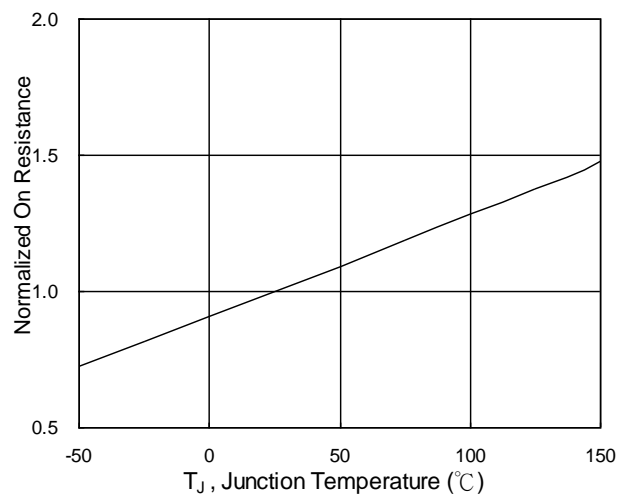


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

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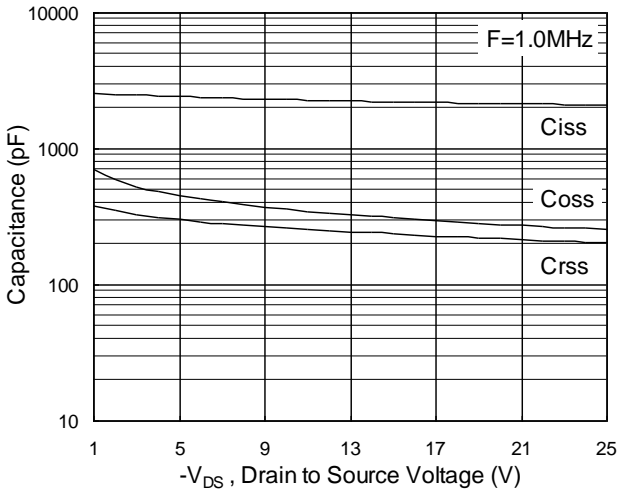


Fig.7 Capacitance

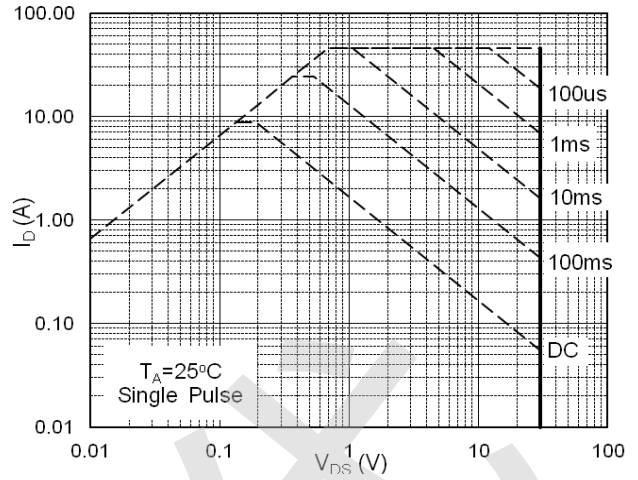


Fig.8 Safe Operating Area

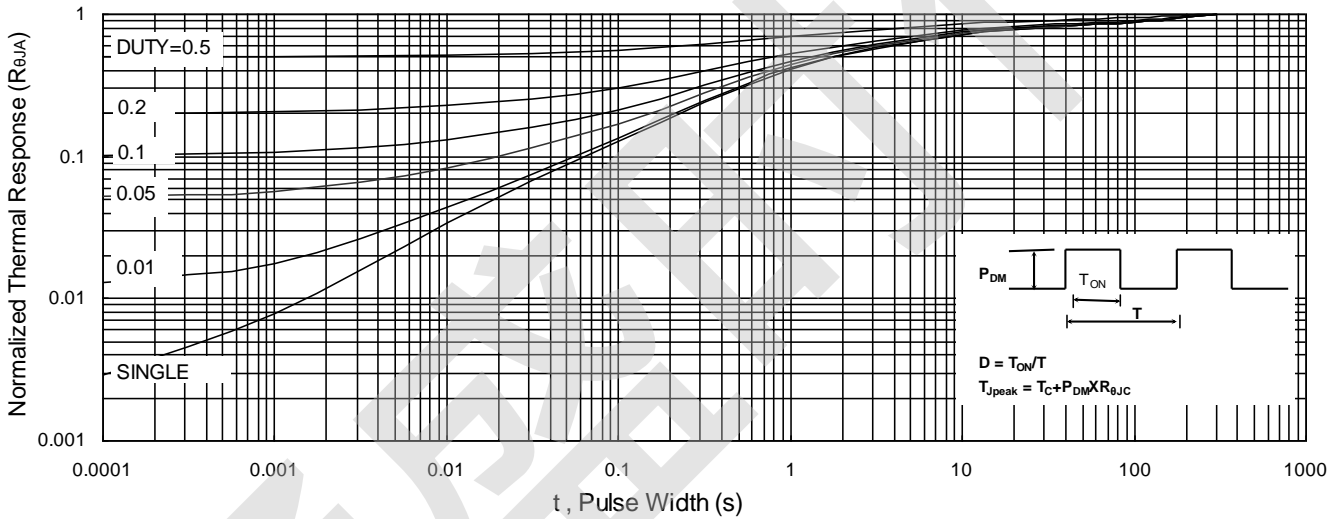


Fig.9 Normalized Maximum Transient Thermal Impedance

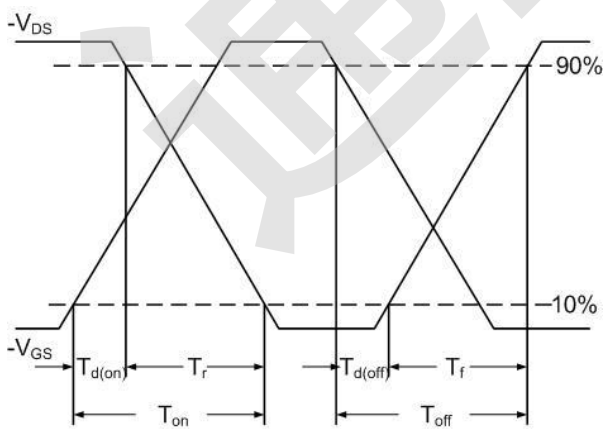


Fig.10 Switching Time Waveform

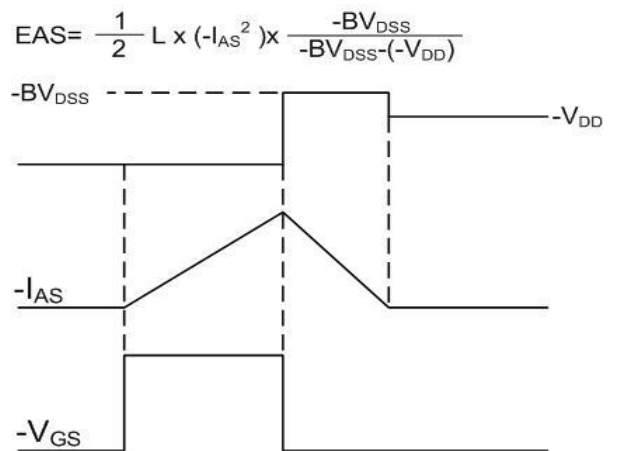
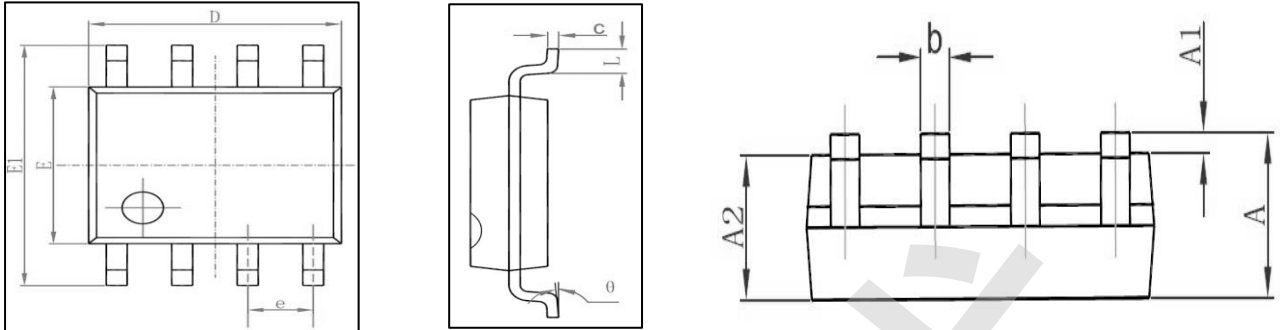


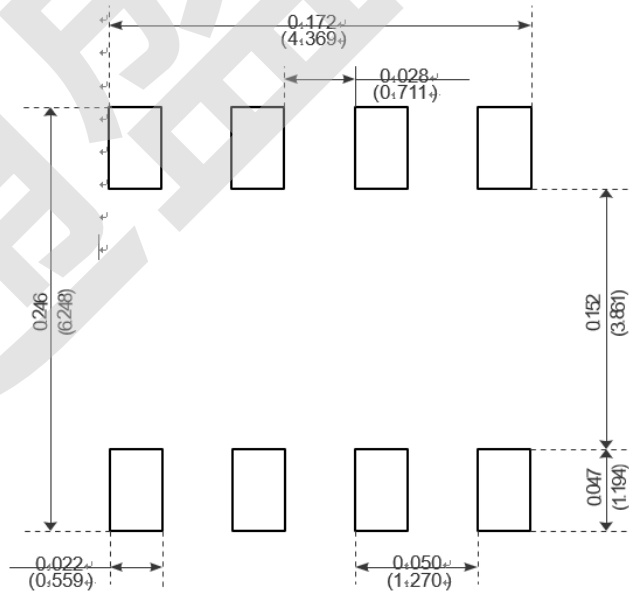
Fig.11 Unclamped Inductive Waveform

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Package Mechanical Data-SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Recommended Minimum Pads

30V P-Channel Enhancement Mode MOSFET Attention

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30V P-Channel Enhancement Mode MOSFET

Edition	Date	Change
Rve1.0	2018/1/31	Initial release
Rve1.2	2019/5/25	Reduce CiSS and QG
Rve1.3	2020/6/20	Reduce RDS

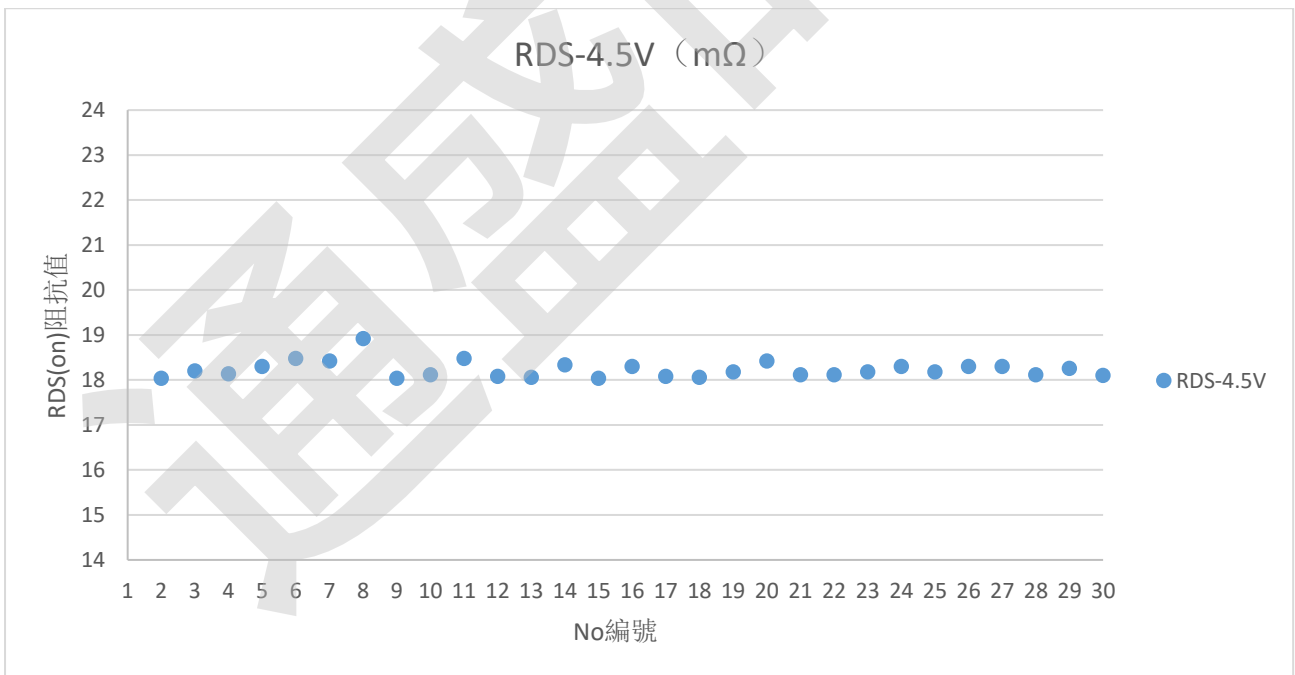
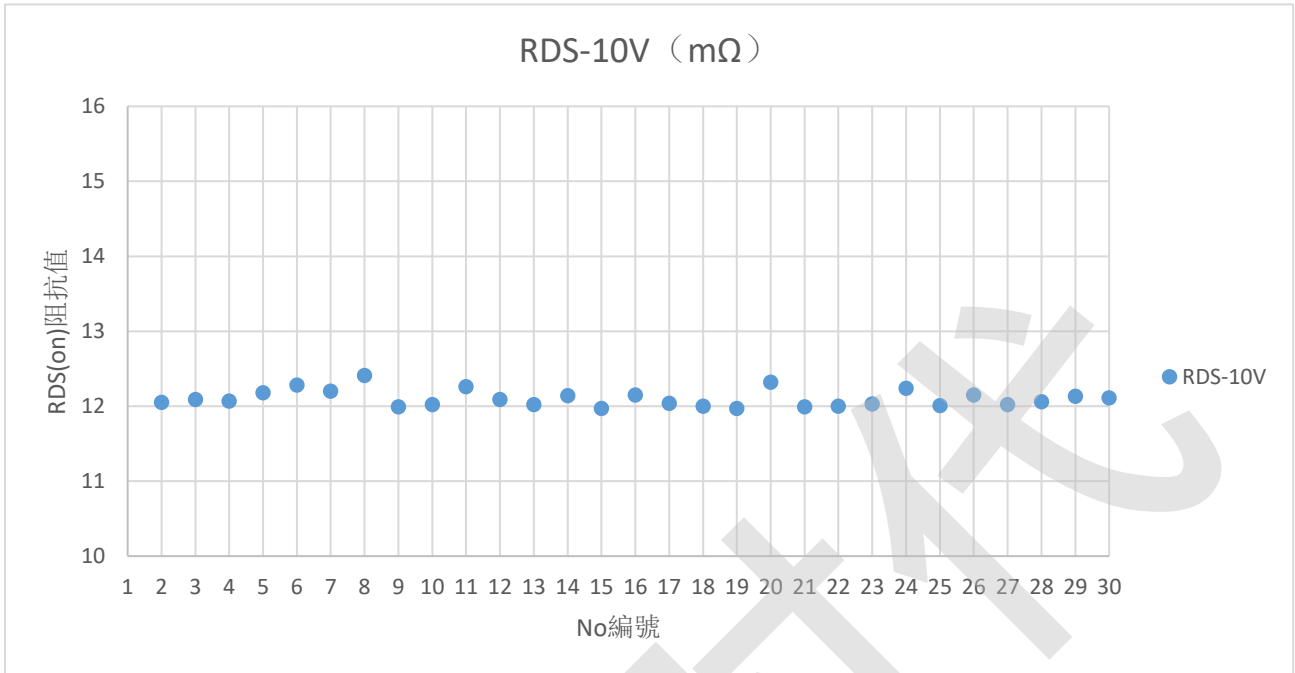
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30V P-Channel Enhancement Mode MOSFET

Test Report For 30PCS (30pcs 典型測試報告)





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