

AP4501SSD

**Advanced Power
Electronics Corp.**

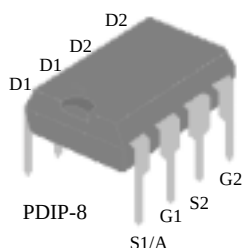
N with Schottky AND P-CHANNEL

ENHANCEMENT MODE POWER MOSFET

▼ Simple Drive Requirement

▼ Low On-resistance

▼ Fast Switching

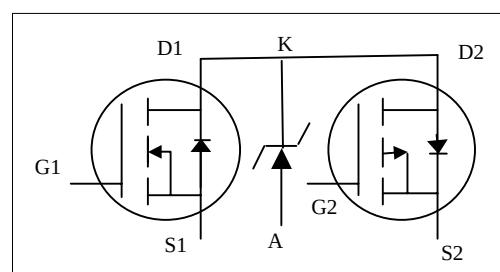


N-CH	BV_{DSS}	30V
	$R_{DS(ON)}$	36m Ω
	I_D	5.3A
P-CH	BV_{DSS}	-30V
	$R_{DS(ON)}$	60m Ω
	I_D	-4.2A

Description

The Advanced Power MOSFETs from APEC provide the design with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

AP4501SSD included N , P channel enhancement mode power MOSFET and Schottky diode.



Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-channel	P-channel	
V_{DS}	Drain-Source Voltage	30	-30	V
V_{GS}	Gate-Source Voltage	± 20	± 20	V
$I_D @ T_A = 25^\circ\text{C}$	Continuous Drain Current ³	5.3	-4.2	A
$I_D @ T_A = 70^\circ\text{C}$	Continuous Drain Current ³	4.3	-3.5	A
I_{DM}	Pulsed Drain Current ¹	40	-30	A
$P_D @ T_A = 25^\circ\text{C}$	Total Power Dissipation	2		W
	Linear Derating Factor	0.016		W/ $^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to 150		$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 125		$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Value	Unit
$R_{thj-amb}$	Thermal Resistance Junction-ambient ³	Max. 62.5	$^\circ\text{C}/\text{W}$



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N-CH Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	30	-	-	V
ΔBV _{DSS} /ΔT _j	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I _D =1mA	-	0.031	-	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =5.3A	-	-	36	mΩ
		V _{GS} =4.5V, I _D =4A	-	-	55	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	1	-	3	V
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =5.3A	-	10	-	S
I _{DSS}	Drain-Source Leakage Current (T _j =25°C) ⁴	V _{DS} =30V, V _{GS} =0V	-	-	100	uA
	Drain-Source Leakage Current (T _j =70°C)	V _{DS} =24V, V _{GS} =0V	-	-	1	mA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V	-	-	±100	nA
Q _g	Total Gate Charge ²	I _D =5.3A	-	8.2	-	nC
Q _{gs}	Gate-Source Charge	V _{DS} =24V	-	2.3	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =4.5V	-	4.8	-	nC
t _{d(on)}	Turn-on Delay Time ²	V _{DS} =15V	-	6	-	ns
t _r	Rise Time	I _D =1A	-	5.2	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =3.3Ω, V _{GS} =10V	-	18.8	-	ns
t _f	Fall Time	R _D =15Ω	-	4.4	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	645	-	pF
C _{oss}	Output Capacitance	V _{DS} =25V	-	150	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	95	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I _S	Source Current (Body Diode) ²	V _D =V _G =0V, V _S =1.2V	-	-	1.7	A
V _{SD}	Forward On Voltage ²	I _S =1.7A, V _{GS} =0V	-	-	1.2	V

Schottky Characteristics@T_j=25°C

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _F	Forward Voltage Drop	I _F =1A	-	-	0.5	V
I _{rm}	Maximum Reverse Leakage Current	V _r =30V	-	-	100	uA



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P-CH Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250uA	-30	-	-	V
ΔBV _{DSS} /ΔT _j	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I _D =-1mA	-	-0.03	-	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =-10V, I _D =-4.2A	-	-	60	mΩ
		V _{GS} =-4.5V, I _D =-3A	-	-	80	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250uA	-1	-	-3	V
g _{fs}	Forward Transconductance	V _{DS} =-10V, I _D =-4.2A	-	7.2	-	S
I _{DSS}	Drain-Source Leakage Current (T=25°C)	V _{DS} =-30V, V _{GS} =0V	-	-	-1	uA
	Drain-Source Leakage Current (T=70°C)	V _{DS} =-24V, V _{GS} =0V	-	-	-25	uA
I _{GSS}	Gate-Source Leakage	V _{GS} = ± 20V	-	-	±100	nA
Q _g	Total Gate Charge ²	I _D =-4.2A	-	9	-	nC
Q _{gs}	Gate-Source Charge	V _{DS} =-15V	-	3.5	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =-4.5V	-	2	-	nC
t _{d(on)}	Turn-on Delay Time ²	V _{DS} =-15V	-	12	-	ns
t _r	Rise Time	I _D =-1A	-	20	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =6Ω, V _{GS} =-10V	-	45	-	ns
t _f	Fall Time	R _D =15Ω	-	27	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	760	-	pF
C _{oss}	Output Capacitance	V _{DS} =-25V	-	330	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	90	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I _S	Source Current (Body Diode ²)	V _D =V _G =0V , V _S =-1.2V	-	-	-1.7	A
V _{SD}	Forward On Voltage ²	I _S =-1.7A, V _{GS} =0V	-	-	-1.2	V

Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse width ≤300us , duty cycle ≤2%.
- 3.Mounted on 1 in² copper pad of FR4 board ; 90°C/W when mounted on Min. copper pad.
- 4.I_{DSS} is the leakage current measurement combined with Schottky diode.



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N-Channel

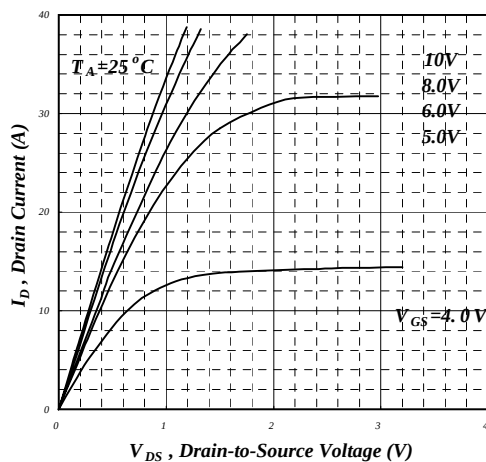


Fig 1. Typical Output Characteristics

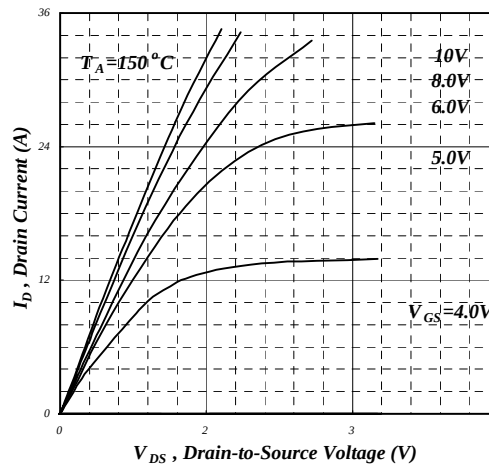


Fig 2. Typical Output Characteristics

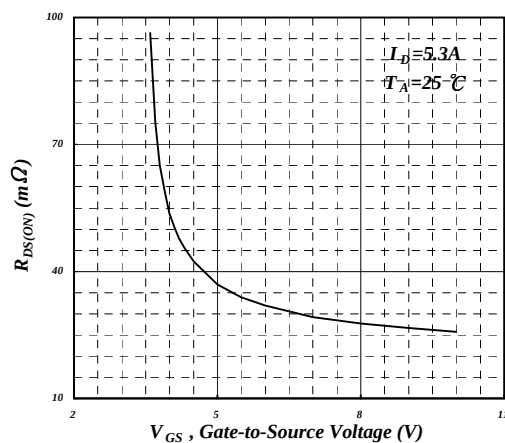


Fig 3. On-Resistance v.s. Gate Voltage

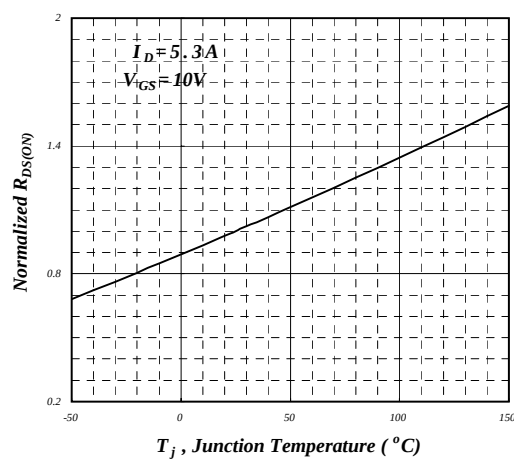


Fig 4. Normalized On-Resistance v.s. Junction Temperature

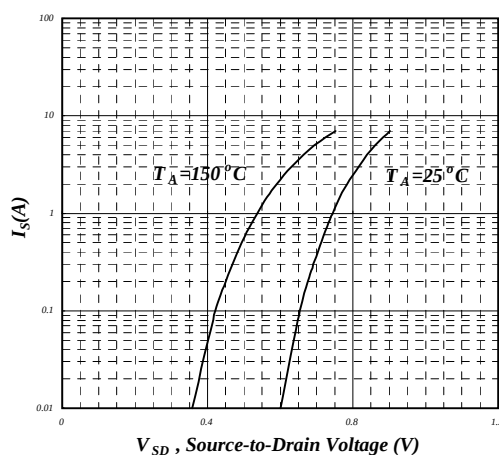


Fig 5. Forward Characteristic of Reverse Diode

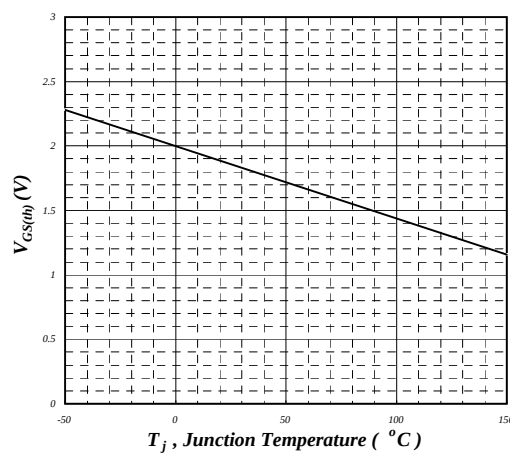


Fig 6. Gate Threshold Voltage v.s. Junction Temperature



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N-Channel

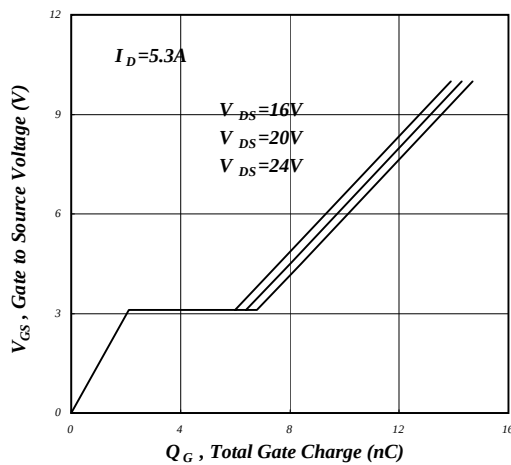


Fig 7. Gate Charge Characteristics

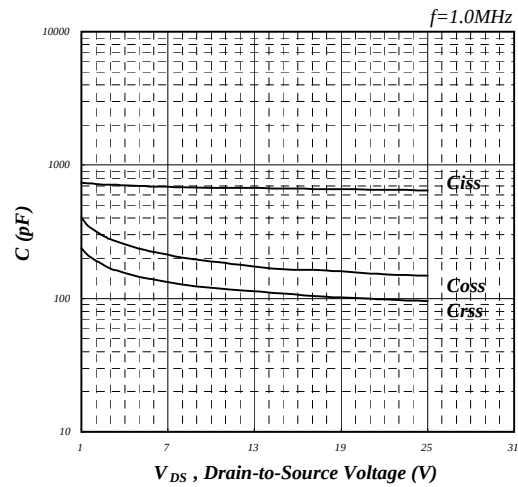


Fig 8. Typical Capacitance Characteristics

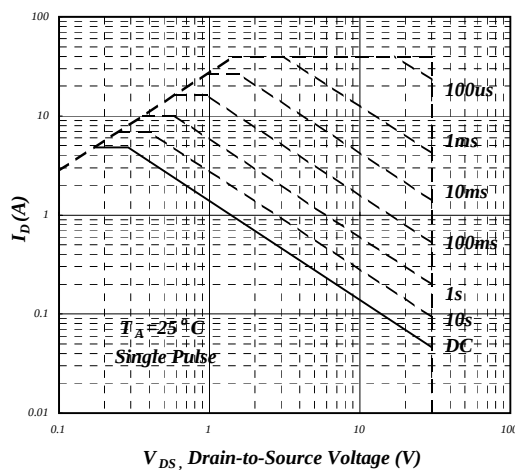


Fig 9. Maximum Safe Operating Area

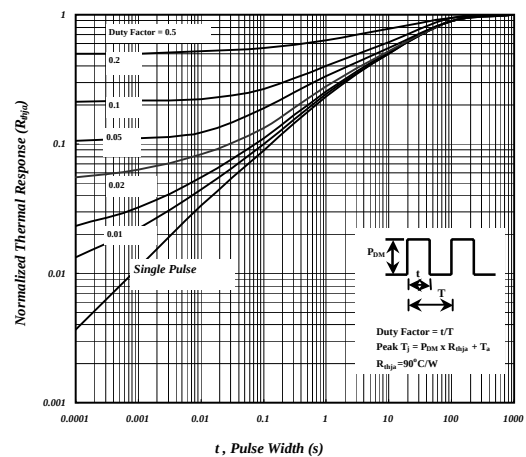


Fig 10. Effective Transient Thermal Impedance

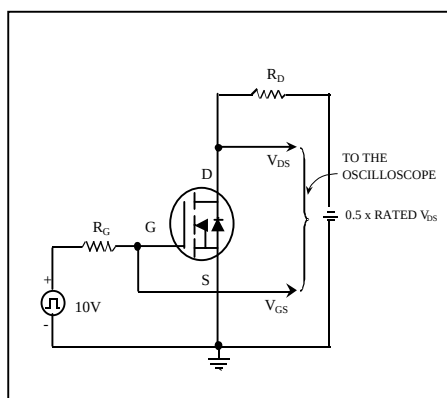


Fig 11. Switching Time Circuit

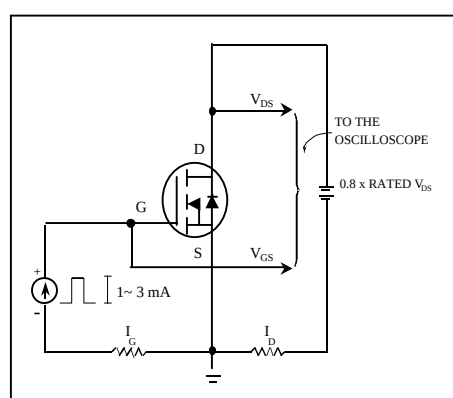


Fig 12. Gate Charge Circuit



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P-Channel

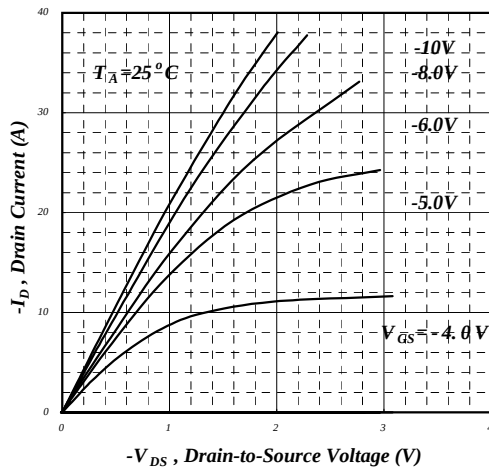


Fig 1. Typical Output Characteristics

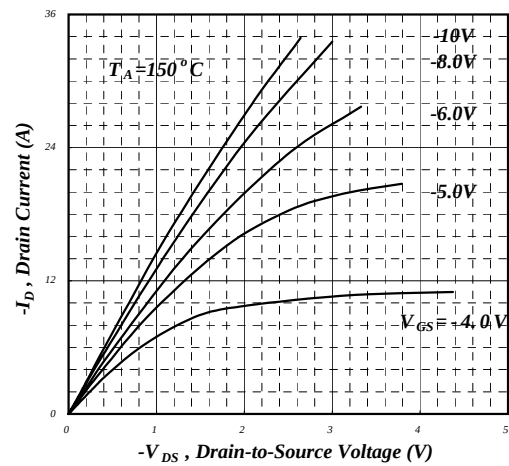


Fig 2. Typical Output Characteristics

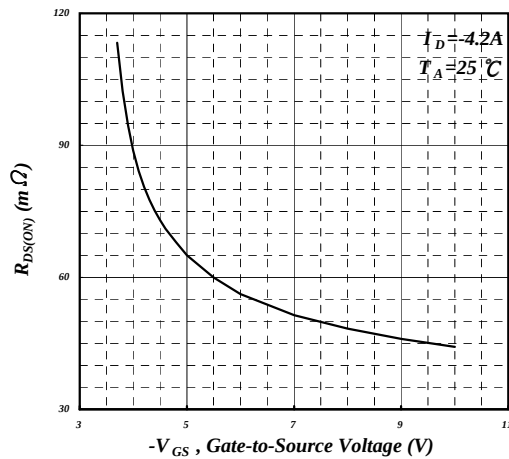


Fig 3. On-Resistance v.s. Gate Voltage

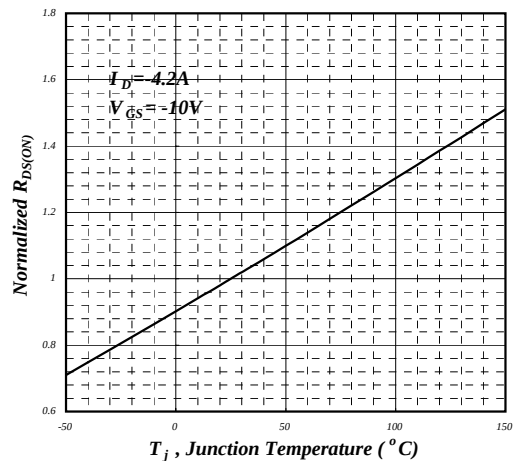


Fig 4. Normalized On-Resistance v.s. Junction Temperature

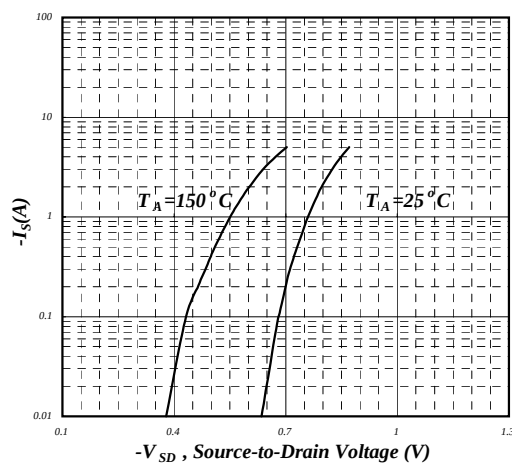


Fig 5. Forward Characteristic of Reverse Diode

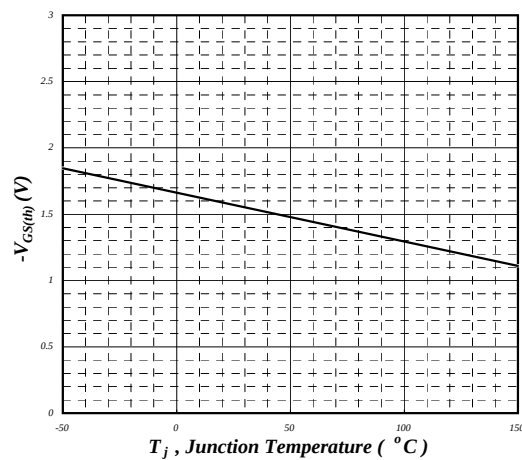


Fig 6. Gate Threshold Voltage v.s. Junction Temperature



P-Channel

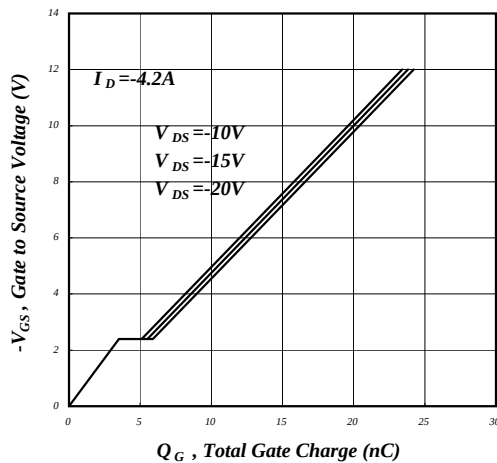


Fig 7. Gate Charge Characteristics

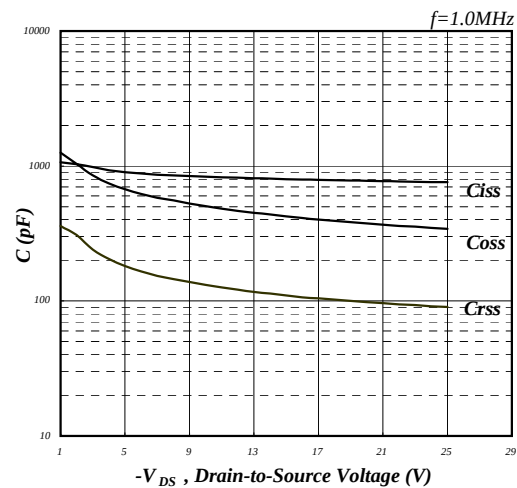


Fig 8. Typical Capacitance Characteristics

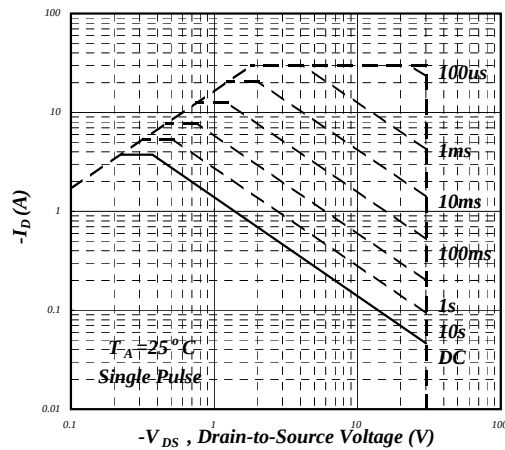


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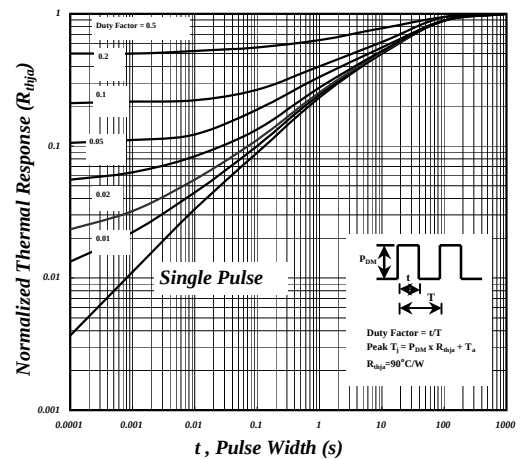


Fig 10. Effective Transient Thermal Impedance

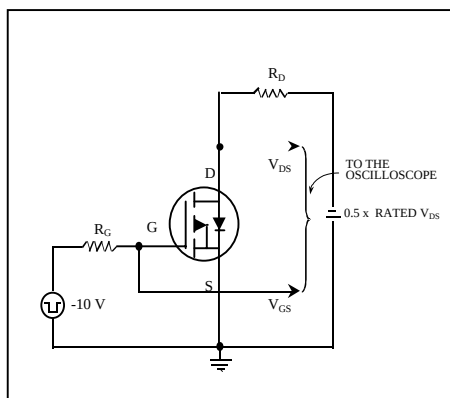


Fig 11. Switching Time Circuit

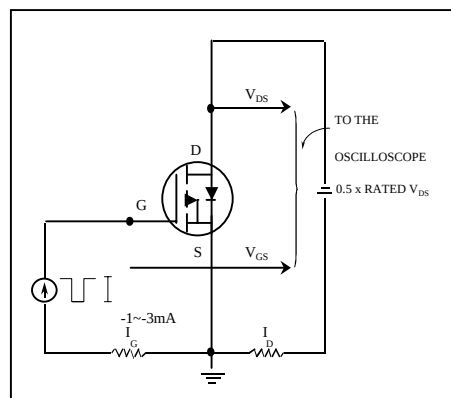


Fig 12. Gate Charge Circuit