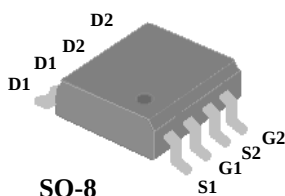




- ▼ Simple Drive Requirement
- ▼ Low On-resistance
- ▼ Fast Switching Characteristic

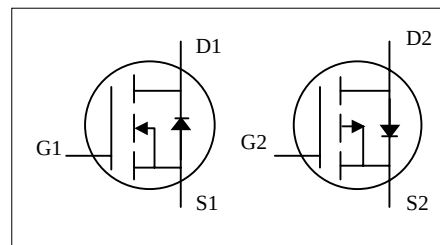


N-CH	BV_{DSS}	30V
	$R_{DS(ON)}$	50m Ω
	I_D	5A
P-CH	BV_{DSS}	-30V
	$R_{DS(ON)}$	70m Ω
	I_D	-4A

Description

Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SO-8 package is widely preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.



Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-channel	P-channel	
V_{DS}	Drain-Source Voltage	30	-30	V
V_{GS}	Gate-Source Voltage	± 20	± 20	V
$I_D@T_A=25^\circ\text{C}$	Continuous Drain Current ³	5	-4	A
$I_D@T_A=70^\circ\text{C}$	Continuous Drain Current ³	4	-3.2	A
I_{DM}	Pulsed Drain Current ¹	20	-20	A
$P_D@T_A=25^\circ\text{C}$	Total Power Dissipation	2		W
	Linear Derating Factor	0.016		W/ $^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to 150		$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150		$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Value	Unit
$R_{thj-amb}$	Maximum Thermal Resistance, Junction-ambient ³	62.5	$^\circ\text{C}/\text{W}$



AP4532GM

N-CH Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	30	-	-	V
ΔBV _{DSS} /ΔT _j	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I _D =1mA	-	0.037	-	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =5A	-	-	50	mΩ
		V _{GS} =4.5V, I _D =4.2A	-	-	70	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	1	-	3	V
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =5A	-	8	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =30V, V _{GS} =0V	-	-	1	uA
	Drain-Source Leakage Current (T _j =70°C)	V _{DS} =24V, V _{GS} =0V	-	-	25	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Q _g	Total Gate Charge ²	I _D =5A	-	10.2	-	nC
Q _{gs}	Gate-Source Charge	V _{DS} =10V	-	1.2	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =10V	-	3.4	-	nC
t _{d(on)}	Turn-on Delay Time ²	V _{DS} =10V	-	6	-	ns
t _r	Rise Time	I _D =1A	-	9	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =6Ω, V _{GS} =10V	-	15	-	ns
t _f	Fall Time	R _D =10Ω	-	5.5	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	240	-	pF
C _{oss}	Output Capacitance	V _{DS} =25V	-	145	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	55	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I _S	Continuous Source Current (Body Diode)	V _D =V _G =0V, V _S =1.2V	-	-	1.7	A
V _{SD}	Forward On Voltage ²	T _j =25°C, I _S =1.7A, V _{GS} =0V	-	-	1.2	V

**P-CH Electrical Characteristics@T_j=25°C(unless otherwise specified)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	-30	-	-	V
ΔBV _{DSS} /ΔT _j	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I _D =-1mA	-	-0.028	-	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =-10V, I _D =-4A	-	-	70	mΩ
		V _{GS} =-4.5V, I _D =-3A	-	-	90	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250uA	-1	-	-3	V
g _{fs}	Forward Transconductance	V _{DS} =-10V, I _D =-4A	-	5	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =-30V, V _{GS} =0V	-	-	-1	uA
	Drain-Source Leakage Current (T _j =70°C)	V _{DS} =-24V, V _{GS} =0V	-	-	-25	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Q _g	Total Gate Charge ²	I _D =-4A	-	18.3	-	nC
Q _{gs}	Gate-Source Charge	V _{DS} =-10V	-	3.6	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =-10V	-	1.5	-	nC
t _{d(on)}	Turn-on Delay Time ²	V _{DS} =-10V	-	8	-	ns
t _r	Rise Time	I _D =-1A	-	9	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =6Ω, V _{GS} =-10V	-	21	-	ns
t _f	Fall Time	R _D =10Ω	-	10	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	760	-	pF
C _{oss}	Output Capacitance	V _{DS} =-25V	-	345	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	90	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I _S	Continuous Source Current (Body Diode)	V _D =V _G =0V , V _S =-1.2V	-	-	-1.7	A
V _{SD}	Forward On Voltage ²	T _j =25°C, I _S =-1.7A, V _{GS} =0V	-	-	-1.2	V

Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse width ≤300us , duty cycle ≤2%.
- 3.Surface mounted on 1 in² copper pad of FR4 board, t≤10sec ; 135 °C/W when mounted on Min. copper pad.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

APEC RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.



N-Channel

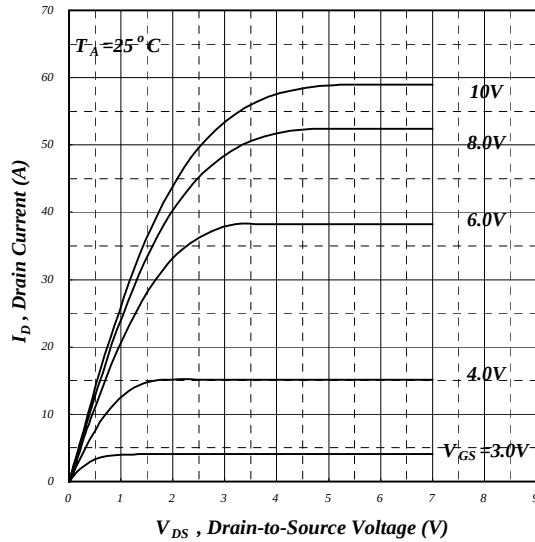


Fig 1. Typical Output Characteristics

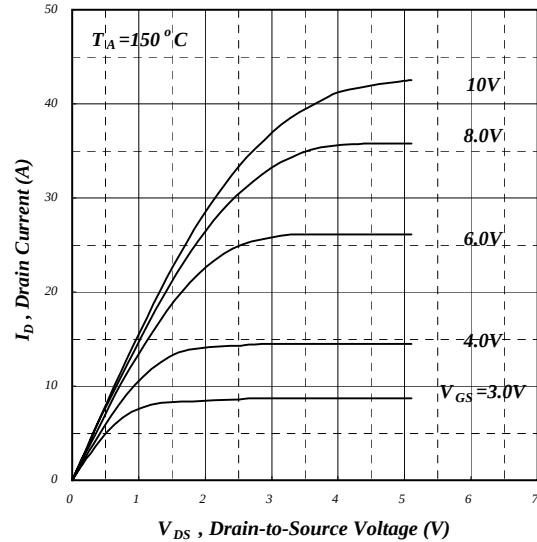


Fig 2. Typical Output Characteristics

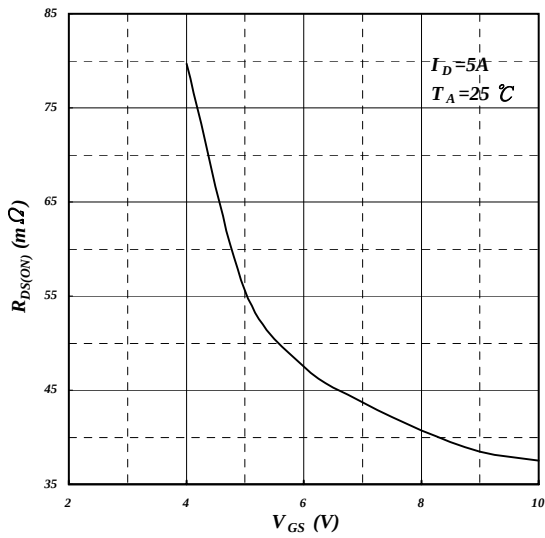


Fig 3. On-Resistance v.s. Gate Voltage

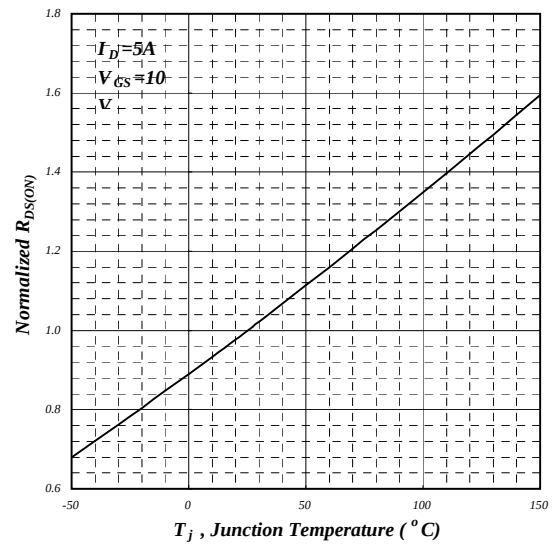


Fig 4. Normalized On-Resistance v.s. Junction Temperature



N-Channel

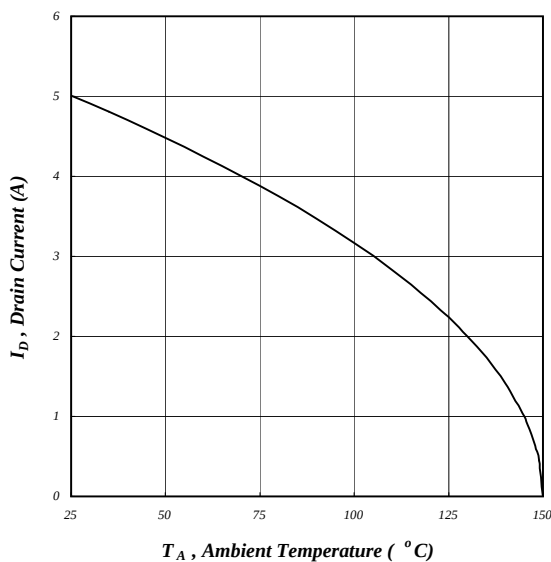


Fig 5. Maximum Drain Current v.s. Case Temperature

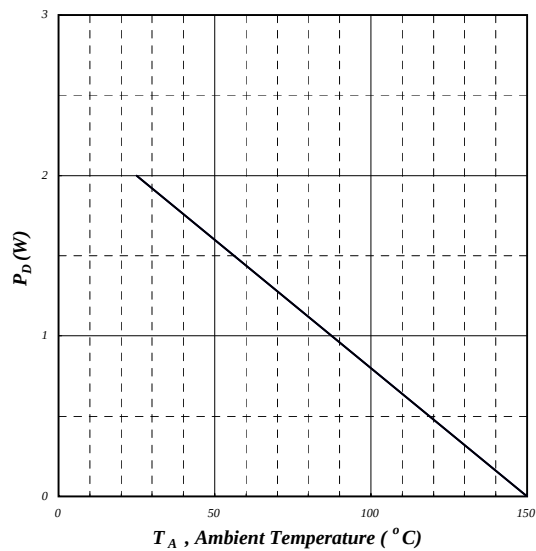


Fig 6. Typical Power Dissipation

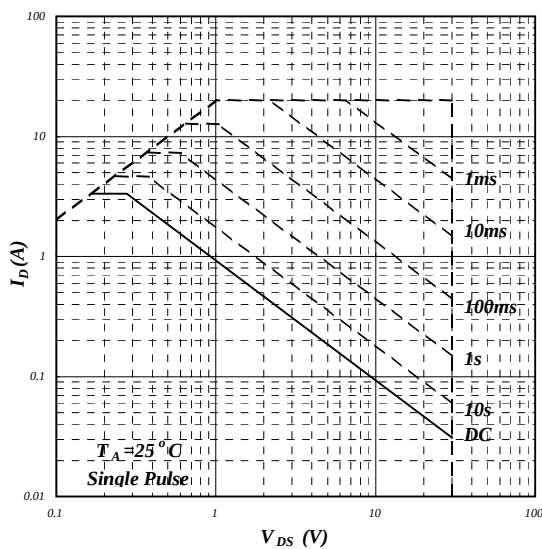


Fig 7. Maximum Safe Operating Area

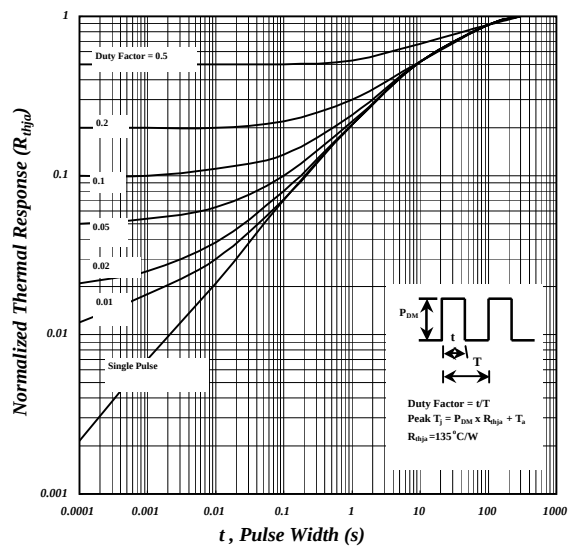
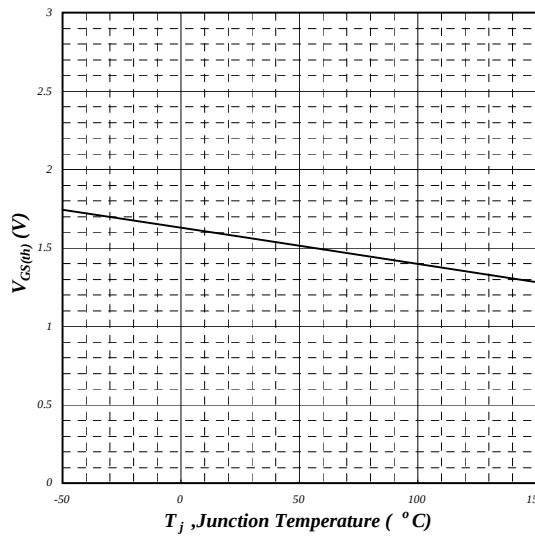
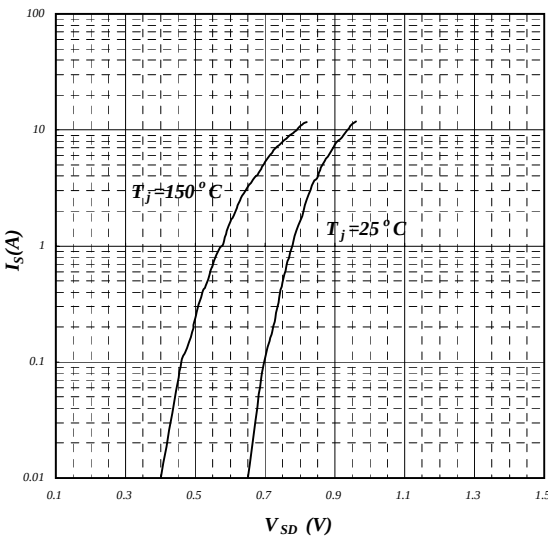
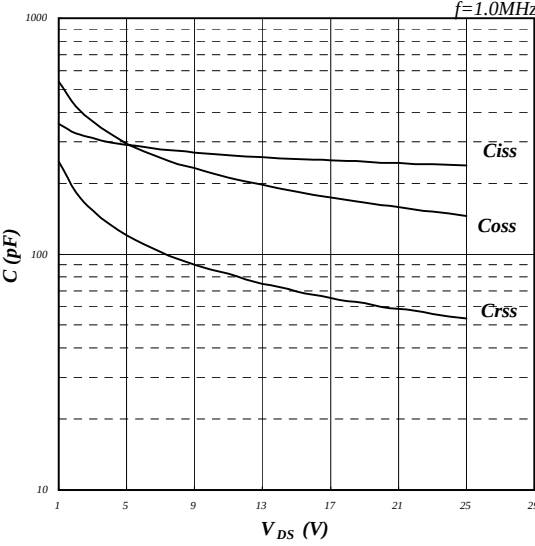
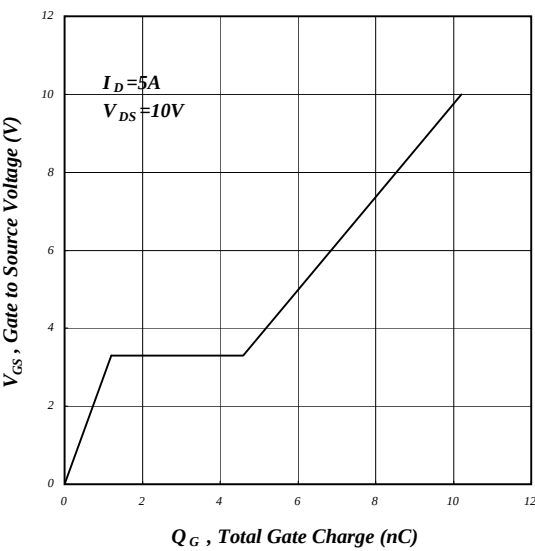


Fig 8. Effective Transient Thermal Impedance



N-Channel





N-Channel

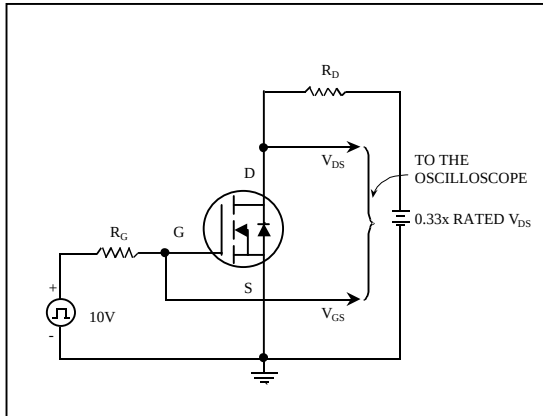


Fig 13. Switching Time Circuit

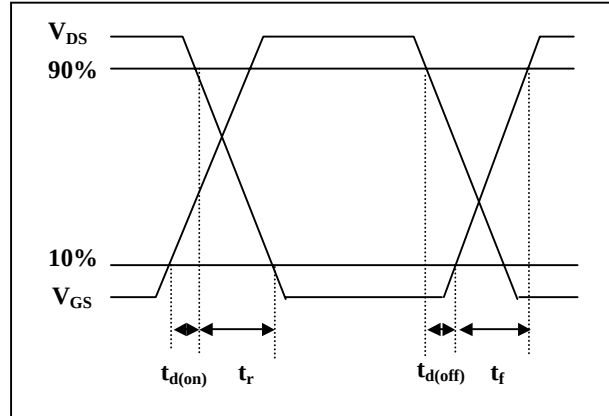


Fig 14. Switching Time Waveform

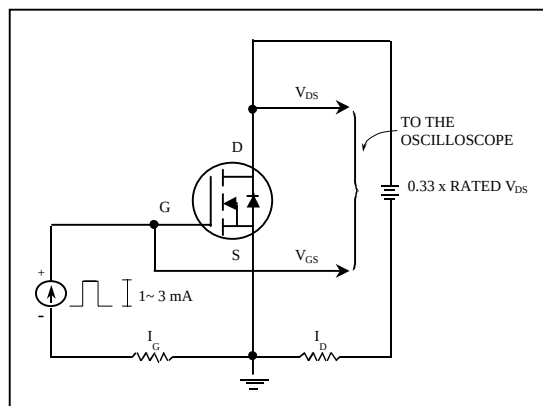


Fig 15. Gate Charge Circuit

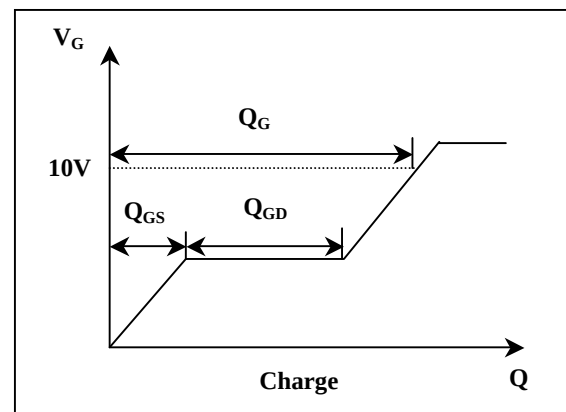


Fig 16. Gate Charge Waveform

P-Channel

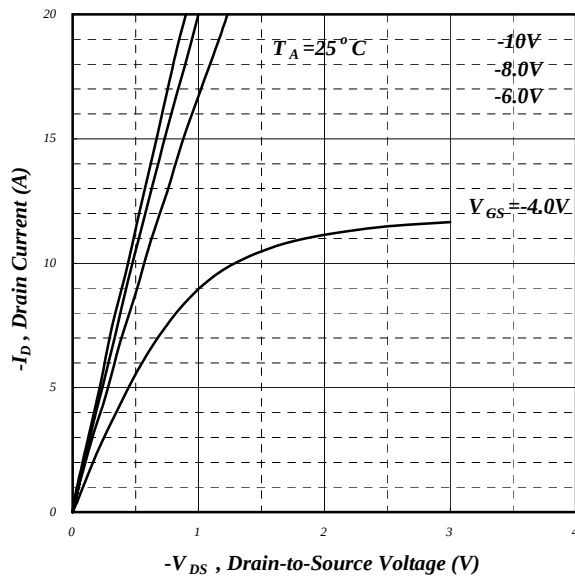


Fig 1. Typical Output Characteristics

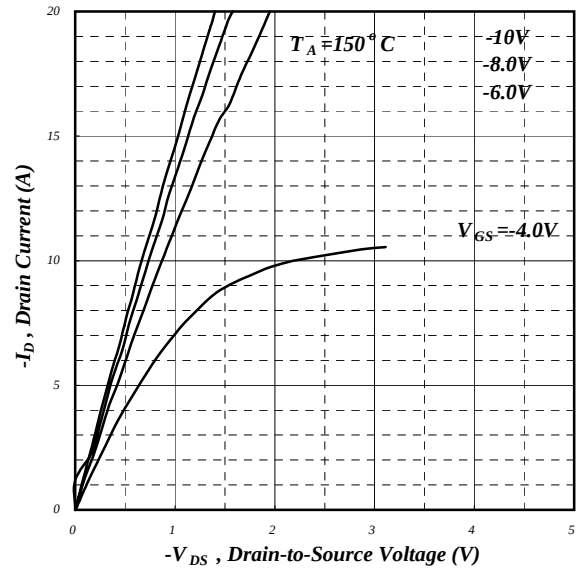


Fig 2. Typical Output Characteristics

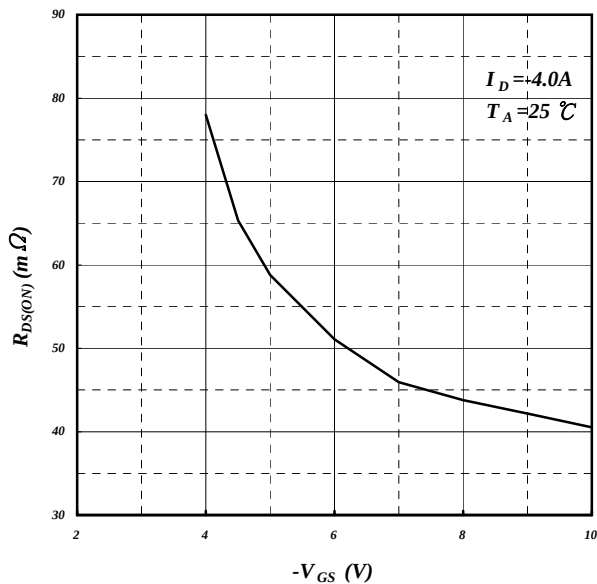


Fig 3. On-Resistance v.s. Gate Voltage

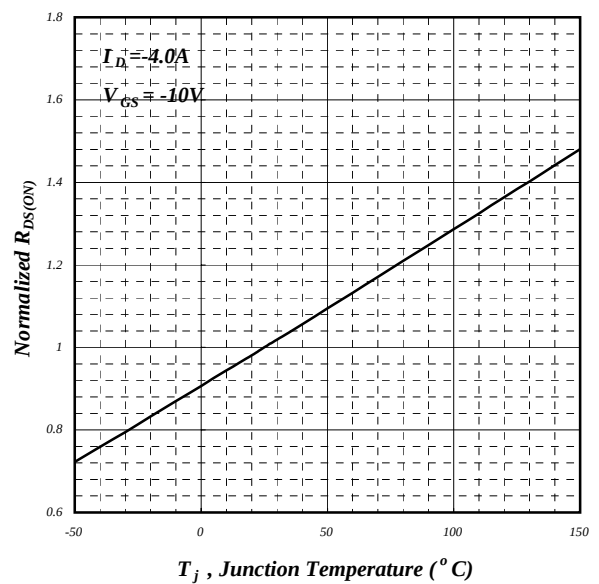


Fig 4. Normalized On-Resistance v.s. Junction Temperature



P-Channel

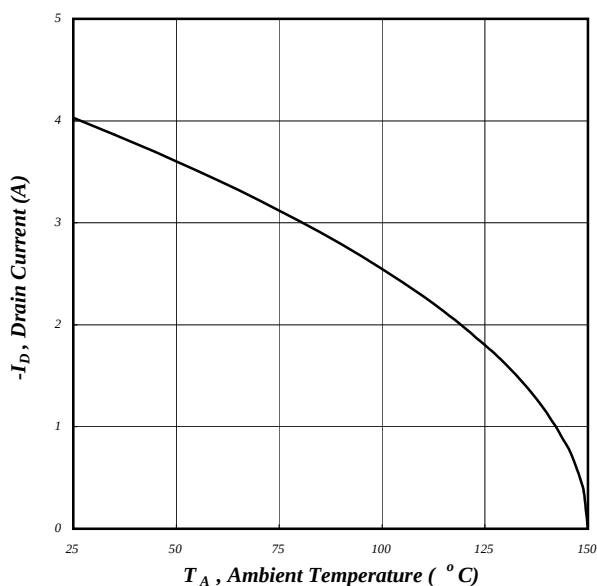


Fig 5. Maximum Drain Current v.s. Case Temperature

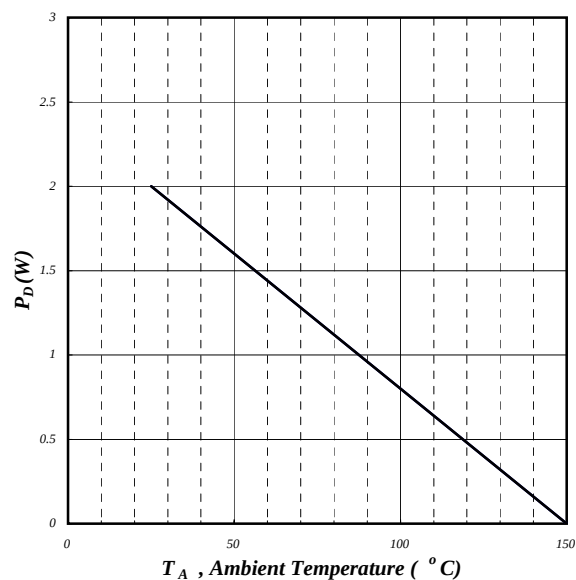


Fig 6. Typical Power Dissipation

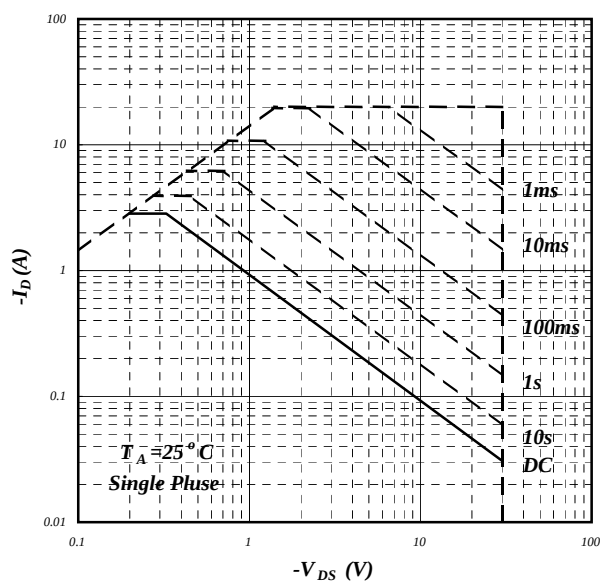


Fig 7. Maximum Safe Operating Area

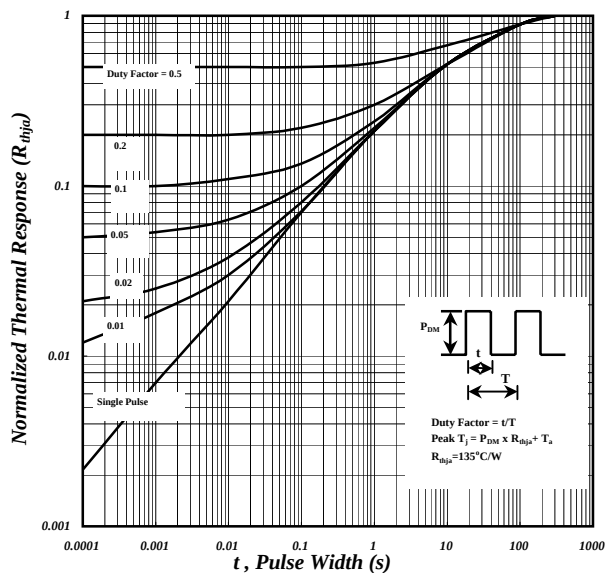


Fig 8. Effective Transient Thermal Impedance



P-Channel

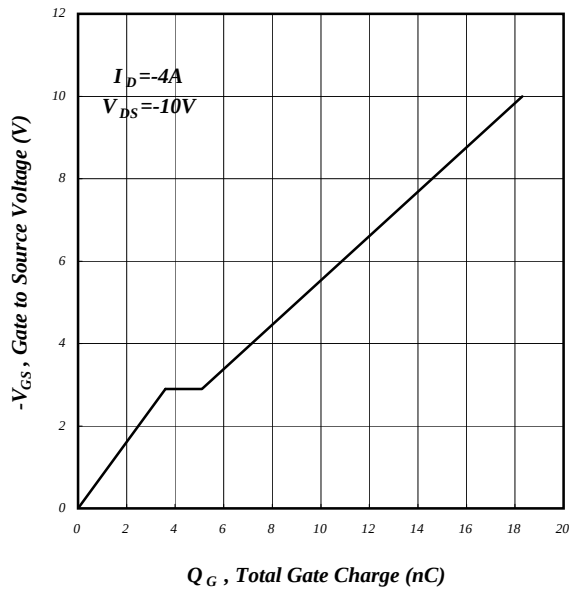


Fig 9. Gate Charge Characteristics

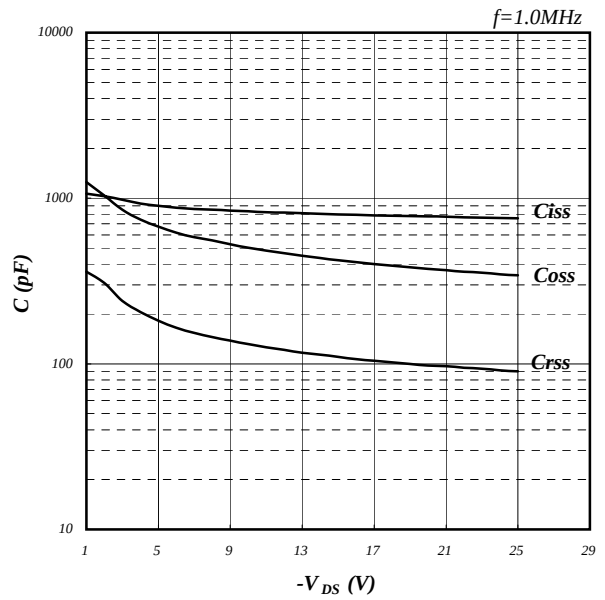


Fig 10. Typical Capacitance Characteristics

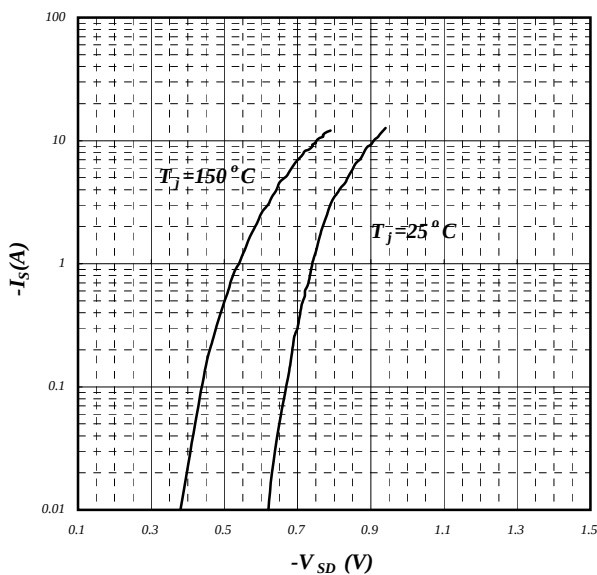


Fig 11. Forward Characteristic of Reverse Diode

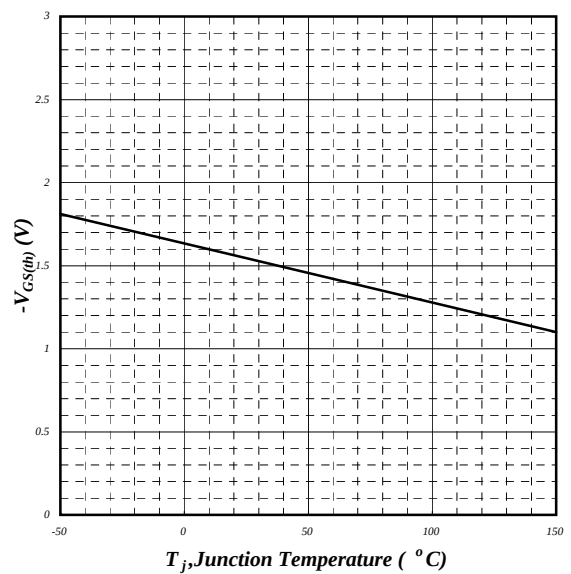


Fig 12. Gate Threshold Voltage v.s. Junction Temperature



P-Channel

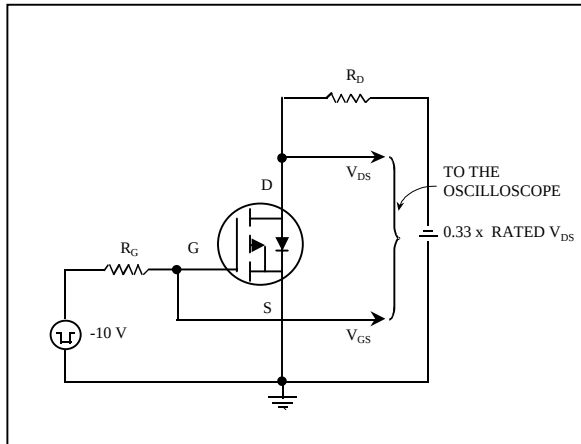


Fig 13. Switching Time Circuit

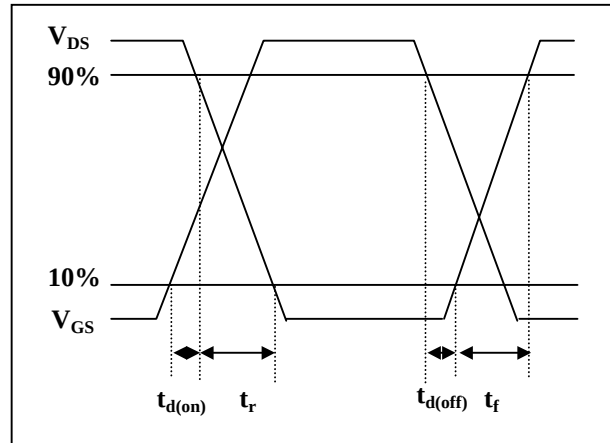


Fig 14. Switching Time Waveform

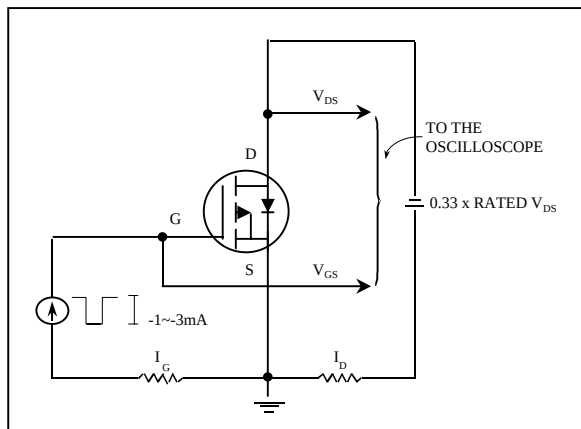


Fig 15. Gate Charge Circuit

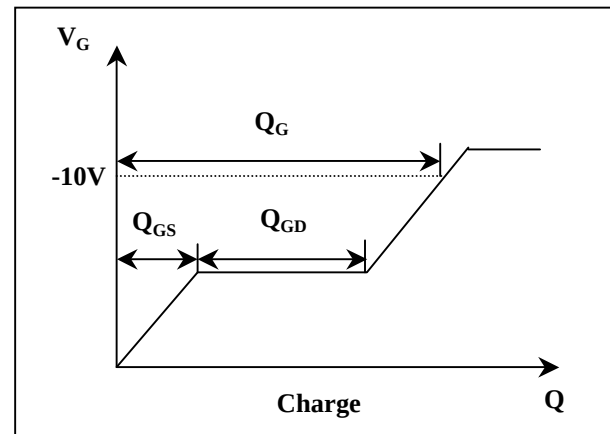


Fig 16. Gate Charge Waveform