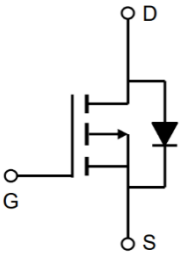
AP50P02BDF

-20V P-Channel Enhancement Mode MOSFET

Description

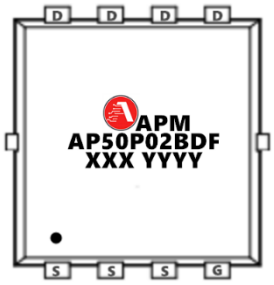
The AP50P02BDF uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

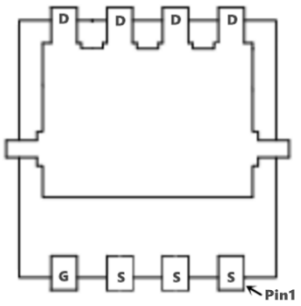


General Features

V_{DS} = -20V I_D =-50A

$R_{DS(ON)}$ < 8.5mΩ @ V_{GS}=4.5V **(Type：6.3mΩ)**



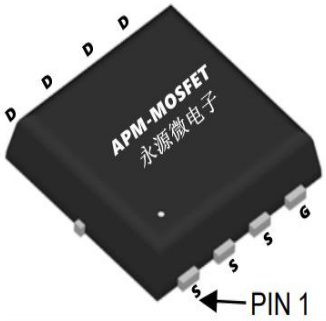


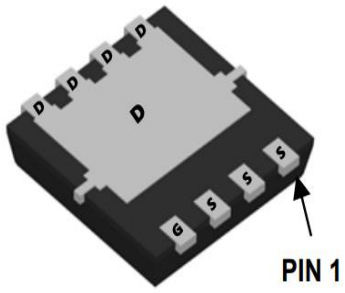
Application

Battery protection

Load switch

Uninterruptible power supply





Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP50P02BDF	PDFN3*3-8L	AP50P02BDF XXX YYYY	5000

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Rating	Units
VDS	Drain-Source Voltage	-20	V
VGS	Gate-Source Voltage	±12	V
I_D@T_C=25℃	Continuous Drain Current, V_{GS} @ -4.5V[1]	-50	A
I_D@T_C=70℃	Continuous Drain Current, V_{GS} @ -4.5V[1]	-36	A
IDM	Pulsed Drain Current[2]	-240	A
P_D@T_C=25℃	Total Power Dissipation[3]	70	W
P_D@T_C=70℃	Total Power Dissipation[3]	3.5	W
TSTG	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃
RθJA	Thermal Resistance Junction-Ambient [1]	62.5	℃/W
RθJC	Thermal Resistance Junction-Case[1]	2.1	℃/W

Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V(BR)DSS	Drain-Source Breakdown Voltage	V_{GS}=0V,I_D= -250μA	-20	-	-	V
IDSS	Zero Gate Voltage Drain Current	V_{DS} = -20V, V_{GS} = 0V,	-	-	-1	μA
IGSS	Gate to Body Leakage Current	V_{DS} =0V, V_{GS} = ±12V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V_{DS}= V_{GS}, I_D= -250μA	-0.35	-0.65	-1.0	V
RDS(on)	Static Drain-Source on-Resistance note3	V_{GS} =-4.5V, I_D =-15A	-	6.3	8.5	mΩ
		V_{GS} =-2.5V, I_D =-12A	-	8.9	10	
C_{iss}	Input Capacitance	V_{DS} =-10V, V_{GS} =0V, f = 1.0MHz	-	4590	-	pF
Coss	Output Capacitance		-	505	-	pF
Crss	Reverse Transfer Capacitance		-	440	-	pF
Q_g	Total Gate Charge	V_{DS} =-10V, I_D =-15A, V_{GS} =-4.5V	-	46	-	nC
Q_{gs}	Gate-Source Charge		-	7.3	-	nC
Q_{gd}	Gate-Drain(“Miller”) Charge		-	10	-	nC
td(on)	Turn-on Delay Time	V_{DD} =-10V, I_D =-14A, R_{GEN}=2.7Ω, V_{GS} =-10V	-	8	-	ns
t_r	Turn-on Rise Time		-	59	-	ns
td(off)	Turn-off Delay Time		-	111	-	ns
t_f	Turn-off Fall Time		-	43	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	-60	A
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-240	A
VSD	Drain to Source Diode Forward Voltage	V_{GS} = 0V, I_S =-20A	-	-	-1.2	V
trr	Reverse Recovery Time	T_J=25℃,I_{SD}=-15A, V_{GS}=0V di/dt=-100A/μs	-	18	-	ns
Qrr	Reverse Recovery Charge		-	7.7	-	nC

Note :

1、The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3、The power dissipation is limited by 150℃ junction temperature

4、The data is theoretically the same as I D and I DM , in real applications , should be limited by total power dissipation.

Typical Characteristics

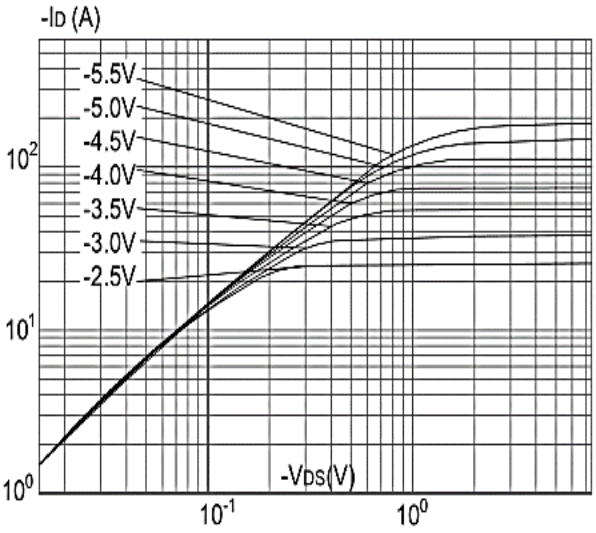


Figure1: Output Characteristics

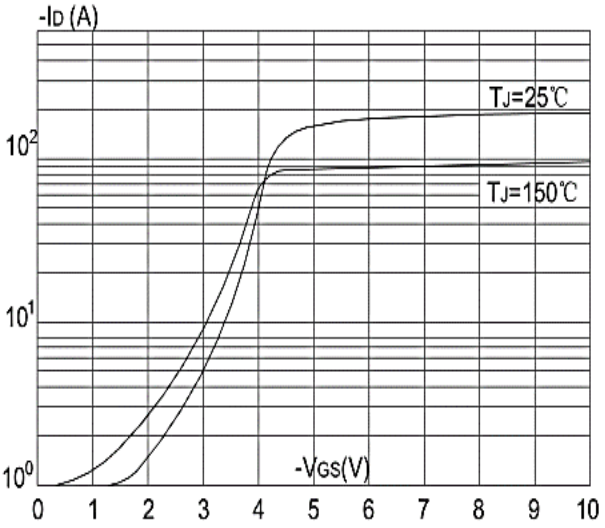


Figure 2: Typical Transfer Characteristics

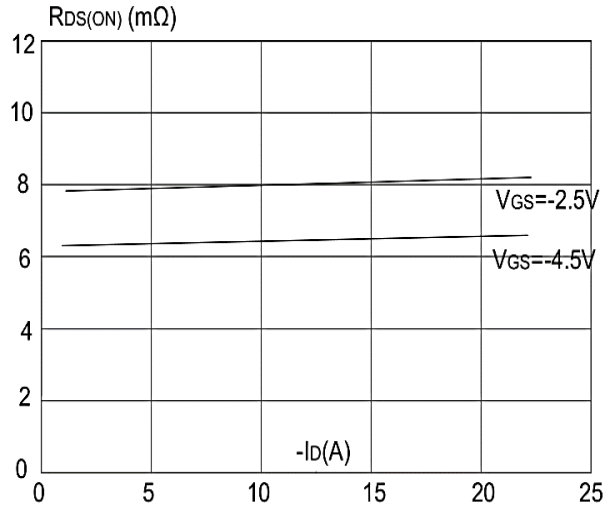


Figure 3:On-resistance vs. Drain Current

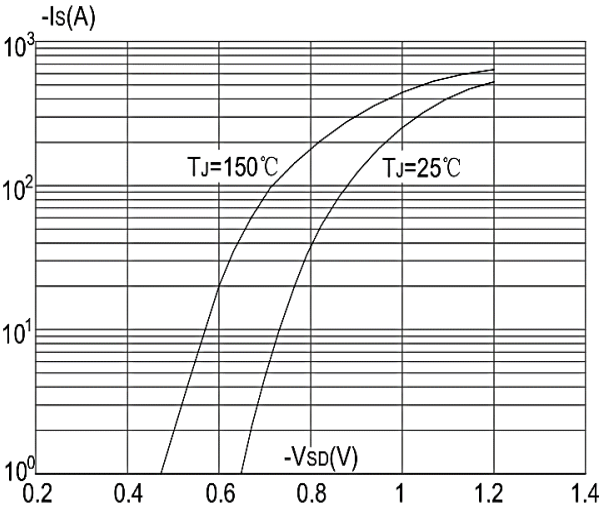


Figure 4: Body Diode Characteristics

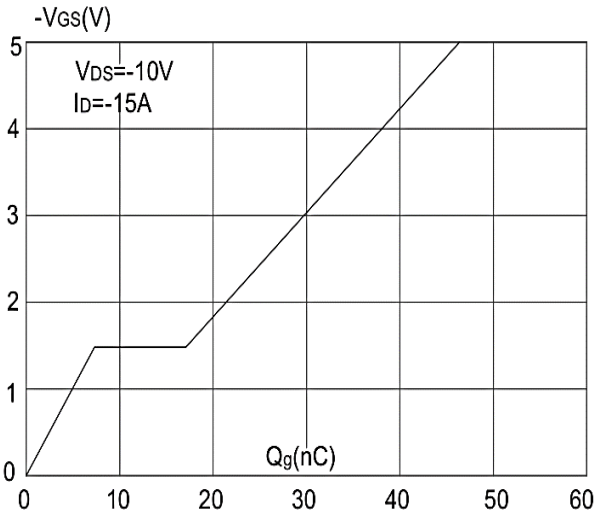


Figure 5: Gate Charge Characteristics

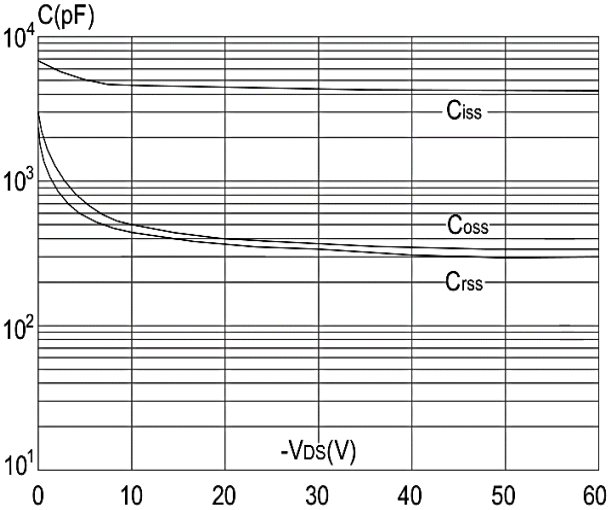


Figure 6: Capacitance Characteristics

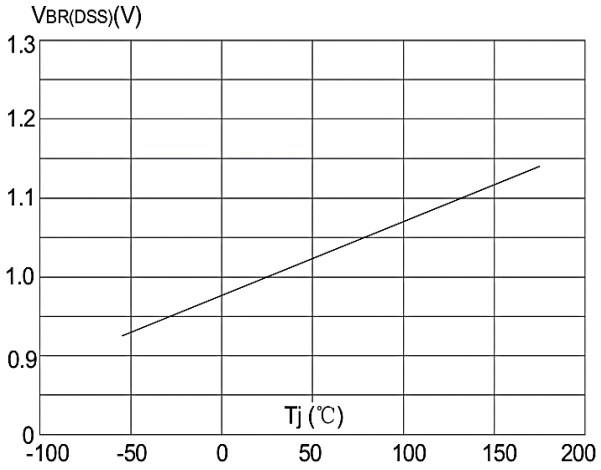


Figure 7: Normalized Breakdown Voltage vs Junction Temperature

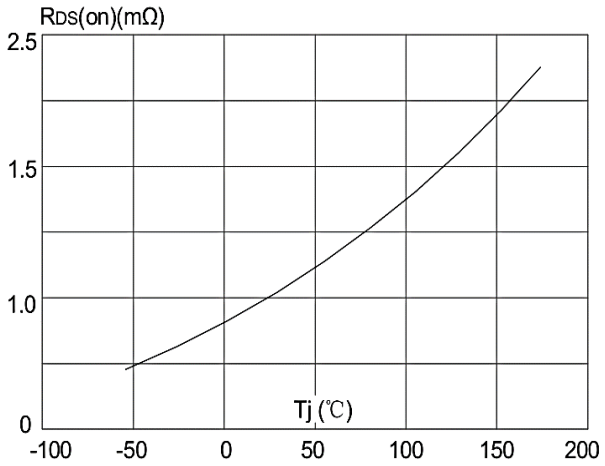


Figure 8: Normalized on Resistance vs. Junction Temperature

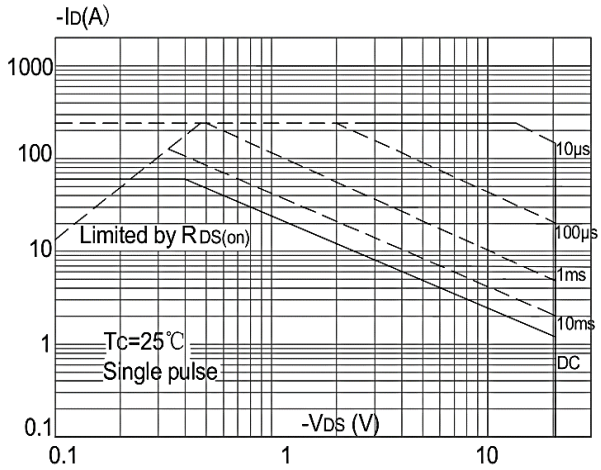


Figure 9: Maximum Safe Operating Area

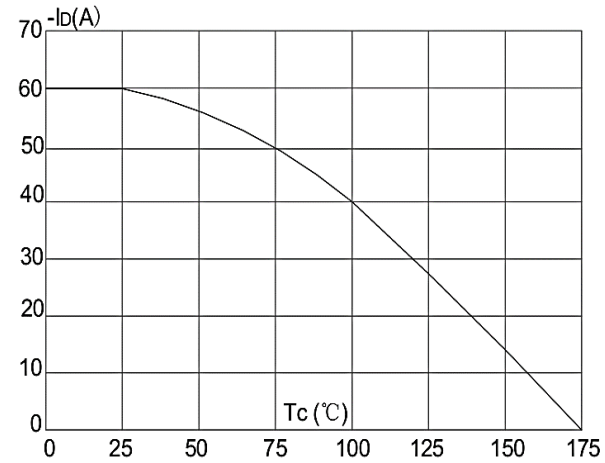


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

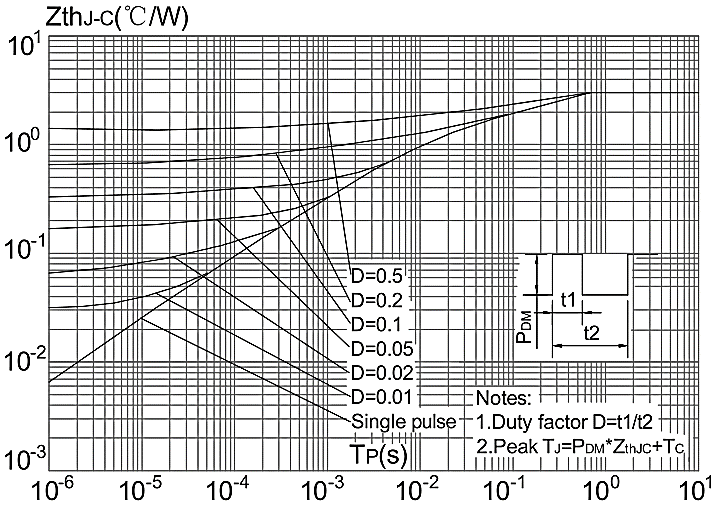
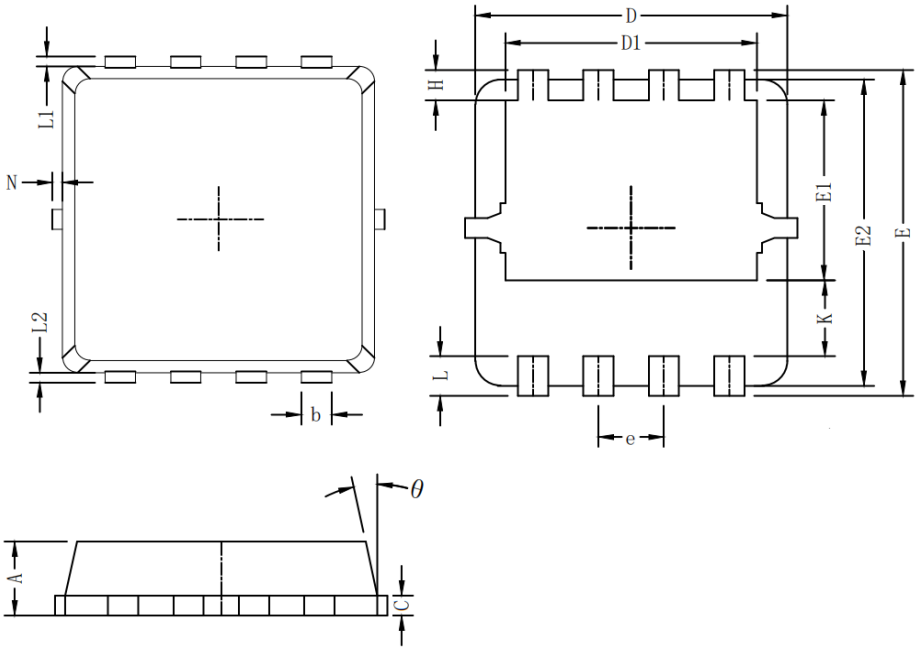


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambien

Package Mechanical Data-PDFN3X3-8L



Symbol	Dim in mm		
	Min	Typ	Max
A	0.6	0.75	0.9
b	0.2	0.3	0.4
C	0.15	0.2	0.25
D	3	3.1	3.2
D1	2.3	2.45	2.6
E	3.15	3.3	3.45
E1	1.43	1.73	1.93
E2	2.9	3.05	3.2
e	0.65BSC		
H	0.2	0.35	0.5
K	0.57	0.77	0.87
L	0.3	0.4	0.5
L1/L2	0.1REF		
θ	8°	10°	13°
N	0		0.15

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-20V P-Channel Enhancement Mode MOSFET

Edition	Date	Change
REV1.0	2023/4/13	Initial release