



**Advanced Power
Electronics Corp.**

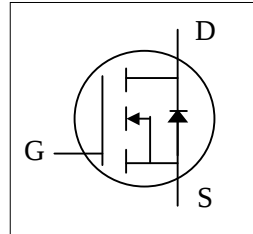
AP50T10GM-HF

Halogen-Free Product

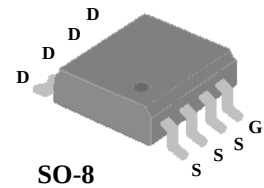
N-CHANNEL ENHANCEMENT MODE

POWER MOSFET

- ▼ Low Gate Charge
- ▼ Simple Drive Requirement
- ▼ Surface Mount Package
- ▼ Halogen Free & RoHS Compliant Product



BV_{DS}	100V
$R_{DS(ON)}$	30m Ω
I_D	6.5A



Description

AP50T10 series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The SO-8 package is widely preferred for all commercial-industrial surface mount applications using infrared reflow technique and suited for voltage conversion or switch applications.

Absolute Maximum Ratings@ $T_j=25^{\circ}\text{C}$ (unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_A=25^{\circ}\text{C}$	Drain Current, V_{GS} @ 10V ³	6.5	A
$I_D@T_A=70^{\circ}\text{C}$	Drain Current, V_{GS} @ 10V ³	5.2	A
I_{DM}	Pulsed Drain Current ¹	24	A
$P_D@T_A=25^{\circ}\text{C}$	Total Power Dissipation	2.5	W
T_{STG}	Storage Temperature Range	-55 to 150	$^{\circ}\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^{\circ}\text{C}$

Thermal Data

Symbol	Parameter	Value	Unit
Rthj-a	Maximum Thermal Resistance Junction-ambient ³	50	$^{\circ}\text{C}/\text{W}$



Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	100	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =6A	-	-	30	mΩ
		V _{GS} =5V, I _D =4A	-	-	70	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	1	-	3	V
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =6A	-	12	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =80V, V _{GS} =0V	-	-	25	uA
I _{GSS}	Gate-Source Leakage	V _{GS} = ±20V, V _{DS} =0V	-	-	±100	nA
Q _g	Total Gate Charge	I _D =6A	-	41	65	nC
Q _{gs}	Gate-Source Charge	V _{DS} =50V	-	6	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =10V	-	15.5	-	nC
t _{d(on)}	Turn-on Delay Time	V _{DS} =50V	-	10	-	ns
t _r	Rise Time	I _D =1A	-	9.5	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =3.3Ω	-	37	-	ns
t _f	Fall Time	V _{GS} =10V	-	19	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	1810	2940	pF
C _{oss}	Output Capacitance	V _{DS} =15V	-	250	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	190	-	pF
R _g	Gate Resistance	f=1.0MHz	-	1.7	3.4	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ²	I _S =1.9A, V _{GS} =0V	-	-	1.3	V
t _{rr}	Reverse Recovery Time	I _S =6A, V _{GS} =0V	-	40	-	ns
Q _{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	70	-	nC

Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test
- 3.Surface mounted on 1 in² copper pad of FR4 board, t ≤10sec ; 125°C/W when mounted on min. copper pad.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

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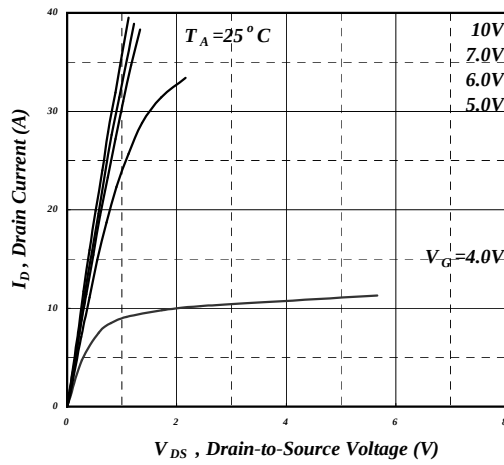


Fig 1. Typical Output Characteristics

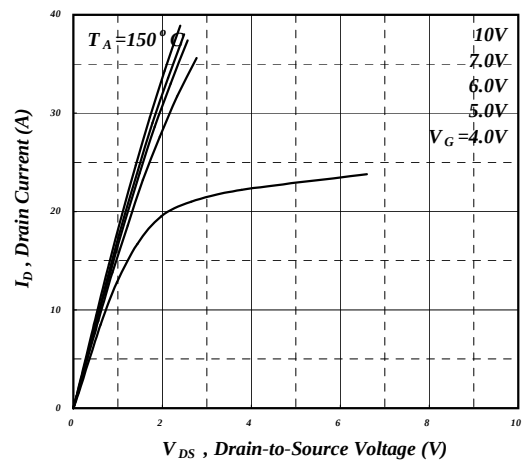


Fig 2. Typical Output Characteristics

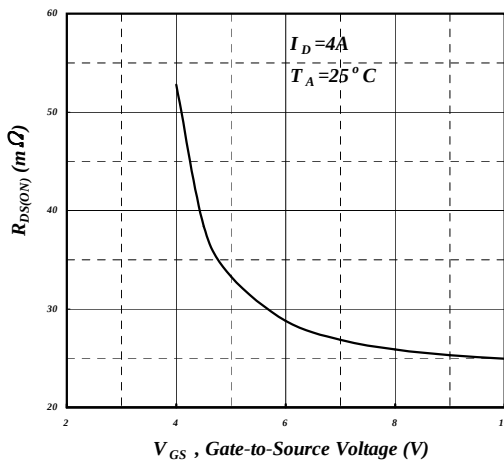


Fig 3. On-Resistance v.s. Gate Voltage

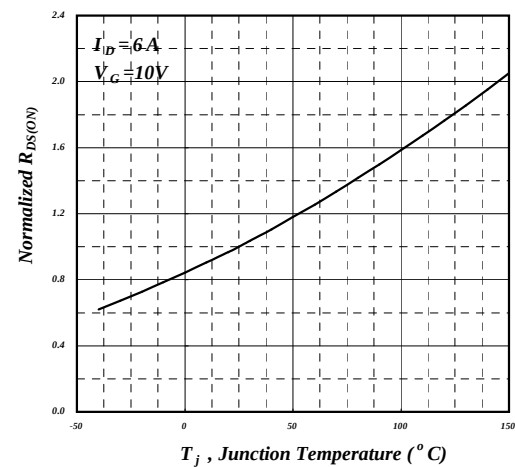


Fig 4. Normalized On-Resistance
v.s. Junction Temperature

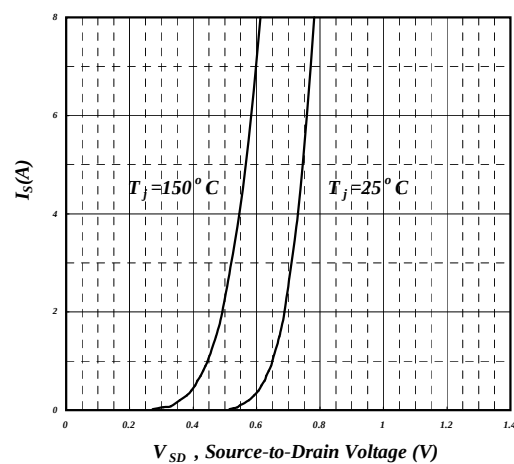


Fig 5. Forward Characteristic of
Reverse Diode

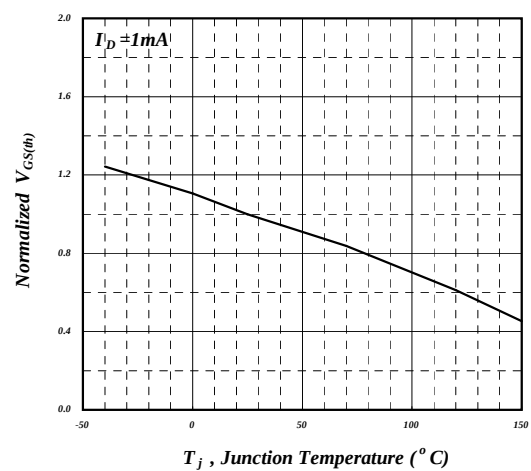


Fig 6. Gate Threshold Voltage v.s.
Junction Temperature

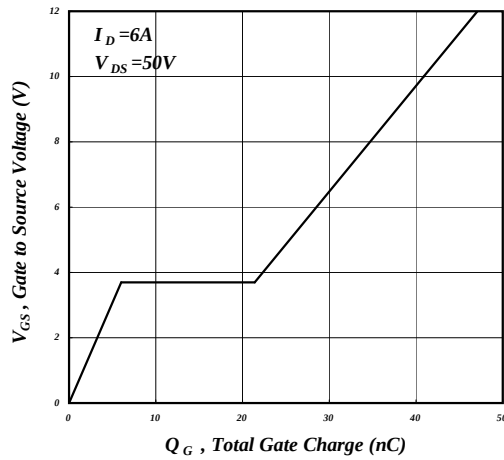


Fig 7. Gate Charge Characteristics

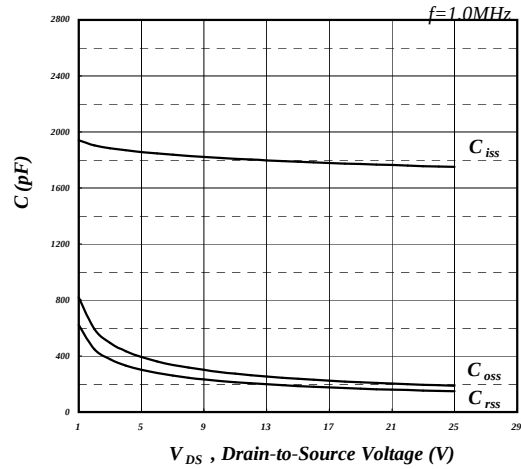


Fig 8. Typical Capacitance Characteristics

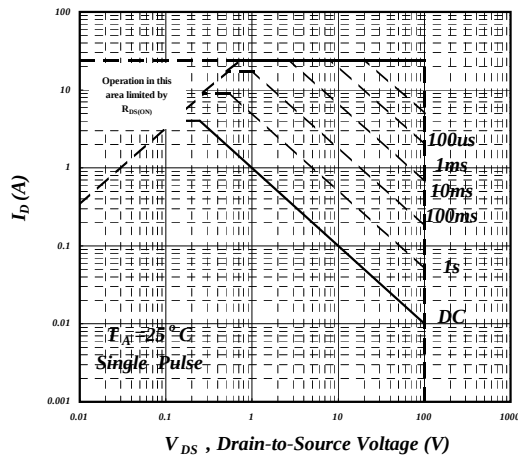


Fig 9. Maximum Safe Operating Area

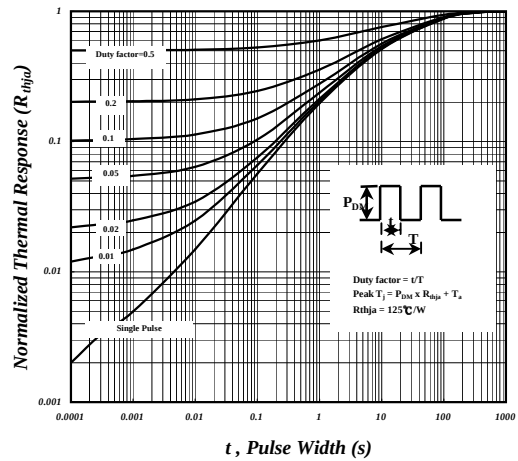


Fig 10. Effective Transient Thermal Impedance

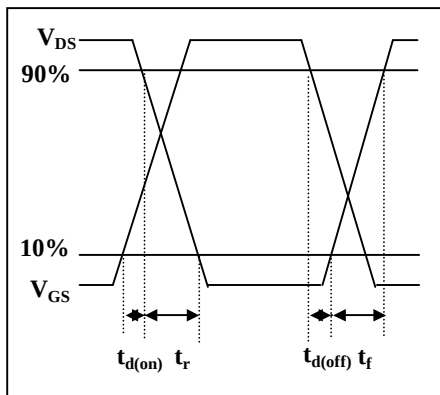


Fig 11. Switching Time Waveform

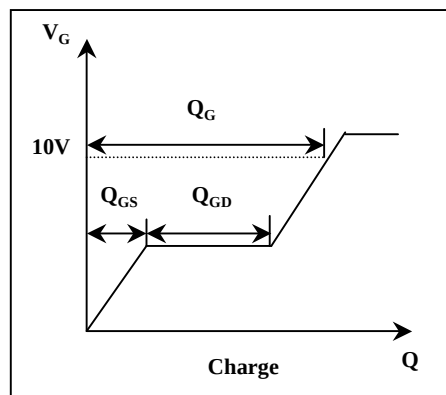


Fig 12. Gate Charge Waveform



MARKING INFORMATION

