AP562

3.3-3.8 GHz WiMAX 8W Power Amplifier

Product Features

- 3.3 – 3.8 GHz
- +39 dBm P1dB
- 12 dB Gain
- 2% EVM @ 30 dBm Pout
- +12 V Supply Voltage
- Lead-free/RoHS-compliant 5x6 mm power DFN package

Applications

- WiMAX CPE/BTS

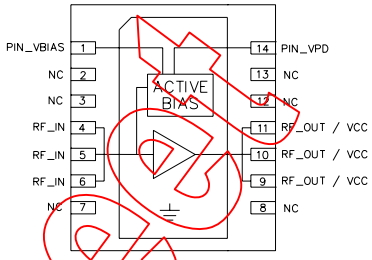
Product Description

The AP562 is a high dynamic range broadband power amplifier in a surface mount package. The single-stage amplifier has 12 dB gain, while being able to achieve high performance for 3.3–3.8 GHz WiMAX applications with up to 39 dBm of compressed 1dB power.

The AP562 uses a high reliability +12V InGaP/GaAs HBT process technology. The device incorporates proprietary bias circuitry to compensate for variations in linearity and current draw over temperature. The device does not require any negative bias voltage; an internal active bias allows the AP562 to operate directly off a commonly used +12V supply and has the added feature of a +5V power down control pin. RoHS-compliant 5x6mm DFN package is surface mountable to allow for low manufacturing costs to the end user.

The AP562 is targeted for use in a balanced or single ended configuration for WiMAX applications where high linearity and high power is required.

Functional Diagram



Specifications

Parameter	Units	Min	Typ	Max
Operational Bandwidth	MHz	3300		3800
Output Channel Power	dBm		+30	
Power Gain	dB		12	
Input Return Loss	dB		14	
Output Return Loss	dB		6.8	
Error Vector Magnitude	%		1.9	
Operating Current, Icc	mA		627	
Collector Efficiency	%		13	
Output P1dB	dBm		+39	
Quiescent Current, Icq	mA		400	
Vpd[4]	V		+5	
Vcc, Vbias	V		+12	

Notes:
1. Test conditions unless otherwise noted: T = 25ºC, Vpd = +5V, Vbias = Vcc = +12, Icq = 400mA at Pout = +30 dBm and f = 2.6 GHz.
2. Using an 802.16-2004 OFDMA, 64QAM-1/2, 1024-FFT, 20 symbols, 30 subchannels signal.
3. Switching speed: 50% TTL to 100/0% RF.
4. Vpd used for device power down. (low=RF off)
5. Capable of handling 10:1 VSWR @ 12 V_{DC}, 2.3-2.9 GHz, Pout = 30dBm.

Absolute Maximum Rating

Parameter	Rating
Pin max (CW into 50Ω load)	+33 dBm
Storage Temperature	-55 to +125 ºC
Max Junction Temperature, $T_{J,max}$	192 ºC
Thermal Resistance, Θ_{JC}	8.7 °C / W

Operation of this device above any of these parameters may cause permanent damage.

Ordering Information

Part No.	Description
AP562-F	WiMAX 12V 8W HBT Amplifier
AP562-PCB3500	3.4-3.6 GHz Fully Assembled Evaluation Board

Standard T/R size = 500 pieces on a 7" reel.

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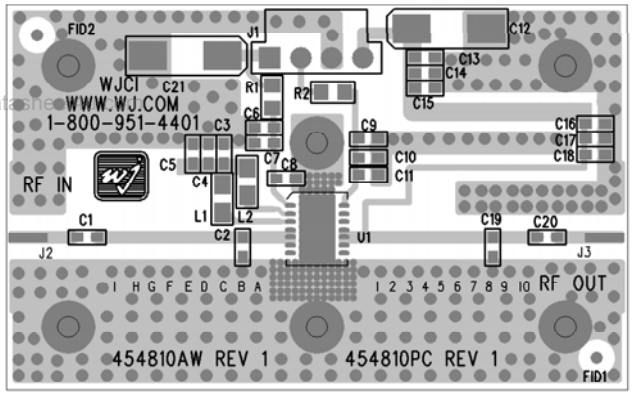
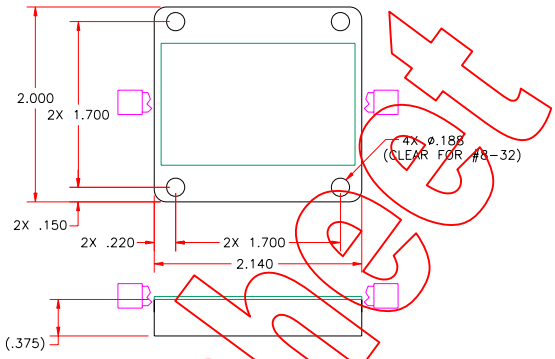
Application Circuit PC Board Layout



Circuit Board Material: 0.0147" Rogers Ultralam 2000, single layer, 1 oz copper, ε_r = 2.45, Microstrip line details: width = .042", spacing = .050"

Baseplate Configuration



Notes:
1. Please note that for reliable operation, the evaluation board will have to be mounted to a much larger heat sink during operation and in laboratory environments to dissipate the power consumed by the device. The use of a convection fan is also recommended in laboratory environments.
2. The area around the module underneath the PCB should not contain any soldermask in order to maintain good RF grounding.
3. For proper and safe operation in the laboratory, the power-on sequencing is recommended.

Evaluation Board Bias Procedure

Following bias procedure is recommended to ensure proper functionality of AP601 in a laboratory environment. The sequencing is not required in the final system application.

Bias:	Voltage (V)
Vcc	+12
Vbias	+12
Vpd	+5

Turn-on Sequence:

1. Attach input and output loads onto the evaluation board.
2. Turn on power supply Vcc = +12V.
3. Turn on power supply Vbias = +12V.
4. Turn on power supply Vpd = +5V.
5. Turn on RF power.

Turn-off Sequence:

1. Turn off RF power.
2. Turn off power supply Vpd = +5V.
3. Turn off power supply Vbias = +12V.
4. Turn off power supply Vcc = +12V.

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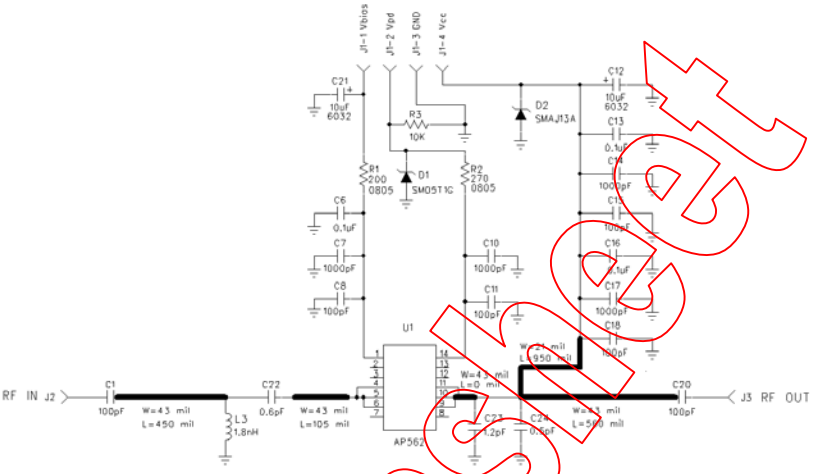
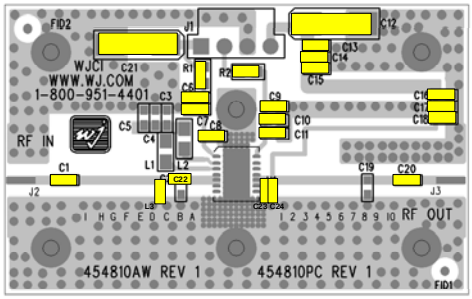
3400-3600 Application Circuit (AP562-PCB3500)

Typical O-FDMA Performance at 25°C

Frequency (MHz)	3400	3500	3600	Units
Channel Power	+30	+30	+30	dBm
Power Gain	12	12	11	dB
Input Return Loss	15	14	15	dB
Output Return Loss	6.1	6.8	5.7	dB
EVM	2.3	1.9	2.1	%
Operating Current, Icc	646	627	643	mA
Collector Efficiency	12.5	13	12.5	%
Output P1dB	39	39	39	dBm
Quiescent Current, Icq	400			mA
Vpd	+5			V
Vcc, Vbias	+12			V

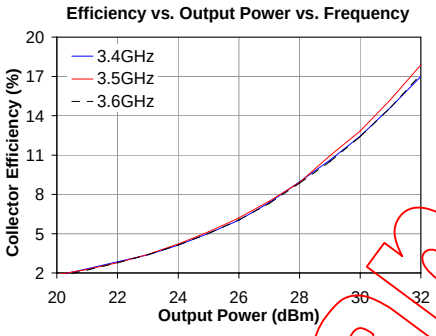


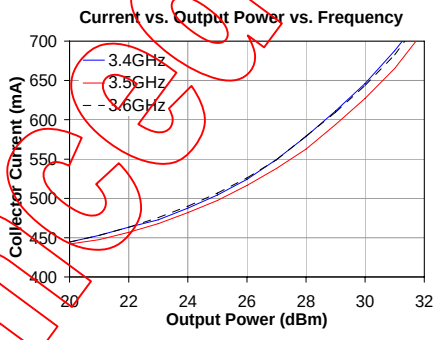


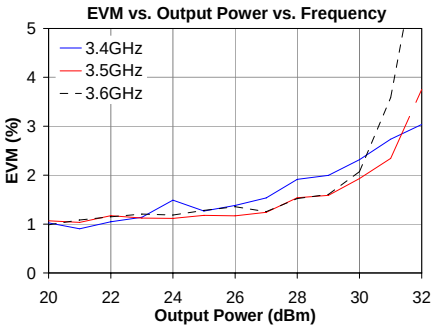
Notes:
1. The primary RF microstrip line is 50 Ω.
2. Components shown on the silkscreen but not on the schematic are not used.
3. The center of C23 is placed at 15mil from AP562 RFout pin.
4. The edge of C24 is placed right next to C23.
5. The center of C22 is placed at 135mil from AP562 RFin pin.
6. The edge of L3 is placed right next to C22.

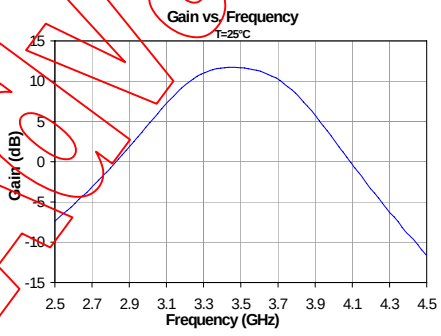
3400-3600 MHz Application Circuit Performance Plots

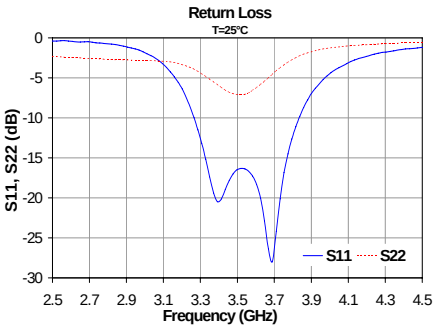
802.16-2004 O-FDMA, 64QAM-1/2, 1024-FFT, 20 symbols and 30 subchannels











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Parameter Measurement Information

Switching Speed Test

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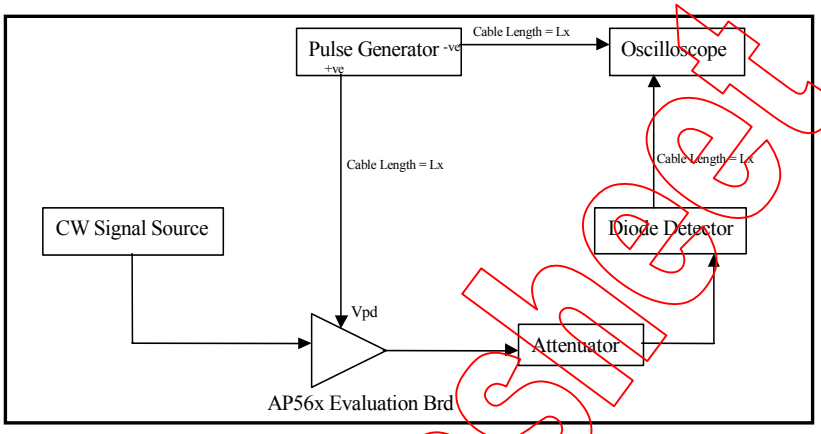
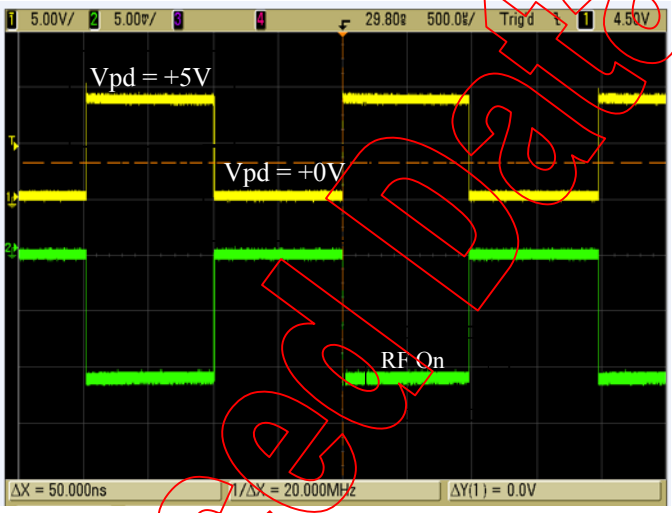
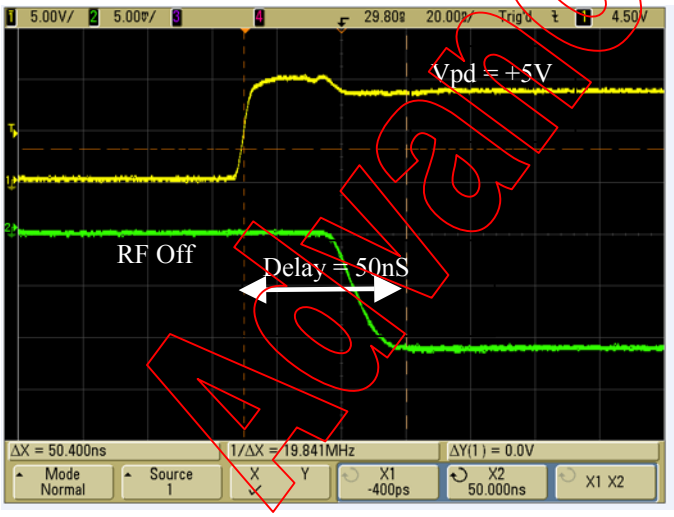
Test Conditions:

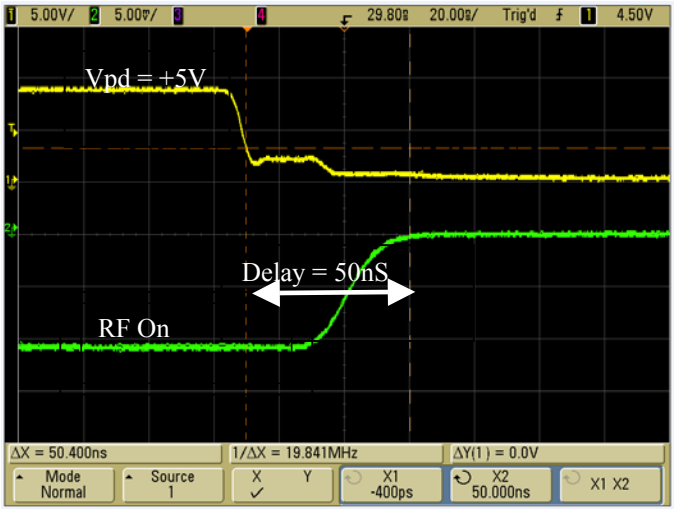
Vcc, Vbias = +12V at 25°C
Output Power = +30dBm @ 2.5 GHz
Rep Rate = 1 KHz, 50% duty cycle
Vpd amplitude = +5V
R2=200 ohms, C9=12pF
C10, C11 = DNP
Xtal Detector Voltage =15mV (square law)



Test Result Waveforms:







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Mechanical Information

This package is RoHS-compliant. The plating material on the pins is annealed matte tin over copper. It is compatible with both lead-free (maximum 260 °C reflow temperature) and leaded (maximum 245 °C reflow temperature) soldering processes.

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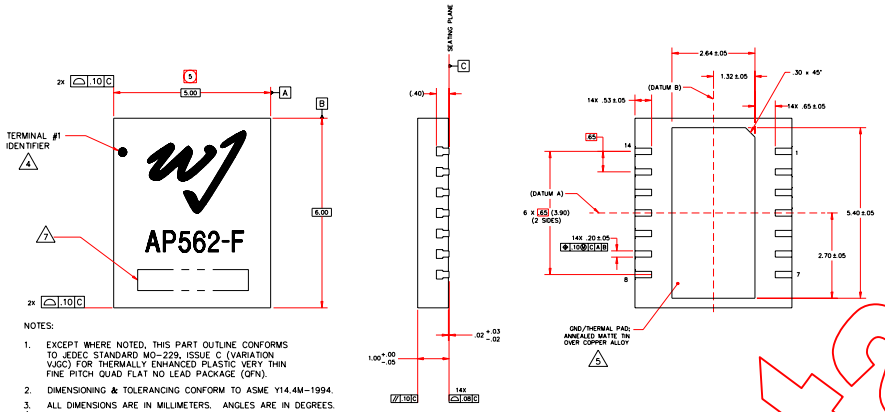
Outline Drawing



NOTES:

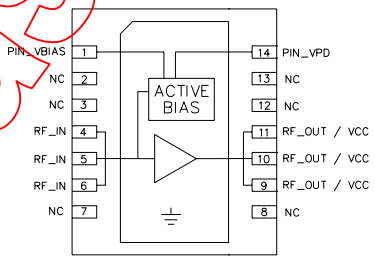
1. EXCEPT WHERE NOTED, THIS PART OUTLINE CONFORMS TO JEDEC STANDARD MO-229, ISSUE C (VARIATION VJGC) FOR THERMALLY ENHANCED PLASTIC VERY THIN FINE PITCH QUAD FLAT NO LEAD PACKAGE (QFN).
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.4M-1994.
3. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION CONFORM TO JESD 95-1 SPP-012.
5. COPLANARITY APPLIES TO THE EXPOSED GROUND/THERMAL PAD AS WELL AS THE TERMINALS.
6. ALPHA-NUMERIC LOT CODE.

Product Marking

The component will be laser marked with a "AP562-F" product label with an alphanumeric lot code on the top surface of the package.

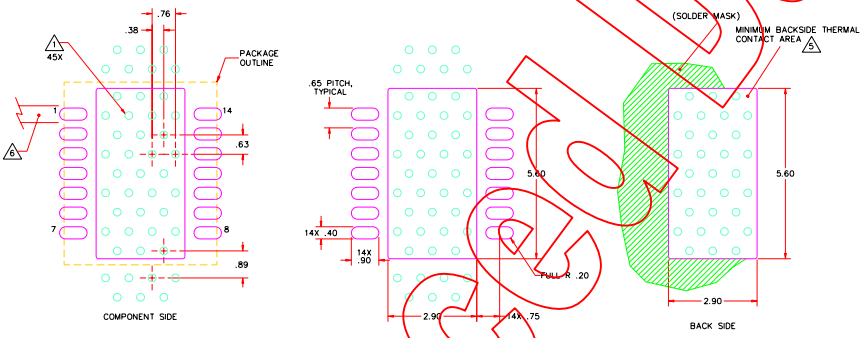
Tape and reel specifications for this part will be located on the website in the "Application Notes" section.

Functional Pin Layout



Pin	Function
1	PIN_VBIAS
2, 3, 7, 8, 12, 13	N/C
4, 5, 6	RF IN
9, 10, 11	RF Output / Vcc
14	PIN_VPD
Backside paddle	GND

Mounting Configuration / Land Pattern



NOTES:

1. GROUND/THERMAL VIAS ARE CRITICAL FOR THE PROPER PERFORMANCE OF THIS DEVICE. VIAS SHOULD USE A .35mm (#80/.0135") DIAMETER DRILL AND HAVE A FINAL PLATED THRU DIAMETER OF .25mm (.010").
2. ADD AS MUCH COPPER AS POSSIBLE TO INNER AND OUTER LAYERS NEAR THE PART TO ENSURE OPTIMAL THERMAL PERFORMANCE.
3. TO ENSURE RELIABLE OPERATION, DEVICE GROUND PADDLE-TO-GROUND PAD SOLDER JOINT IS CRITICAL.
4. ADD MOUNTING SCREWS NEAR THE PART TO FASTEN THE BOARD TO A HEATSINK. ENSURE THAT THE GROUND/THERMAL VIA REGION CONTACTS THE HEATSINK.
5. DO NOT PUT SOLDER MASK ON THE BACK SIDE OF THE PC BOARD IN THE REGION WHERE THE BOARD CONTACTS THE HEATSINK.
6. RF TRACE WIDTH DEPENDS UPON THE PC BOARD MATERIAL AND CONSTRUCTION.
7. USE 1 OZ. COPPER MINIMUM.
8. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
9. A HEATSINK UNDERNEATH THE AREA OF THE PCB FOR THE MOUNTED DEVICE IS STRICTLY REQUIRED FOR PROPER THERMAL OPERATION. DAMAGE TO THE DEVICE CAN OCCUR WITHOUT THE USE OF ONE.

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