



正基科技股份有限公司

## 產品規格書

### SPECIFICATION

PRODUCT NAME : AP6236

SPEC. NO. :                      REV : 1.8

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|----------|--------|----|----------|-----------|
|          | PM     | QA |          |           |
|          |        |    |          |           |

AMPAK

AP6236

WiFi + Bluetooth 4.2  
SIP Module Spec Sheet

# Revision History

| Date       | Revision Content                                           | Revised By | Version |
|------------|------------------------------------------------------------|------------|---------|
| 2017/06/15 | - Preliminary                                              | Richard    | 1.0     |
| 2017/09/01 | - Modify Recommended Reflow Profile                        | Richard    | 1.1     |
| 2018/02/07 | - Modify 2.4GHz support channel                            | Richard    | 1.2     |
| 2018/04/10 | - Modify Pin Assignments                                   | Richard    | 1.3     |
| 2018/07/19 | - Modify GPIO                                              | Ali        | 1.4     |
| 2018/08/20 | - Modify SDIO/gSPI strapping.<br>- Modify gSPI Mode timing | Richard    | 1.5     |
| 2018/09/10 | - Modify External LPO signal characteristics               | Richard    | 1.6     |
| 2018/09/13 | - Modify operating temperature range                       | Ali        | 1.7     |
| 2018/12/10 | - Modify 4.2 Voltages<br>- Modify PCM timing Diagram       | Ali        | 1.8     |

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# 1. Introduction

AMPAK Technology would like to announce a low-cost and low-power consumption module which has all of the WiFi, Bluetooth functionalities. The highly integrated module makes the possibilities of web browsing, VoIP, Bluetooth headsets functional applications and other applications. With seamless roaming capabilities and advanced security, also could interact with different vendors' 802.11b/g/n Access Points in the wireless LAN.

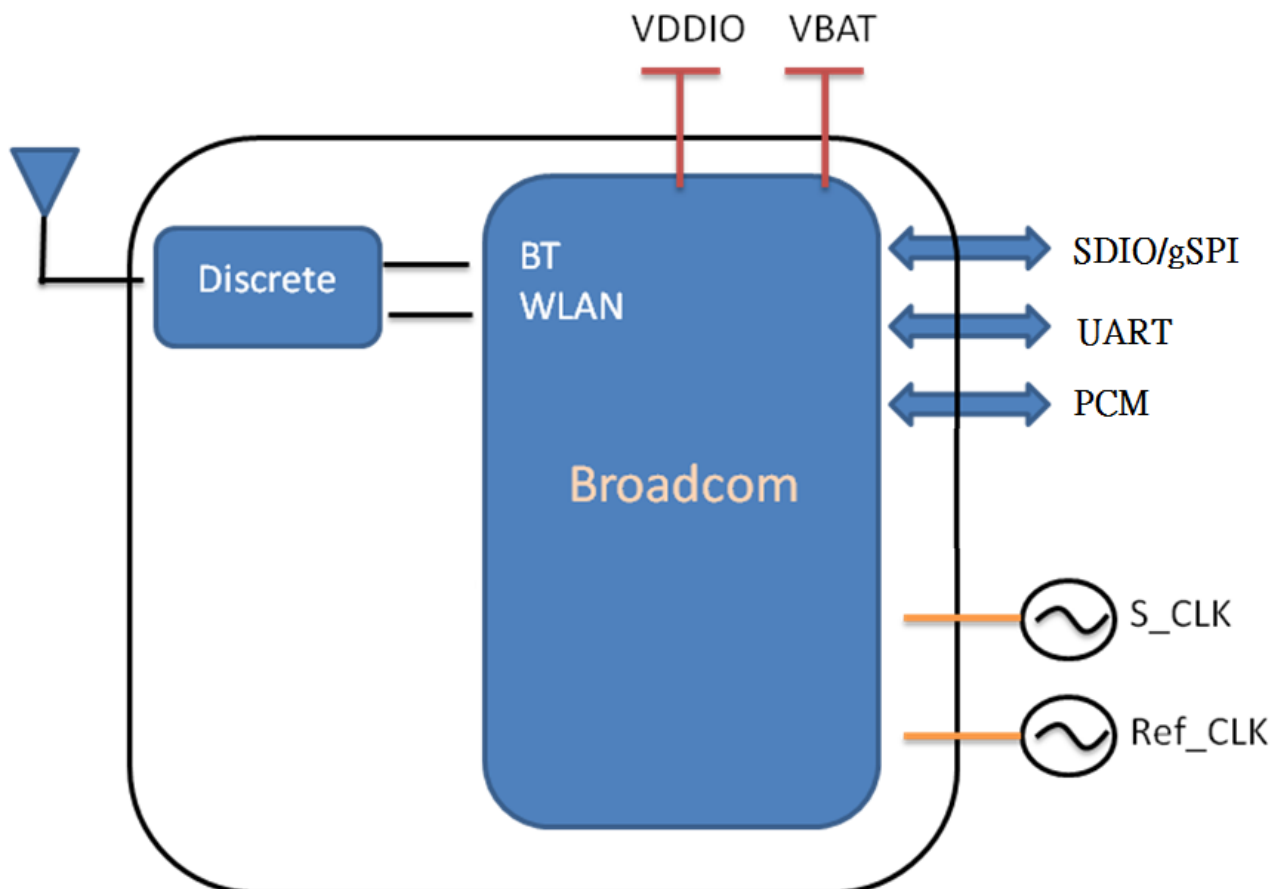
The wireless module complies with IEEE 802.11 b/g/n standard and it can achieve up to a speed of 72.2Mbps with single stream in 802.11n draft, 54Mbps as specified in IEEE 802.11g, or 11Mbps for IEEE 802.11b to connect to the wireless LAN. The integrated module provides SDIO / gSPI interface for WiFi, UART / PCM interface for Bluetooth.

This compact module is a total solution for a combination of WiFi + BT technologies. The module is specifically developed for Smart phones and Portable devices.

## 2. Features

- 802.11b/g/n single-band radio
- Bluetooth V4.2(HS) with integrated Class 1.5 PA and Low Energy (BLE) support
- Concurrent Bluetooth, WLAN operation
- Simultaneous BT/WLAN receive with single antenna
- WLAN host interface options:
  - SDIO v2.0 — up to 50 MHz clock rate
  - gSPI — up to 50 MHz clock rate
- BT host digital interface:
  - UART (up to 4 Mbps)
- IEEE Co-existence technologies are integrated die solution
- ECI — enhanced coexistence support, ability to coordinate BT SCO transmissions around WLAN receives

A simplified block diagram of the module is depicted in the figure below.



# 3. Deliverables

## 3.1 Deliverables

The following products and software will be part of the product.

- Module with packaging
- Evaluation Kits
- Software utility for integration, performance test.
- Product Datasheet.
- Agency certified pre-tested report with the adapter board.

## 3.2 Regulatory certifications

The product delivery is a pre-tested module, without the module level certification. For module approval, the platform's antennas are required for the certification.

## 4. General Specification

### 4.1 General Specification

|                                      |                                        |
|--------------------------------------|----------------------------------------|
| Model Name                           | AP6236                                 |
| Product Description                  | Support WiFi/Bluetooth functionalities |
| Dimension                            | L x W x H: 12 x 12 x 1.5 (typical) mm  |
| WiFi Interface                       | SDIOV2.0/gSPI                          |
| BT Interface                         | UART / PCM                             |
| Operating temperature <sup>a,b</sup> | -30°C to 85°C                          |
| Storage temperature                  | -40°C to 105°C                         |
| Humidity                             | Operation : less than 85%              |
|                                      | Storage : less than 60%                |

a. The operating temperature 65 to 85°C is feasible at conditional environment. Please examine the reliability on final product.

b. Functionality is guaranteed across this range of temperature. Optimal RF performance as specified in the data sheet, however, is guaranteed only for -10°C to 55°C.

### 4.2 Voltages

#### 4.2.1 Absolute Maximum Ratings

| Symbol    | Description                         | Min. | Max. | Unit |
|-----------|-------------------------------------|------|------|------|
| VBAT      | Input supply Voltage                | -0.5 | 4.5  | V    |
| WL_VIO_SD | Digital/Bluetooth/SDIO/ I/O Voltage | -0.5 | 3.6  | V    |

#### 4.2.2 Recommended Operating Rating

The module requires two power supplies: VBAT and VDDIO.

|                       | Min. | Typ. | Max. | Unit  |
|-----------------------|------|------|------|-------|
| Operating Temperature | -30  | 25   | 85   | deg.C |
| VBAT                  | 3.0  | 3.3  | 3.8  | V     |
| VDDIO                 | 1.7  | 3.3  | 3.6  | V     |

The module requires two power supplies: other Digital I/O Pins.

| For VDDIO=1.8V     | Min.       | Max.       | Unit |
|--------------------|------------|------------|------|
| VIL/VIH            | 0.35×VDDIO | 0.65×VDDIO | V    |
| VOL/VOH output@2mA | 0.4        | VDDIO-0.4  | V    |
| For VDDIO=3.3V     | Min.       | Max.       | Unit |
| VIL/VIH            | 0.80       | 2          | V    |
| VOL/VOH output@2mA | 0.4        | VDDIO-0.4  | V    |

## 5. WiFi RF Specification

### 5.1 2.4GHz RF Specification

Conditions : VBAT=3.3V ; VDDIO=3.3V ; Temp:25°C

| Feature                                        | Description                                                                  |
|------------------------------------------------|------------------------------------------------------------------------------|
| WLAN Standard                                  | IEEE 802.11b/g/n, WiFi compliant                                             |
| Frequency Range                                | 2.400 GHz ~ 2.4835 GHz (2.4 GHz ISM Band)                                    |
| Number of Channels                             | 2.4GHz : Ch1 ~ Ch13                                                          |
| Modulation                                     | 802.11b : DQPSK, DBPSK, CCK<br>802.11 g/n : OFDM /64-QAM, 16-QAM, QPSK, BPSK |
| Output Power                                   | 802.11b /11Mbps : 16 dBm ± 1.5 dB @ EVM ≤ -9dB                               |
|                                                | 802.11g /54Mbps : 15 dBm ± 1.5 dB @ EVM ≤ -25dB                              |
|                                                | 802.11n /65Mbps : 14 dBm ± 1.5 dB @ EVM ≤ -27dB                              |
| Receive Sensitivity<br>(11n,20MHz)<br>@10% PER | - MCS=0 PER @ -88 dBm, +/- 2dB                                               |
|                                                | - MCS=1 PER @ -86 dBm, +/- 2dB                                               |
|                                                | - MCS=2 PER @ -84 dBm, +/- 2dB                                               |
|                                                | - MCS=3 PER @ -82 dBm, +/- 2dB                                               |
|                                                | - MCS=4 PER @ -79 dBm, +/- 2dB                                               |
|                                                | - MCS=5 PER @ -75 dBm, +/- 2dB                                               |
|                                                | - MCS=6 PER @ -73 dBm, +/- 2dB                                               |
|                                                | - MCS=7 PER @ -71 dBm, +/- 2dB                                               |
| Receive Sensitivity (11g)<br>@10% PER          | - 6Mbps PER @ -89 dBm, +/- 2dB                                               |
|                                                | - 9Mbps PER @ -87 dBm, +/- 2dB                                               |
|                                                | - 12Mbps PER @ -86 dBm, +/- 2dB                                              |
|                                                | - 18Mbps PER @ -84 dBm, +/- 2dB                                              |

|                                      |                                                          |
|--------------------------------------|----------------------------------------------------------|
|                                      | - 24Mbps PER @ -82 dBm, +/- 2dB                          |
|                                      | - 36Mbps PER @ -79 dBm, +/- 2dB                          |
|                                      | - 48Mbps PER @ -76 dBm, +/- 2dB                          |
|                                      | - 54Mbps PER @ -73 dBm, +/- 2dB                          |
| Receive Sensitivity (11b)<br>@8% PER | - 1Mbps PER @ -95 dBm, +/- 2dB                           |
|                                      | - 2Mbps PER @ -92 dBm, +/- 2dB                           |
|                                      | - 5.5Mbps PER @ -90 dBm, +/- 2dB                         |
|                                      | - 11Mbps PER @ -88 dBm, +/- 2dB                          |
| Data Rate                            | 802.11b : 1, 2, 5.5, 11Mbps                              |
|                                      | 802.11g : 6, 9, 12, 18, 24, 36, 48, 54Mbps               |
| Data Rate<br>(20MHz ,Long GI,800ns)  | 802.11n: 6.5, 13, 19.5, 26, 39, 52, 58.5, 65Mbps         |
| Data Rate<br>(20MHz ,short GI,400ns) | 802.11n : 7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65,72.2Mbps |
| Maximum Input Level                  | 802.11b : -10 dBm                                        |
|                                      | 802.11g/n : -20 dBm                                      |
| Antenna Reference                    | Small antennas with 0~2 dBi peak gain                    |

# 6. Bluetooth Specification

## 6.1 Bluetooth Specification

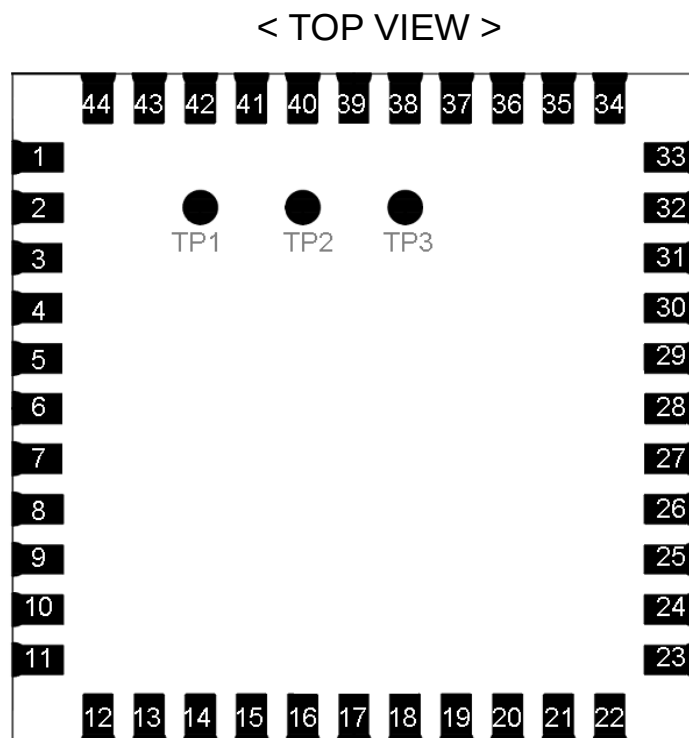
Conditions : VBAT=3.3V ; VDDIO=3.3V ; Temp:25°C

| Feature                                          | Description                           |          |      |
|--------------------------------------------------|---------------------------------------|----------|------|
| <b>General Specification</b>                     |                                       |          |      |
| Bluetooth Standard                               | Bluetooth V4.2 of 1, 2 and 3 Mbps.    |          |      |
| Host Interface                                   | UART                                  |          |      |
| Antenna Reference                                | Small antennas with 0~2 dBi peak gain |          |      |
| Frequency Band                                   | 2402MHz ~ 2480MHz                     |          |      |
| Number of Channels                               | 79 channels                           |          |      |
| Modulation                                       | FHSS, GFSK, DPSK, DQPSK, 8DPSK        |          |      |
| <b>RF Specification</b>                          |                                       |          |      |
|                                                  | Min.                                  | Typical. | Max. |
| Output Power <sup>1</sup>                        |                                       | 7        |      |
| Sensitivity @ BER=0.1%<br>for GFSK (1Mbps)       |                                       | -86 dBm  |      |
| Sensitivity @ BER=0.01%<br>for π/4-DQPSK (2Mbps) |                                       | -88 dBm  |      |
| Sensitivity @ BER=0.01%<br>for 8DPSK (3Mbps)     |                                       | -82 dBm  |      |
| Maximum Input Level                              | GFSK (1Mbps):-20dBm                   |          |      |
|                                                  | π/4-DQPSK (2Mbps) :-20dBm             |          |      |
|                                                  | 8DPSK (3Mbps) :-20dBm                 |          |      |

**NOTE<sup>1</sup>** : Output power can be configured by HCD firmware.

# 7. Pin Assignments

## 7.1 Pin Outline



## 7.2 Pin Definition

| NO | Name         | Type | Description                              |
|----|--------------|------|------------------------------------------|
| 1  | GND          | —    | Ground connections                       |
| 2  | WL_BT_ANT    | I/O  | RF I/O port                              |
| 3  | GND          | —    | Ground connections                       |
| 4  | NC           | —    | Floating (Don't connected to ground)     |
| 5  | NC           | —    | Floating (Don't connected to ground)     |
| 6  | BT_WAKE      | I    | HOST wake-up Bluetooth device            |
| 7  | BT_HOST_WAKE | O    | Bluetooth device to wake-up HOST         |
| 8  | NC           | —    | Floating (Don't connected to ground)     |
| 9  | VBAT         | P    | Main power voltage source input          |
| 10 | XTAL_IN      | I    | Crystal input                            |
| 11 | XTAL_OUT     | O    | Crystal output                           |
| 12 | WL_REG_ON    | I    | Internal regulators power enable/disable |
| 13 | WL_HOST_WAKE | O    | WLAN to wake-up HOST                     |

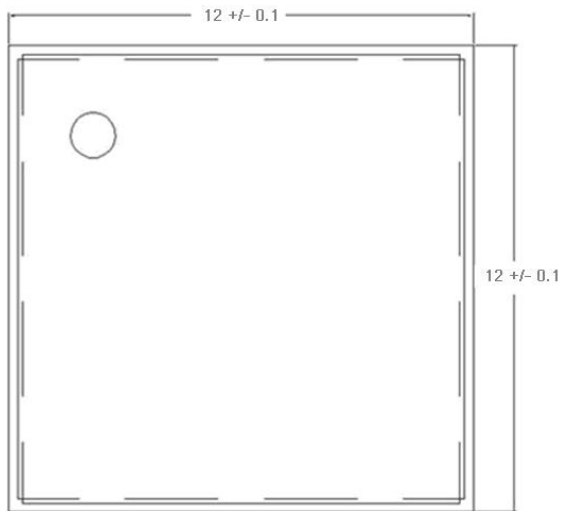
|    |                            |     |                                                                                     |
|----|----------------------------|-----|-------------------------------------------------------------------------------------|
| 14 | SDIO_DATA_2/gSPI Strapping | I/O | SDIO data line 2/gSPI Strapping<br>The default is SDIO. For gSPI, pull this pin low |
| 15 | SDIO_DATA_3/CS             | I/O | SDIO data line 3/ gSPI card select                                                  |
| 16 | SDIO_DATA_CMD/DI           | I/O | SDIO command line/ gSPI data input                                                  |
| 17 | SDIO_DATA_CLK/SCLK         | I/O | SDIO clock line/ gSPI Clock                                                         |
| 18 | SDIO_DATA_0/DO             | I/O | SDIO data line 0/ gSPI data output                                                  |
| 19 | SDIO_DATA_1/IRQ            | I/O | SDIO data line 1/ gSPI interrupt                                                    |
| 20 | GND                        | —   | Ground connections                                                                  |
| 21 | VIN_LDO_OUT                | P   | Internal Buck voltage generation pin                                                |
| 22 | VDDIO                      | P   | I/O Voltage supply input                                                            |
| 23 | VIN_LDO                    | P   | Internal Buck voltage generation pin                                                |
| 24 | LPO                        | I   | External Low Power Clock input (32.768KHz)                                          |
| 25 | PCM_OUT                    | O   | PCM Data output                                                                     |
| 26 | PCM_CLK                    | I/O | PCM clock                                                                           |
| 27 | PCM_IN                     | I   | PCM data input                                                                      |
| 28 | PCM_SYNC                   | I/O | PCM sync signal                                                                     |
| 29 | NC                         | —   | Floating (Don't connected to ground)                                                |
| 30 | NC                         | —   | Floating (Don't connected to ground)                                                |
| 31 | GND                        | —   | Ground connections                                                                  |
| 32 | NC                         | —   | Floating (Don't connected to ground)                                                |
| 33 | GND                        | —   | Ground connections                                                                  |
| 34 | BT_RST_N                   | I   | Low asserting reset for Bluetooth core                                              |
| 35 | NC                         | —   | Floating (Don't connected to ground)                                                |
| 36 | GND                        | —   | Ground connections                                                                  |
| 37 | NC                         | —   | Floating (Don't connected to ground)                                                |
| 38 | NC                         | —   | Floating (Don't connected to ground)                                                |
| 39 | GPIO2                      | I/O | GPIO Control                                                                        |
| 40 | GPIO1                      | I/O | GPIO Control                                                                        |
| 41 | UART_RTS_N                 | O   | Bluetooth UART interface                                                            |
| 42 | UART_TXD                   | O   | Bluetooth UART interface                                                            |
| 43 | UART_RXD                   | I   | Bluetooth UART interface                                                            |
| 44 | UART_CTS_N                 | I   | Bluetooth UART interface                                                            |
| 45 | TP1 (NC)                   | —   | Floating (Don't connected to ground)                                                |
| 46 | TP2 (NC)                   | —   | Floating (Don't connected to ground)                                                |
| 47 | TP3 (NC)                   | —   | Floating (Don't connected to ground)                                                |

# 8. Dimensions

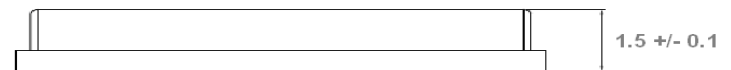
## 8.1 Physical Dimensions

(Unit: mm)

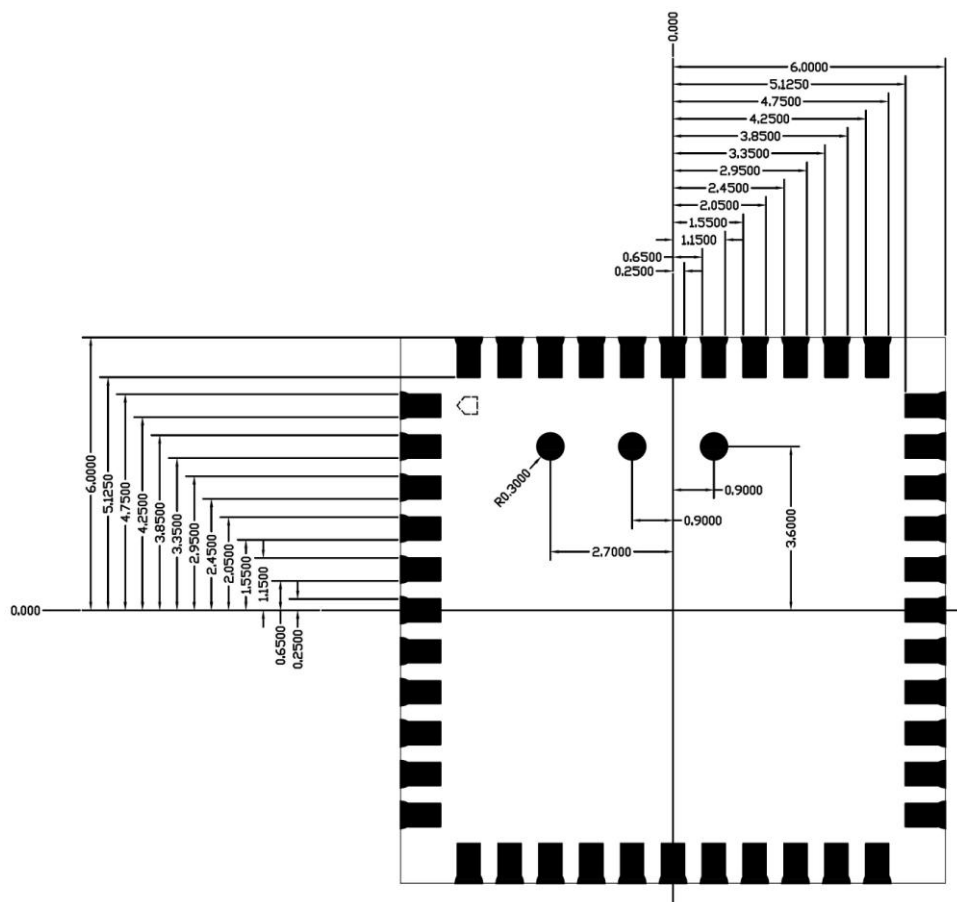
< TOP VIEW >



< Side View >

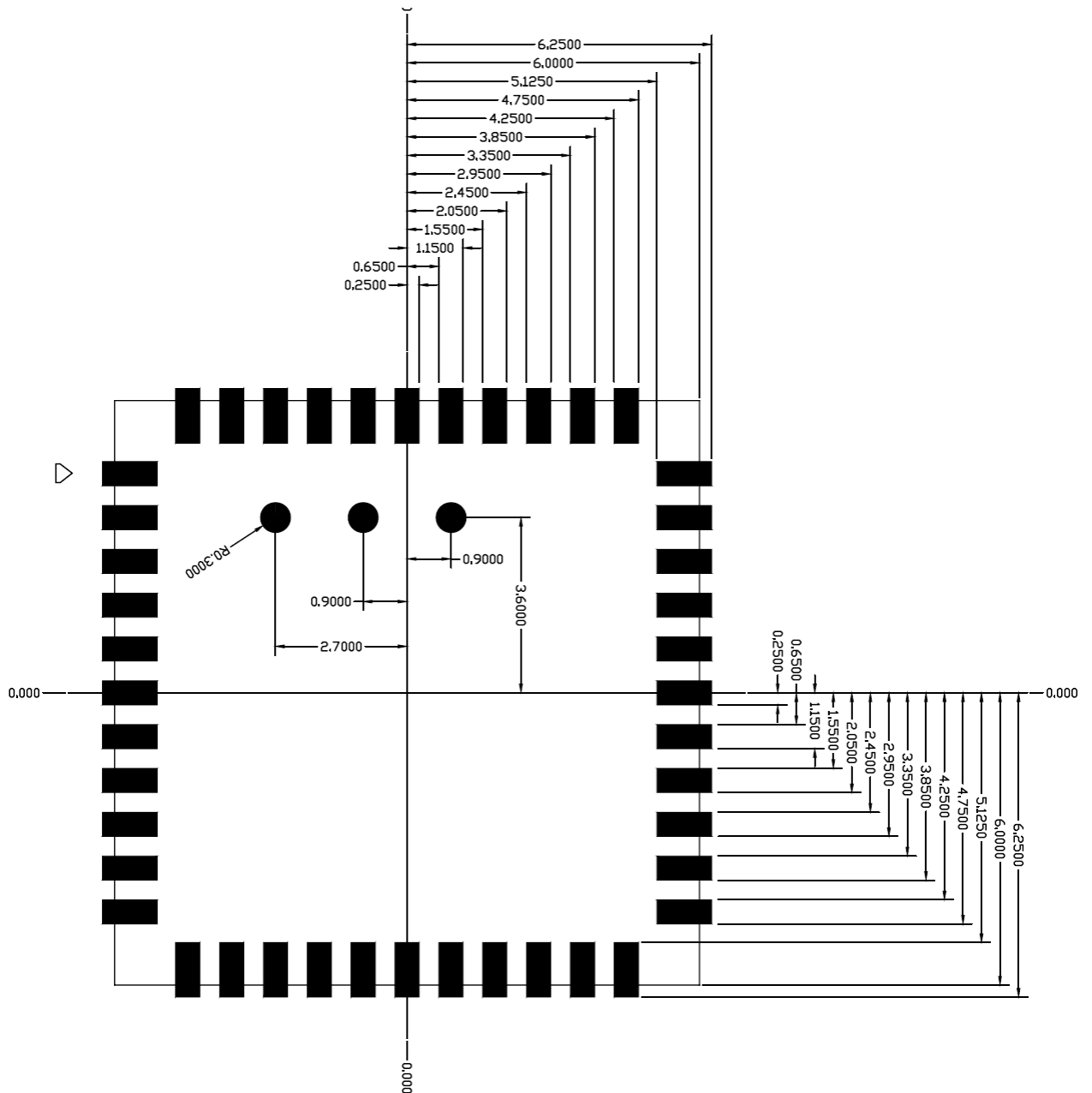


< TOP VIEW >



(Unit: mm)

< TOP VIEW >



## 9. External clock reference

External LPO signal characteristics

| Parameter               | Specification                        | Units   |
|-------------------------|--------------------------------------|---------|
| Nominal input frequency | 32.768                               | kHz     |
| Frequency accuracy      | ±200                                 | ppm     |
| Duty cycle              | 30 - 70                              | %       |
| Input signal amplitude  | 400 to 3300                          | mV, p-p |
| Signal type             | Square-wave                          | -       |
| Input impedance         | >100k<br><5                          | Ω<br>pF |
| Clock jitter            | <5,000                               | ppm     |
| Output high voltage     | 0.7V <sub>io</sub> - V <sub>io</sub> | V       |

External Ref\_CLK signal characteristics

| No. | Item                         | Symb.            | Electrical Specification |      |      |       | Remark                |
|-----|------------------------------|------------------|--------------------------|------|------|-------|-----------------------|
|     |                              |                  | Min.                     | Type | Max. | Units |                       |
| 1   | Nominal Frequency            | F0               | 26.00000                 |      |      | MHz   |                       |
| 2   | Mode of Vibration            |                  | Fundamental              |      |      |       |                       |
| 3   | Frequency Tolerance          | ΔF/F0            | -10                      | -    | 10   | ppm   | at 25°C±3°C           |
| 4   | Operating Temperature Range  | T <sub>OPR</sub> | -30                      | -    | 85   | °C    |                       |
| 5   | Frequency Stability          | TC               | -10                      | -    | 10   | ppm   |                       |
| 6   | Storage Temperature          | T <sub>STG</sub> | -55                      | -    | 125  | °C    |                       |
| 7   | Load capacitance             | CL               | -                        | 16   |      | pF    |                       |
| 8   | Equivalent Series Resistance | ESR              | -                        | -    | 50   | Ω     |                       |
| 9   | Drive Level                  | DL               | -                        | 100  | 200  | μW    |                       |
| 10  | Insulation Resistance        | IR               | 500                      | -    | -    | MΩ    | At 100V <sub>dc</sub> |
| 11  | Shunt Capacitance            | C0               | -                        | -    | 3    | pF    |                       |
| 12  | Aging Per Year               | Fa               | -2                       | -    | 2    | ppm   | First Year            |

## 9.1 SDIO Pin Description

The module supports SDIO version 2.0 for 4-bit modes (100 Mbps), and high speed 4-bit (50 MHz clocks – 200 Mbps). It has the ability to stop the SDIO clock and map the interrupt signal into a GPIO pin. This 'out-of-band' interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force the control of the gated clocks from within the WLAN chip is also provided.

- ❖ Function 0 Standard SDIO function (Max BlockSize / ByteCount = 32B)
- ❖ Function 1 Backplane Function to access the internal System On Chip (SOC) address space (Max BlockSize / ByteCount = 64B)
- ❖ Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max BlockSize/ByteCount=512B)

### SDIO/gSPI Pin Description

| SD 4-Bit Mode |                          | gSPI Mode |             |
|---------------|--------------------------|-----------|-------------|
| DATA0         | Data Line 0              | DO        | Data Output |
| DATA1         | Data Line 1 or Interrupt | IRQ       | Interrupt   |
| DATA2         | Data Line 2 or Read Wait | NC        | Not Used    |
| DATA3         | Data Line 3              | CS        | Card select |
| CLK           | Clock                    | SCLK      | Clock       |
| CMD           | Command Line             | DI        | Data Input  |

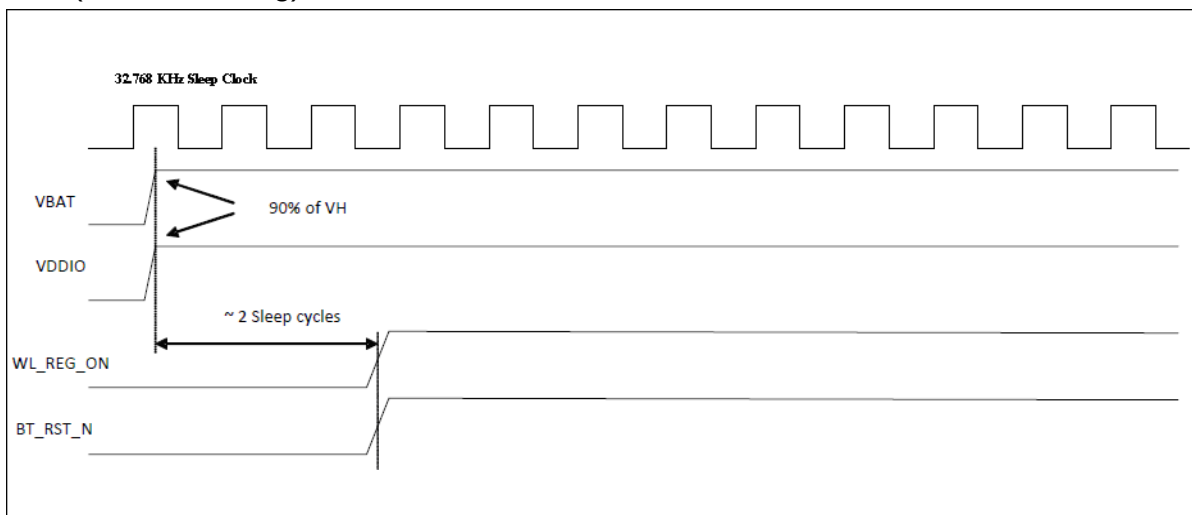
# 10. Host Interface Timing Diagram

## 10.1 Power-up Sequence Timing Diagram

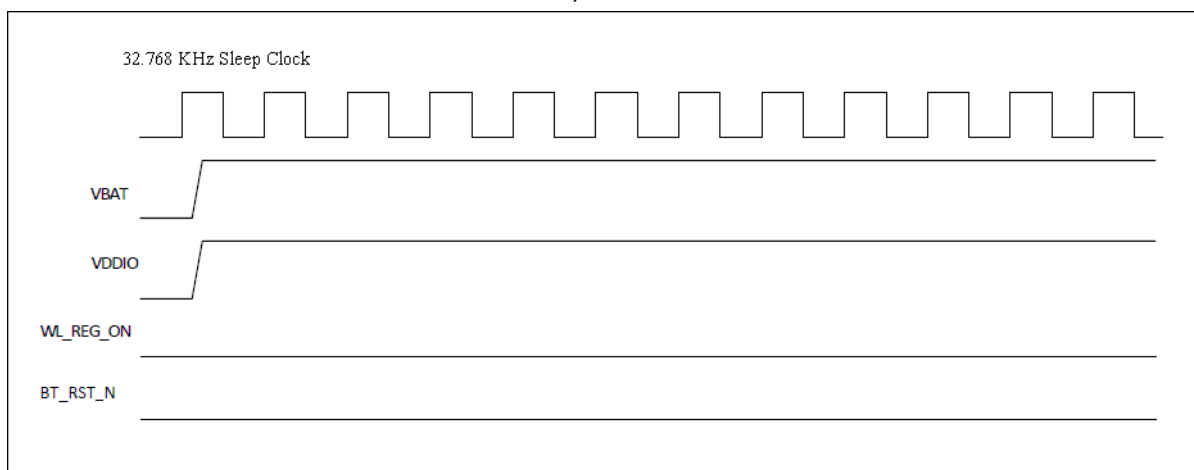
The module has signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN and internal regulator blocks. These signals are described below.

Additionally, diagrams are provided to indicate proper sequencing of the signals for various operating states. The timing value indicated are minimum required values: longer delays are also acceptable.

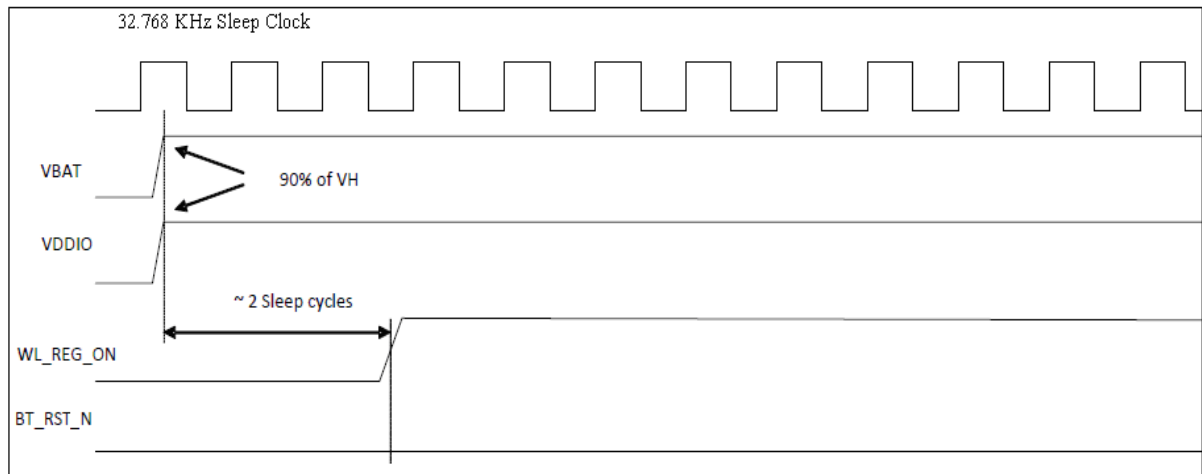
- ✘ WL\_REG\_ON: Used by the PMU to power up the WLAN section. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset.
- ✘ BT\_RST\_N: Low asserting reset for Bluetooth only. This pin has no effect on WLAN and does not control any PMU functions. This pin must be driven high or low (not left floating).



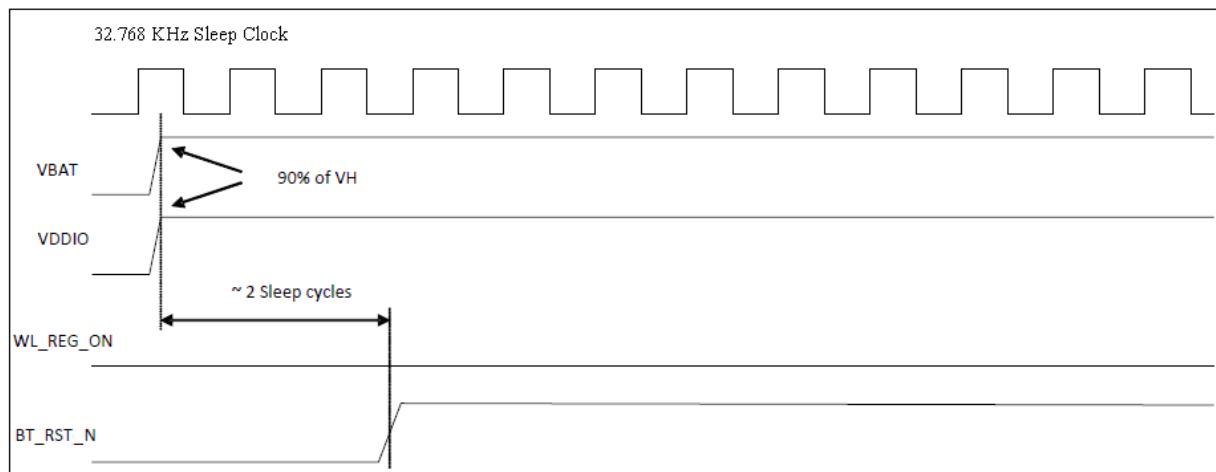
WLAN=ON, Bluetooth=ON



WLAN=OFF, Bluetooth=OFF

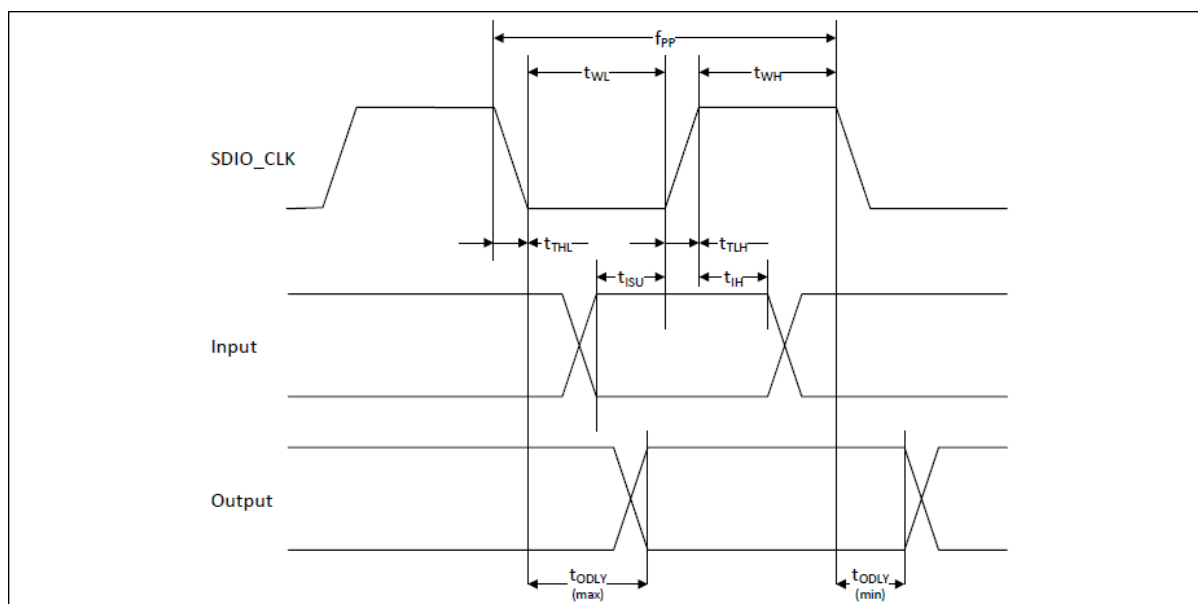


WLAN=ON, Bluetooth=OFF



WLAN=OFF, Bluetooth=ON

## 10.2 SDIO Default Mode Timing Diagram

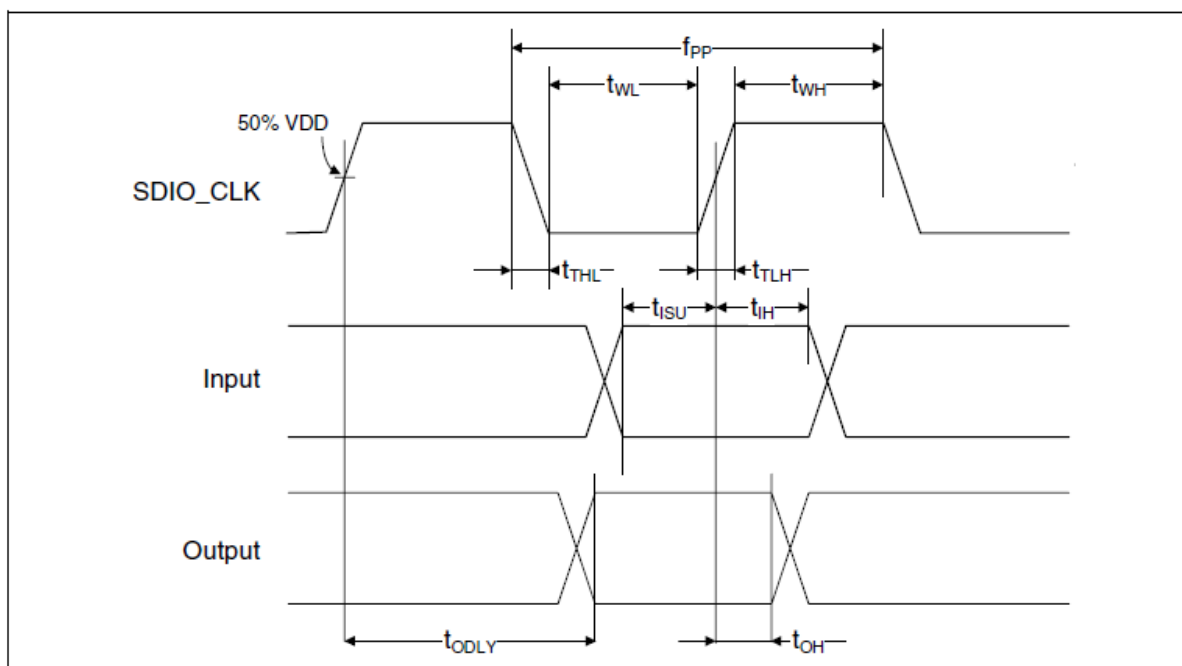


| Parameter                                                                                                            | Symbol     | Minimum | Typical | Maximum | Unit |
|----------------------------------------------------------------------------------------------------------------------|------------|---------|---------|---------|------|
| <b>SDIO CLK (All values are referred to minimum <math>V_{IH}</math> and maximum <math>V_{IL}</math><sup>b</sup>)</b> |            |         |         |         |      |
| Frequency-Data Transfer mode                                                                                         | $f_{PP}$   | 0       | -       | 25      | MHz  |
| Frequency-Identification mode                                                                                        | $f_{OD}$   | 0       | -       | 400     | kHz  |
| Clock low time                                                                                                       | $t_{WL}$   | 10      | -       | -       | ns   |
| Clock high time                                                                                                      | $t_{WH}$   | 10      | -       | -       | ns   |
| Clock rise time                                                                                                      | $t_{TLH}$  | -       | -       | 10      | ns   |
| Clock low time                                                                                                       | $t_{THL}$  | -       | -       | 10      | ns   |
| <b>Inputs: CMD, DAT (referenced to CLK)</b>                                                                          |            |         |         |         |      |
| Input setup time                                                                                                     | $t_{ISU}$  | 5       | -       | -       | ns   |
| Input hold time                                                                                                      | $t_{IH}$   | 5       | -       | -       | ns   |
| <b>Outputs: CMD, DAT (referenced to CLK)</b>                                                                         |            |         |         |         |      |
| Output delay time - Data Transfer mode                                                                               | $t_{ODLY}$ | 0       | -       | 14      | ns   |
| Output delay time - Identification mode                                                                              | $t_{ODLY}$ | 0       | -       | 50      | ns   |

a. Timing is based on  $CL \leq 40pF$  load on CMD and Data.

b.  $\min(V_{IH}) = 0.7 \times V_{DDIO}$  and  $\max(V_{IL}) = 0.2 \times V_{DDIO}$ .

## 10.3 SDIO High Speed Mode Timing Diagram

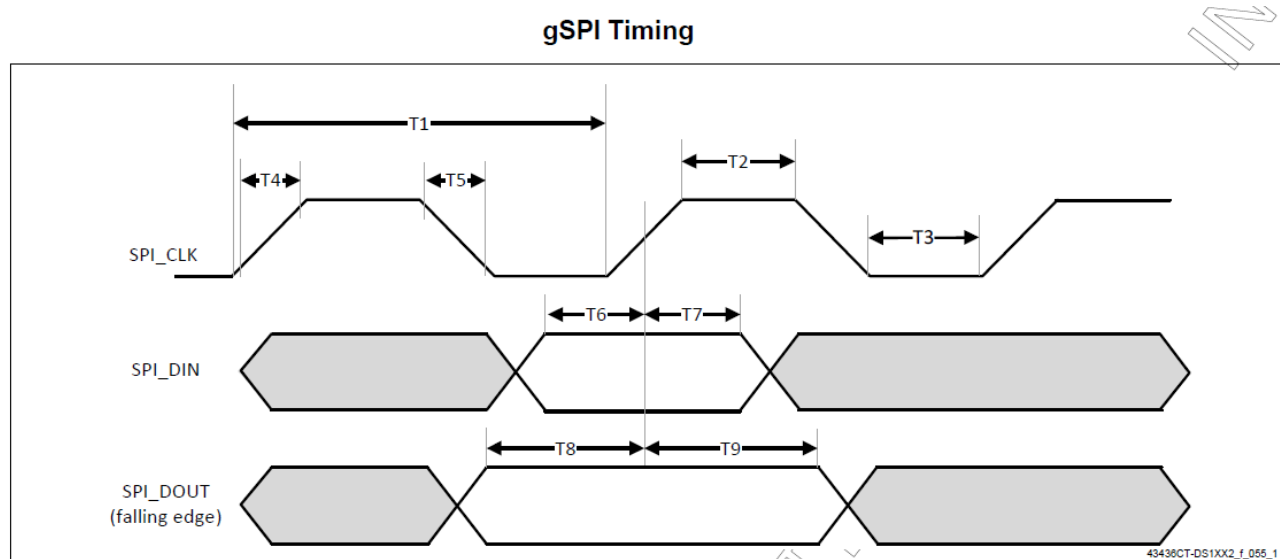


| Parameter                                                                                                            | Symbol     | Minimum | Typical | Maximum | Unit |
|----------------------------------------------------------------------------------------------------------------------|------------|---------|---------|---------|------|
| <b>SDIO CLK (All values are referred to minimum <math>V_{IH}</math> and maximum <math>V_{IL}</math><sup>b</sup>)</b> |            |         |         |         |      |
| Frequency-Data Transfer mode                                                                                         | $f_{PP}$   | 0       | -       | 50      | MHz  |
| Frequency-Identification mode                                                                                        | $f_{OD}$   | 0       | -       | 400     | kHz  |
| Clock low time                                                                                                       | $t_{WL}$   | 7       | -       | -       | ns   |
| Clock high time                                                                                                      | $t_{WH}$   | 7       | -       | -       | ns   |
| Clock rise time                                                                                                      | $t_{TLH}$  | -       | -       | 3       | ns   |
| Clock low time                                                                                                       | $t_{THL}$  | -       | -       | 3       | ns   |
| <b>Inputs: CMD, DAT (referenced to CLK)</b>                                                                          |            |         |         |         |      |
| Input setup time                                                                                                     | $t_{ISU}$  | 6       | -       | -       | ns   |
| Input hold time                                                                                                      | $t_{IH}$   | 2       | -       | -       | ns   |
| <b>Outputs: CMD, DAT (referenced to CLK)</b>                                                                         |            |         |         |         |      |
| Output delay time - Data Transfer mode                                                                               | $t_{ODLY}$ | -       | -       | 14      | ns   |
| Output hold time                                                                                                     | $t_{OH}$   | 2.5     | -       | -       | ns   |
| Total system capacitance (each line)                                                                                 | CL         | -       | -       | 40      | pF   |

a. Timing is based on  $CL \leq 40\text{pF}$  load on CMD and Data.

b.  $\min(V_{IH}) = 0.7 \times V_{DDIO}$  and  $\max(V_{IL}) = 0.2 \times V_{DDIO}$ .

## 10.4 gSPI Mode Timing Diagram



**gSPI Timing Parameters**

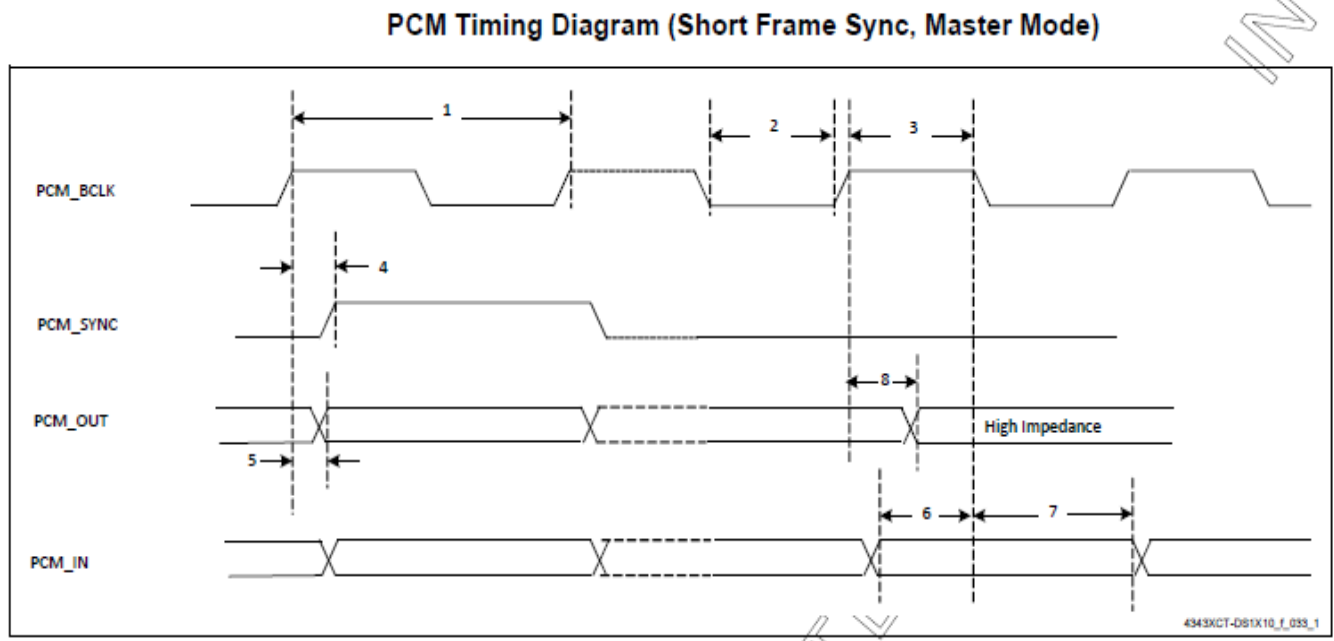
| Parameter                 | Symbol | Minimum                 | Maximum                 | Units | Note                                           |
|---------------------------|--------|-------------------------|-------------------------|-------|------------------------------------------------|
| Clock period              | T1     | 20.8                    | —                       | ns    | $F_{\max} = 50 \text{ MHz}$                    |
| Clock high/low            | T2/T3  | $(0.45 \times T1) - T4$ | $(0.55 \times T1) - T4$ | ns    | —                                              |
| Clock rise/fall time      | T4/T5  | —                       | 2.5                     | ns    | —                                              |
| Input setup time          | T6     | 5.0                     | —                       | ns    | Setup time, SIMO valid to SPI_CLK active edge  |
| Input hold time           | T7     | 5.0                     | —                       | ns    | Hold time, SPI_CLK active edge to SIMO invalid |
| Output setup time         | T8     | 5.0                     | —                       | ns    | Setup time, SOMI valid before SPI_CLK rising   |
| Output hold time          | T9     | 5.0                     | —                       | ns    | Hold time, SPI_CLK active edge to SOMI invalid |
| CSX to clock <sup>a</sup> | —      | 7.86                    | —                       | ns    | CSX fall to 1st rising edge                    |
| Clock to CSX              | —      | —                       | —                       | ns    | Last falling edge to CSX high                  |

a. SPI\_CSx remains active for entire duration of gSPI read/write/write\_read transaction (that is, overall words for multiple word transaction).

## 10.5 Uart Interface Timing

### Short Frame Sync, Master Mode

#### Short Frame Sync, Master Mode

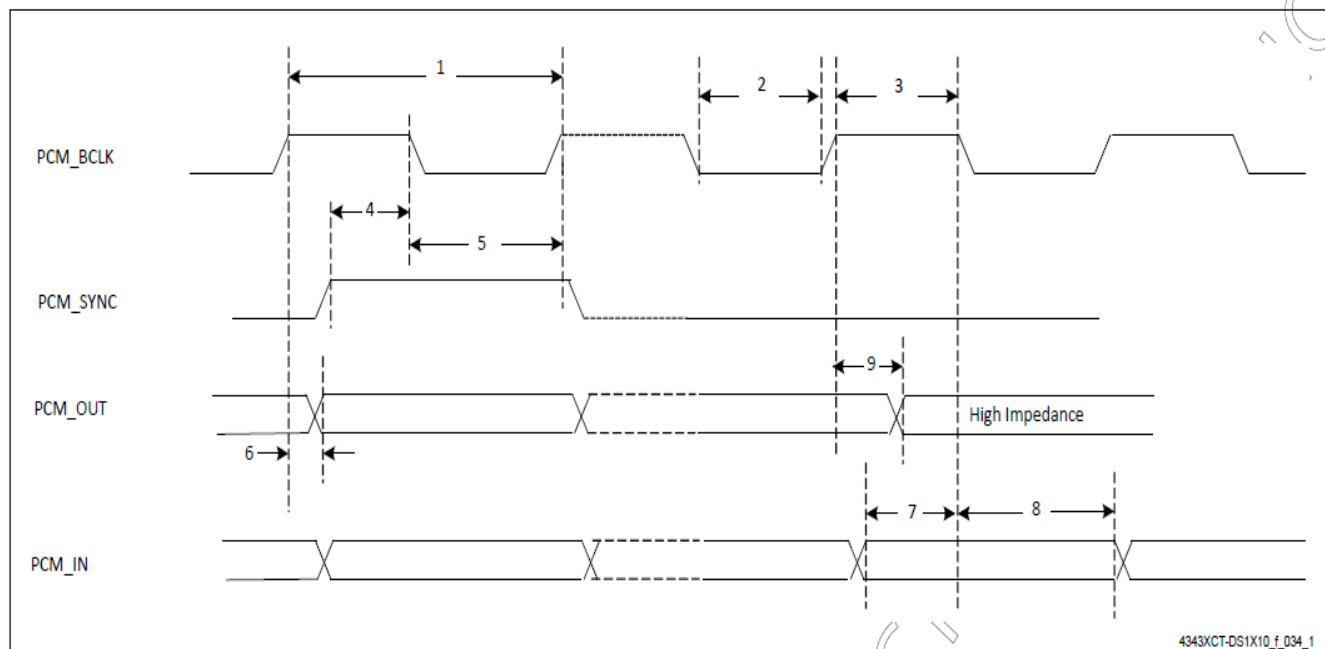


#### PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

| Ref No. | Characteristics                                                                              | Minimum | Typical | Maximum | Unit |
|---------|----------------------------------------------------------------------------------------------|---------|---------|---------|------|
| 1       | PCM bit clock frequency                                                                      | –       | –       | 12      | MHz  |
| 2       | PCM bit clock low                                                                            | 41      | –       | –       | ns   |
| 3       | PCM bit clock high                                                                           | 41      | –       | –       | ns   |
| 4       | PCM_SYNC delay                                                                               | 0       | –       | 25      | ns   |
| 5       | PCM_OUT delay                                                                                | 0       | –       | 25      | ns   |
| 6       | PCM_IN setup                                                                                 | 8       | –       | –       | ns   |
| 7       | PCM_IN hold                                                                                  | 8       | –       | –       | ns   |
| 8       | Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance | 0       | –       | 25      | ns   |

## Short Frame Sync, Slave Mode

**PCM Timing Diagram (Short Frame Sync, Slave Mode)**

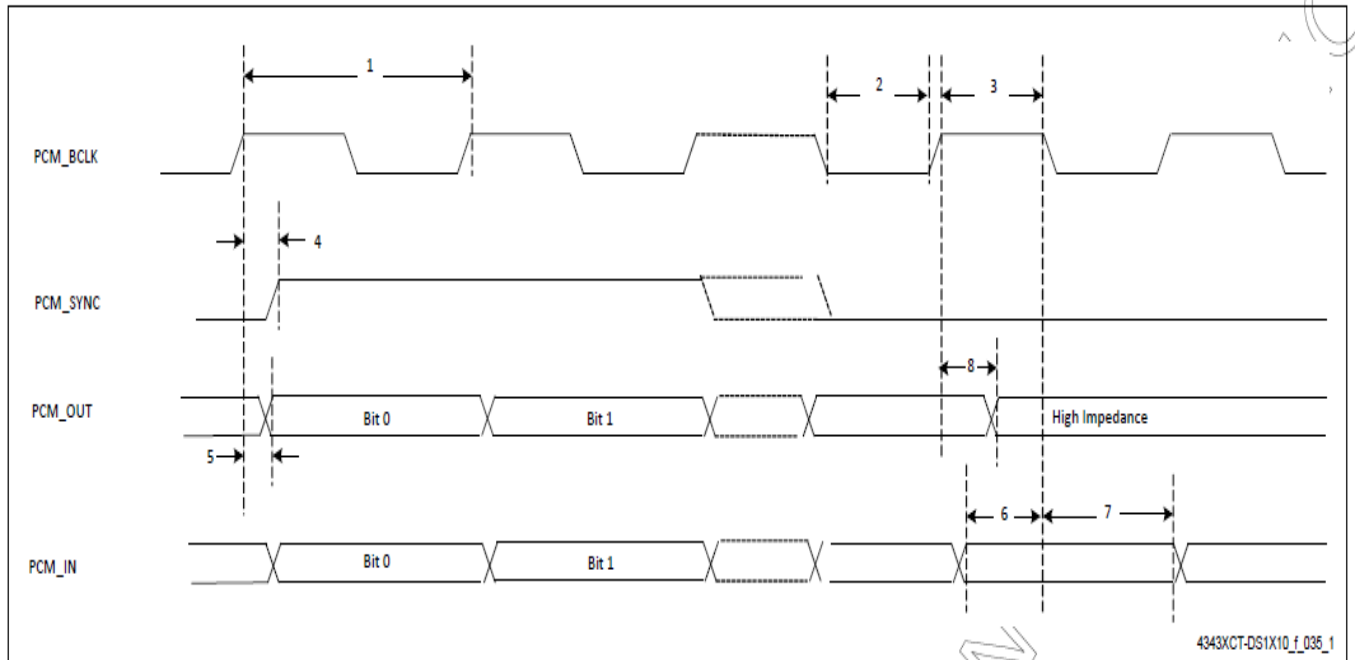


**PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)**

| Ref No. | Characteristics                                                                              | Minimum | Typical | Maximum | Unit |
|---------|----------------------------------------------------------------------------------------------|---------|---------|---------|------|
| 1       | PCM bit clock frequency                                                                      | –       | –       | 12      | MHz  |
| 2       | PCM bit clock low                                                                            | 41      | –       | –       | ns   |
| 3       | PCM bit clock high                                                                           | 41      | –       | –       | ns   |
| 4       | PCM_SYNC setup                                                                               | 8       | –       | –       | ns   |
| 5       | PCM_SYNC hold                                                                                | 8       | –       | –       | ns   |
| 6       | PCM_OUT delay                                                                                | 0       | –       | 25      | ns   |
| 7       | PCM_IN setup                                                                                 | 8       | –       | –       | ns   |
| 8       | PCM_IN hold                                                                                  | 8       | –       | –       | ns   |
| 9       | Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance | 0       | –       | 25      | ns   |

## Long Frame Sync, Master Mode

**PCM Timing Diagram (Long Frame Sync, Master Mode)**

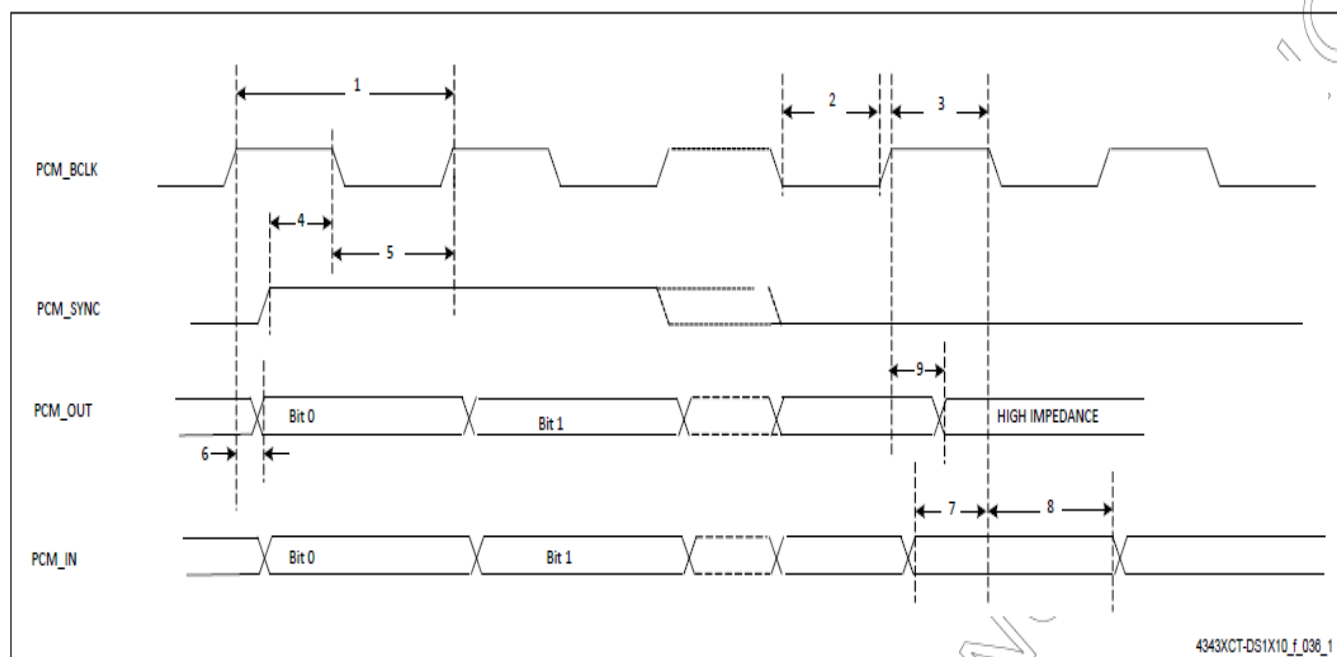


**PCM Interface Timing Specifications (Long Frame Sync, Master Mode)**

| Ref No. | Characteristics                                                                              | Minimum | Typical | Maximum | Unit |
|---------|----------------------------------------------------------------------------------------------|---------|---------|---------|------|
| 1       | PCM bit clock frequency                                                                      | –       | –       | 12      | MHz  |
| 2       | PCM bit clock low                                                                            | 41      | –       | –       | ns   |
| 3       | PCM bit clock high                                                                           | 41      | –       | –       | ns   |
| 4       | PCM_SYNC delay                                                                               | 0       | –       | 25      | ns   |
| 5       | PCM_OUT delay                                                                                | 0       | –       | 25      | ns   |
| 6       | PCM_IN setup                                                                                 | 8       | –       | –       | ns   |
| 7       | PCM_IN hold                                                                                  | 8       | –       | –       | ns   |
| 8       | Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance | 0       | –       | 25      | ns   |

## Long Frame Sync, Slave Mode

**PCM Timing Diagram (Long Frame Sync, Slave Mode)**



**PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)**

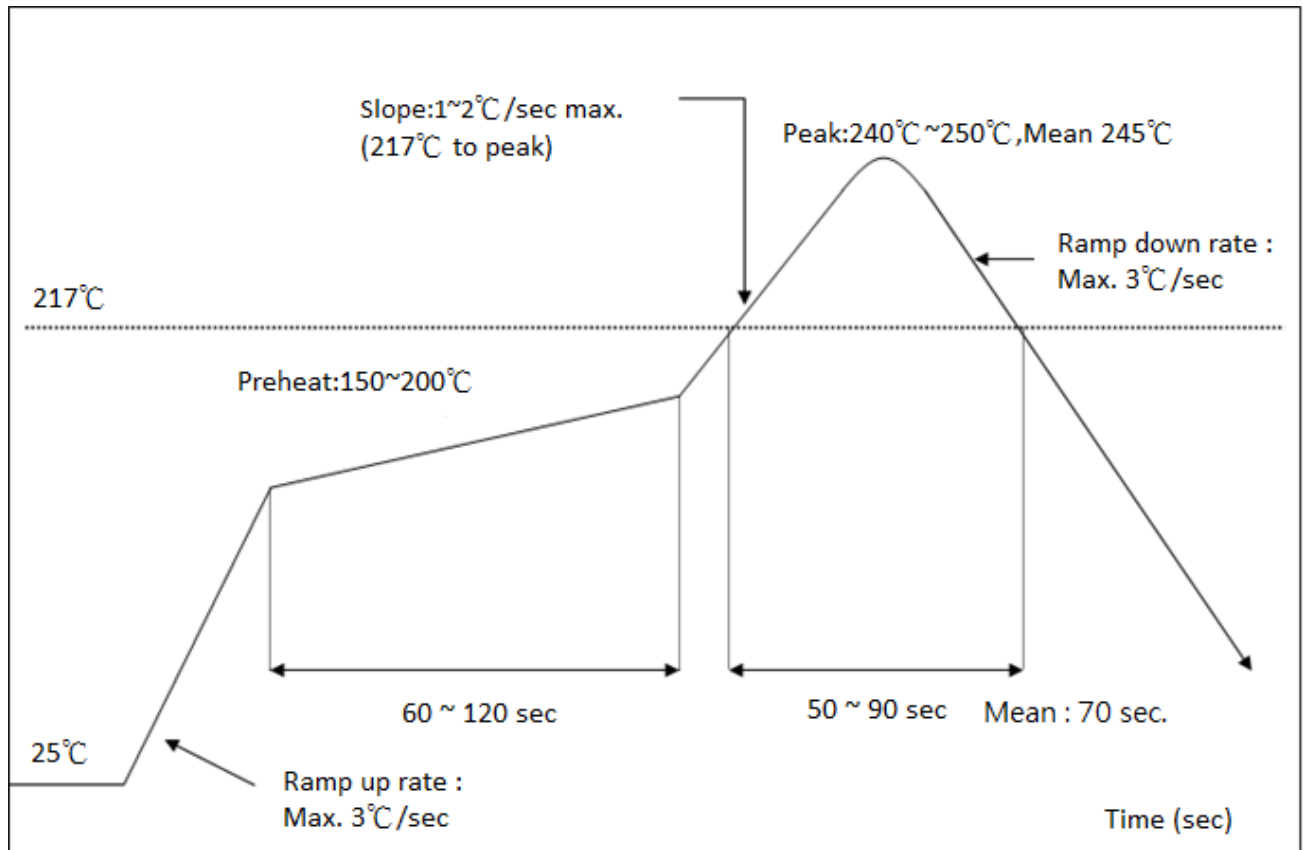
| Ref No. | Characteristics                                                                              | Minimum | Typical | Maximum | Unit |
|---------|----------------------------------------------------------------------------------------------|---------|---------|---------|------|
| 1       | PCM bit clock frequency                                                                      | –       | –       | 12      | MHz  |
| 2       | PCM bit clock low                                                                            | 41      | –       | –       | ns   |
| 3       | PCM bit clock high                                                                           | 41      | –       | –       | ns   |
| 4       | PCM_SYNC setup                                                                               | 8       | –       | –       | ns   |
| 5       | PCM_SYNC hold                                                                                | 8       | –       | –       | ns   |
| 6       | PCM_OUT delay                                                                                | 0       | –       | 25      | ns   |
| 7       | PCM_IN setup                                                                                 | 8       | –       | –       | ns   |
| 8       | PCM_IN hold                                                                                  | 8       | –       | –       | ns   |
| 9       | Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance | 0       | –       | 25      | ns   |

# 11. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <250°C

Number of Times : ≤2 times



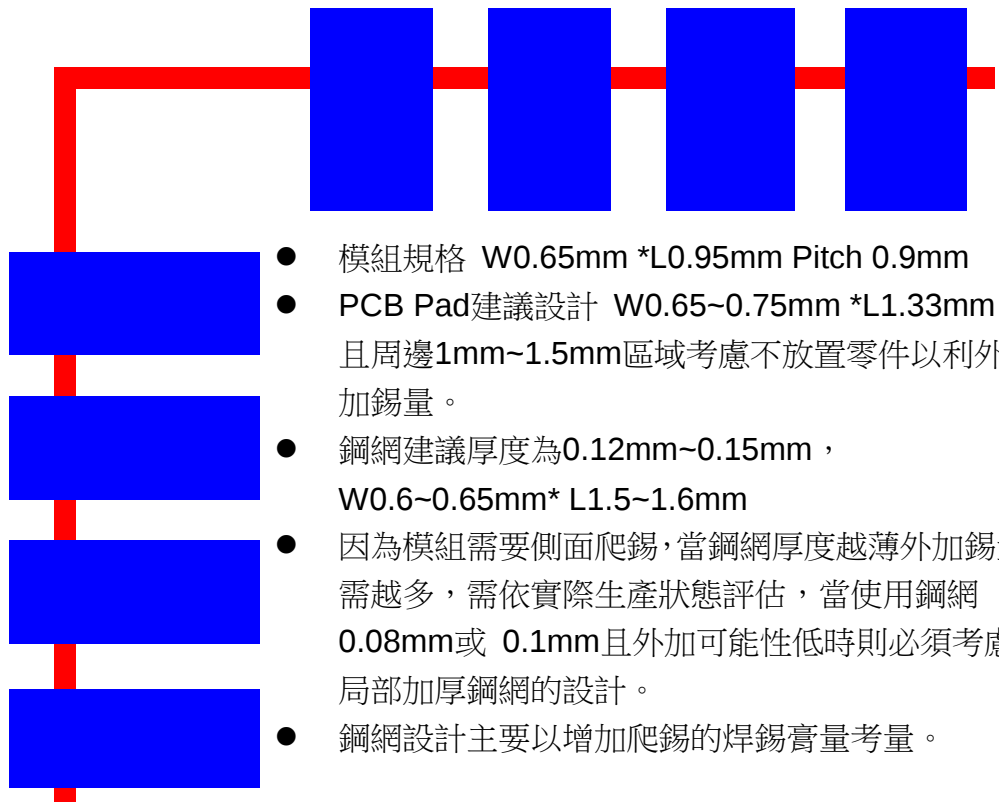
The notification of WiFi module before mounting:

The aperture of stencil should be larger than foot print of module, and the stencil thickness should be not less than 0.12mm.

Reflow 時需使用 N2, 含氧量建議 5000 ppm 以下,

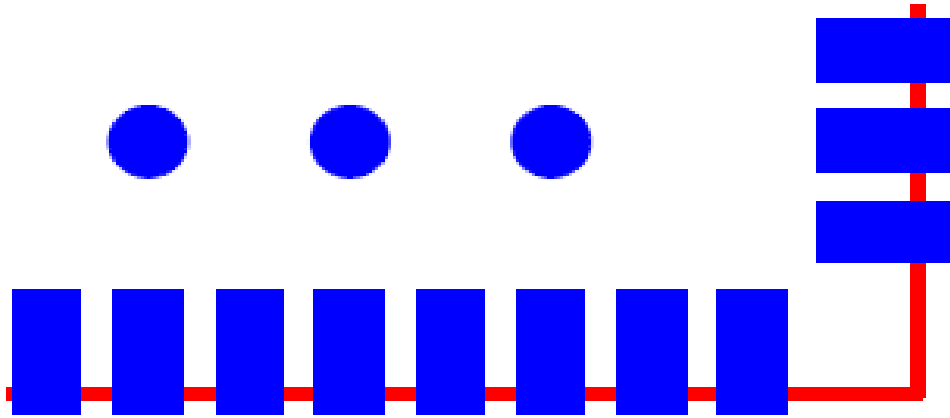
It must use N2 for reflow and suggest the concentration of oxygen less than 5000 ppm .

# Solder Paste definition



- 模組規格 W0.65mm \*L0.95mm Pitch 0.9mm
- PCB Pad建議設計 W0.65~0.75mm \*L1.33mm，且周邊1mm~1.5mm區域考慮不放置零件以利外加錫量。
- 鋼網建議厚度為0.12mm~0.15mm，W0.6~0.65mm\* L1.5~1.6mm
- 因為模組需要側面爬錫，當鋼網厚度越薄外加錫量需越多，需依實際生產狀態評估，當使用鋼網0.08mm或 0.1mm且外加可能性低時則必須考慮局部加厚鋼網的設計。
- 鋼網設計主要以增加爬錫的焊錫膏量考量。

- Module Specifications : W:0.65mm \* L:0.95mm pitch 0.9 mm
- The proposed design W:0.65~0.75 mm \* L:1.33mm. Consider not place other parts in the peripheral area of 1 mm ~ 1.5 mm to facilitate additional amount of solder for PCB pad.
- We Suggest the thickness of Stencil between 0.12 mm ~0.15mm, the W between 0.6~0.65mm and the L between L1.5~1.6mm.
- If the thickness of the stencil is thinner, we suggest to adding more solder, to increase the wetting ability. Depends on different production situation, if the stencil thickness is 0.08~0.1mm, and the module nearby area is no more space for expending soldering area, we will suggest to increase the stencil thickness to increase the wetting ability.
- The major consideration parts of stencil design is to increase the solder paste wetting ability.



模組規格 L 0.7mm

PCB Pad 設計 L 0.8mm

鋼網開孔建議 L0.5mm~0.6mm

適當內縮可以避免撐高造成高度影響

- Module Specifications L 0.7mm
- The design for PCB Pad : L:0.8mm
- We recommend the apertures for stencil L:0.5mm~0.6mm
- In order to avoid highness impact caused solder paste thickness, the stencil open size can be appropriately retracted

# 12. Package Information

## 12.1 Label

Label A→ Anti-static and humidity notice



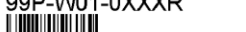
Label B→ MSL caution / Storage Condition

|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                                                          |                                                                                                                                                              |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | <b>Caution</b><br>This bag contains<br><b>MOISTURE-SENSITIVE DEVICES</b> | <b>LEVEL</b><br><div style="border: 1px solid black; width: 30px; height: 20px; margin: 0 auto;"></div> <small>If blank, see adjacent bar code label</small> |
| <ol style="list-style-type: none"><li>1. Calculated shelf life in sealed bag: 12 months at &lt;40°C and &lt;90% relative humidity (RH)</li><li>2. Peak package body temperature: _____ °C<br/><small>If blank, see adjacent bar code label</small></li><li>3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be<ol style="list-style-type: none"><li>a) Mounted within: _____ hours of factory conditions<br/><small>If blank, see adjacent bar code label</small><br/>≤30°C/60% RH, or</li><li>b) Stored per J-STD-033</li></ol></li><li>4. Devices require bake, before mounting, if:<ol style="list-style-type: none"><li>a) Humidity Indicator Card reads &gt;10% for level 2a - 5a devices or &gt;60% for level 2 devices when read at 23 ± 5°C</li><li>b) 3a or 3b are not met</li></ol></li><li>5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure</li></ol> |                                                                          |                                                                                                                                                              |
| Bag Seal Date: _____<br><small>If blank, see adjacent bar code label</small>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |                                                                          |                                                                                                                                                              |
| <small>Note: Level and body temperature defined by IPC/JEDEC J-STD-020</small>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                                                                          |                                                                                                                                                              |

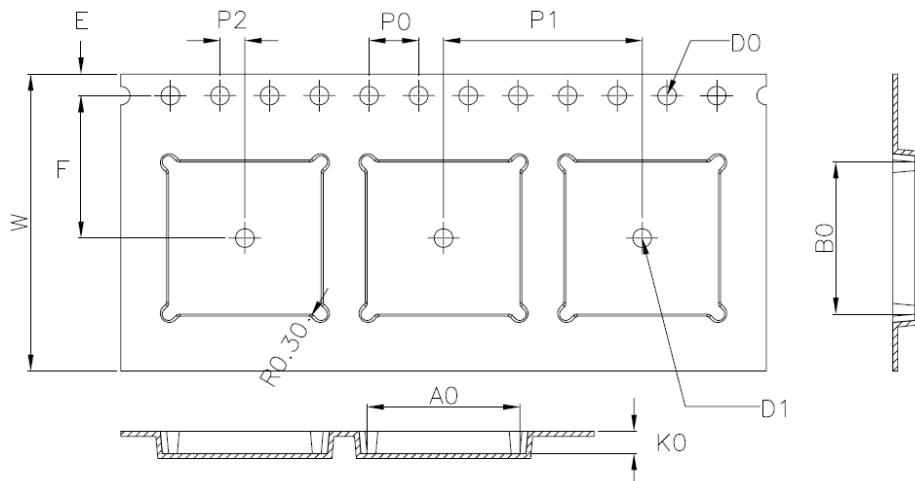
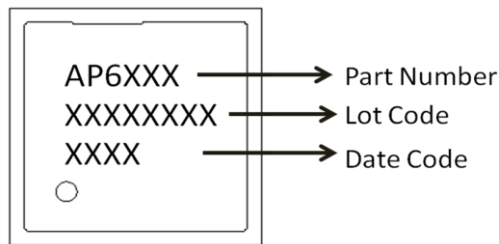
Label C→ Inner box label .

|             |                                                                                                       |
|-------------|-------------------------------------------------------------------------------------------------------|
| PO:         |                    |
| AMK DEVICE: |                    |
| PKG S/N:    | <br>9PKGXXXXXXXXXX |
| Model :     | <br>AP6XXX(HF)     |
| P/N:        | <br>99P-W01-0XXXR  |
| Qty :       | <br>1500           |
| Date Code : | <br>XXXX           |
| Lot Code :  | <br>TXXXXXX        |

Label D→ Carton box label .

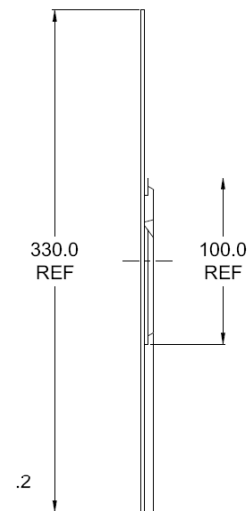
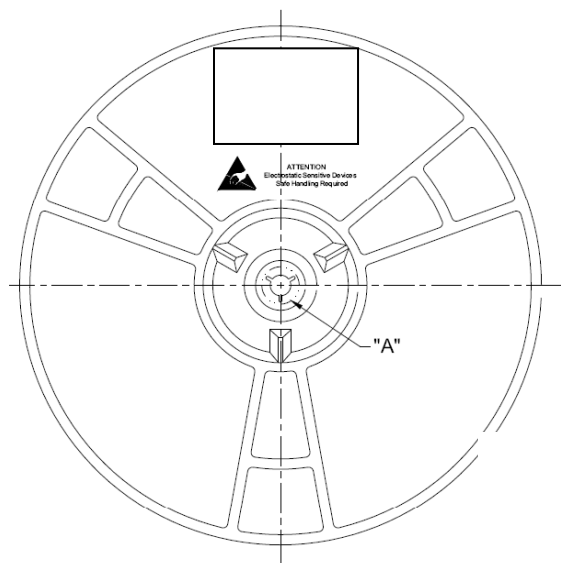
| AMPAK Technology |                                                                                                      |
|------------------|------------------------------------------------------------------------------------------------------|
| PO :             |                   |
| AMK DEVICE:      |                   |
| Model Name :     | <br>AP6XXX (HF)   |
| Part No.:        | <br>99P-W01-0XXXR |
| Quantity :       | <br>7500          |
| Lot D/C:         | <br>TXXXXXX XXXX |
| Manufacture:     | <br>YYYY/MM/DD    |

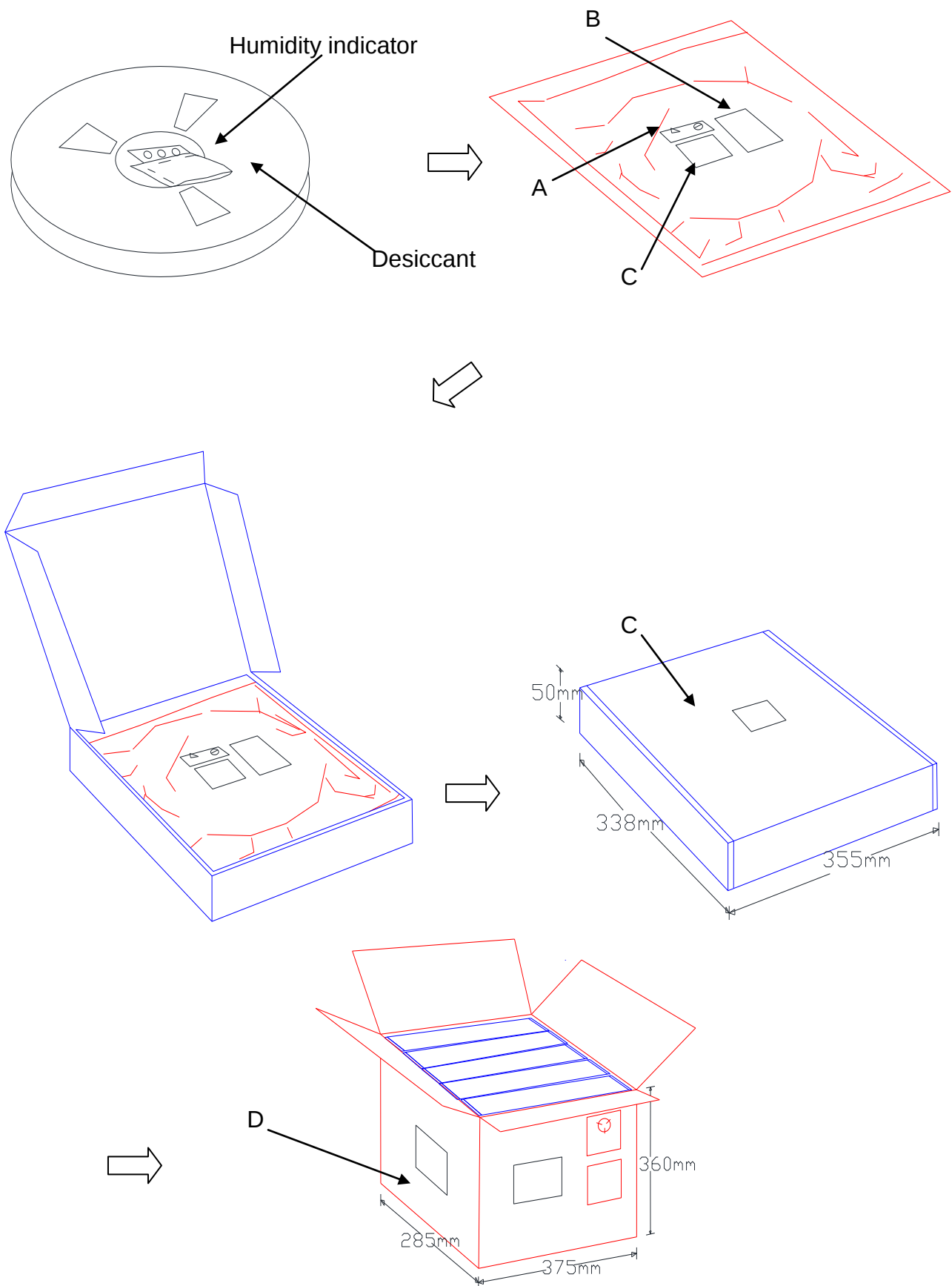
## 12.2 Dimension



|    |                                                             |
|----|-------------------------------------------------------------|
| W  | 24.00±0.30                                                  |
| A0 | 12.30±0.10                                                  |
| B0 | 12.30±0.10                                                  |
| K0 | 1.80±0.10                                                   |
| E  | 1.75±0.10                                                   |
| F  | 11.50±0.10                                                  |
| P0 | 4.00±0.10                                                   |
| P1 | 16.00±0.10                                                  |
| P2 | 2.00±0.10                                                   |
| D0 | 1.50 $\begin{smallmatrix} +0.10 \\ -0.00 \end{smallmatrix}$ |
| D1 | Ø1.50MIN                                                    |

1. 10 sprocket hole pitch cumulative tolerance  $\pm 0.20$ .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481-D requirements.
5. Thickness :  $0.30 \pm 0.05$ mm.
6. Packing length per 22" reel : 98.5 Meters.(1:3)
7. Component load per 13" reel : 1500 pcs.





## 12.3 MSL Level / Storage Condition

|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |                                                                          |                                                                                                                                                                    |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | <b>Caution</b><br>This bag contains<br><b>MOISTURE-SENSITIVE DEVICES</b> | <div style="border: 1px solid black; padding: 5px; display: inline-block;"><b>LEVEL</b><br/><b>4</b></div><br><small>If blank, see adjacent bar code label</small> |
| <p>1. Calculated shelf life in sealed bag: 12 months at <math>&lt;40^{\circ}\text{C}</math> and <math>&lt;90\%</math> relative humidity (RH)</p> <p>2. Peak package body temperature: <u>250</u> <math>^{\circ}\text{C}</math><br/><small>If blank, see adjacent bar code label</small></p> <p>3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be</p> <p style="margin-left: 40px;">a) Mounted within: <u>72</u> hours of factory conditions<br/><small>If blank, see adjacent bar code label</small></p> <p style="margin-left: 80px;"><math>\leq 30^{\circ}\text{C} / 60\% \text{ RH}</math>, or</p> <p style="margin-left: 40px;">b) Stored per J-STD-033</p> <p>4. Devices require bake, before mounting, if:</p> <p style="margin-left: 40px;">a) Humidity Indicator Card reads <math>&gt;10\%</math> for level 2a-5a devices or <math>&gt;60\%</math> for level 2 devices when read at <math>23 \pm 5^{\circ}\text{C}</math></p> <p style="margin-left: 40px;">b) 3a or 3b are not met.</p> <p>5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure.</p> <p>Bag Seal Date: _____<br/><small>If blank, see adjacent bar code label</small></p> <p style="text-align: center; margin-top: 20px;"><small>Note: Level and body temperature defined by IPC/JEDEC J-STD-020</small></p> |                                                                          |                                                                                                                                                                    |