AUTOMOTIVE-COMPLIANT, 32V, 3A LOW IQ SYNCHRONOUS BUCK CONVERTER

Description

The AP63300Q/AP63301Q is an automotive-compliant, 3A, synchronous buck converter with a wide input voltage range of 3.8V to 32V. The device fully integrates a 75mΩ high-side power MOSFET and a 40mΩ low-side power MOSFET to provide high-efficiency step-down DC-DC conversion.

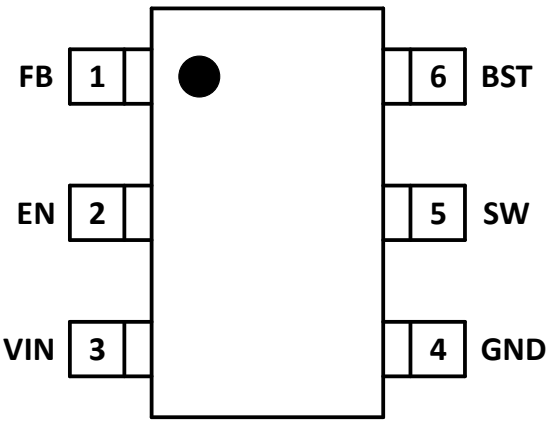
The AP63300Q/AP63301Q device is easily used by minimizing the external component count due to its adoption of peak current mode control along with its integrated loop compensation network.

The AP63300Q/AP63301Q design is optimized for Electromagnetic Interference (EMI) reduction. The device has a proprietary gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off times, which reduces high-frequency radiated EMI noise caused by MOSFET switching. The AP63300Q also features Frequency Spread Spectrum (FSS) with a switching frequency jitter of ±6%, which reduces EMI by not allowing emitted energy to stay in any one frequency for a significant period of time.

The device is available in a TSOT26 package.

Pin Assignments

(Top View)



TSOT26

Features

- AEC-Q100 Qualified for Automotive Applications
  - Device Temperature Grade 1: -40°C to +125°C T_A Range
- VIN: 3.8V to 32V
- Output Voltage (VOUT): 0.8V to VIN
- 3A Continuous Output Current
- 0.8V ± 1% Reference Voltage
- 22μA Low Quiescent Current (Pulse Frequency Modulation)
- 500kHz Switching Frequency
- Supports Pulse Frequency Modulation (PFM)
  - AP63300Q
  - Up to 88% Efficiency at 5mA Light Load
- Pulse Width Modulation (PWM) Regardless of Output Load
  - AP63301Q
- Proprietary Gate Driver Design for Best EMI Reduction
- Frequency Spread Spectrum (FSS) to Reduce EMI
  - AP63300Q
- Low-Dropout (LDO) Mode
- Precision Enable Threshold to Adjust UVLO
- Protection Circuitry
  - Undervoltage Lockout (UVLO)
  - Output Overvoltage Protection (OVP)
  - Cycle-by-Cycle Peak Current Limit
  - Thermal Shutdown
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **The AP63300Q and AP63301Q are suitable for automotive applications requiring specific change control; these parts are AEC-Q100 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.**
  https://www.diodes.com/quality/product-definitions/

Applications

- Automotive Power Systems
- Automotive Infotainment
- Automotive Instrument Clusters
- Automotive Body Electronics and Lighting
- Automotive Telematics
- Advanced Driver Assistance Systems

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

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Typical Application Circuit

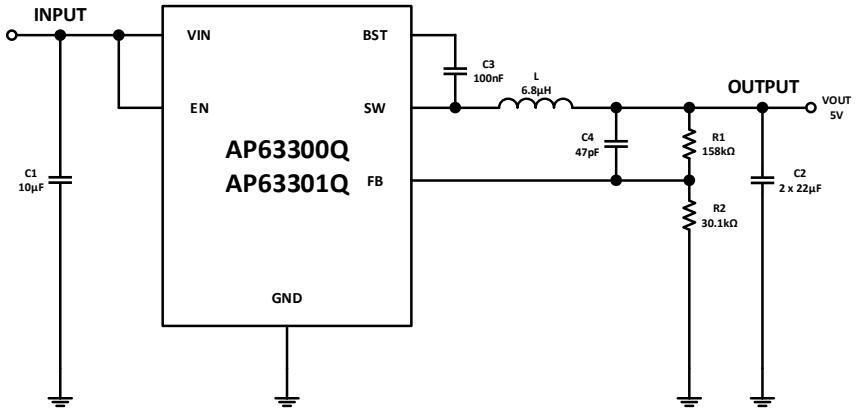

Figure 1. Typical Application Circuit

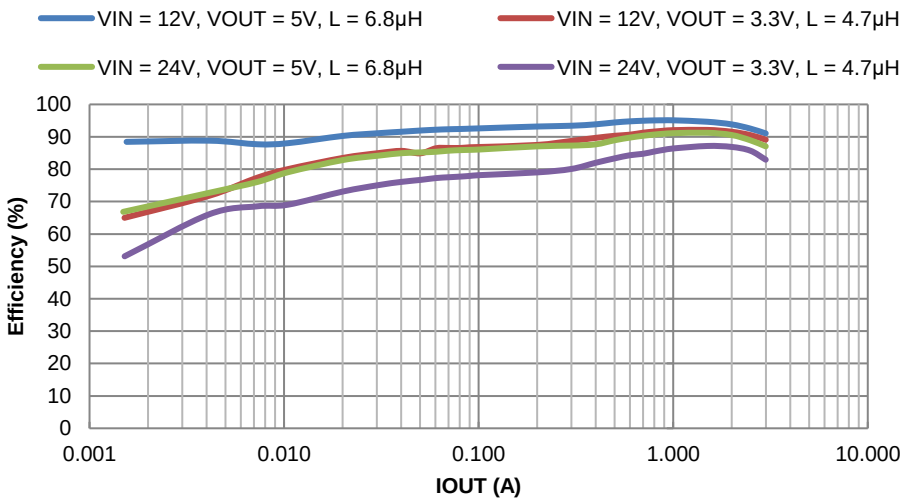

Figure 2. Efficiency vs. Output Current, AP63300Q

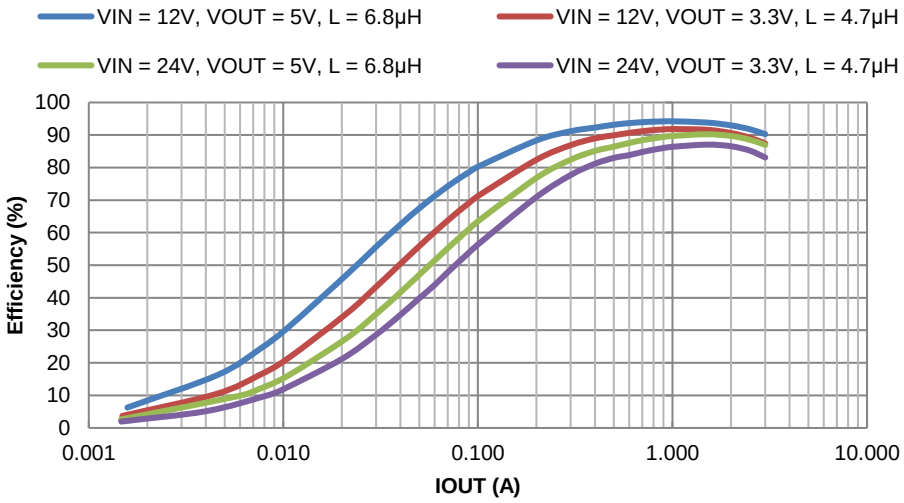

Figure 3. Efficiency vs. Output Current, AP63301Q

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Pin Descriptions

Pin Name	Pin Number	Function
FB	1	Feedback sensing terminal for the output voltage. Connect this pin to the resistive divider of the output. See **Setting the Output Voltage** section for more details.
EN	2	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator and low to turn it off. Connect to VIN or leave floating for automatic startup. The EN has a precision threshold of 1.18V for adjusting the UVLO. See **Enable** section for more details.
VIN	3	Power Input. VIN supplies the power to the IC as well as the step-down converter's power MOSFETs. Drive VIN with a 3.8V to 32V power source. Bypass VIN to GND with a suitably large capacitor to eliminate noise due to the switching of the IC. See **Input Capacitor** section for more details.
GND	4	Power Ground.
SW	5	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
BST	6	High-Side Gate Drive Boost Input. BST supplies the drive for the high-side N-channel power MOSFET. A 100nF capacitor is recommended from BST to SW to power the high-side driver.

Functional Block Diagram

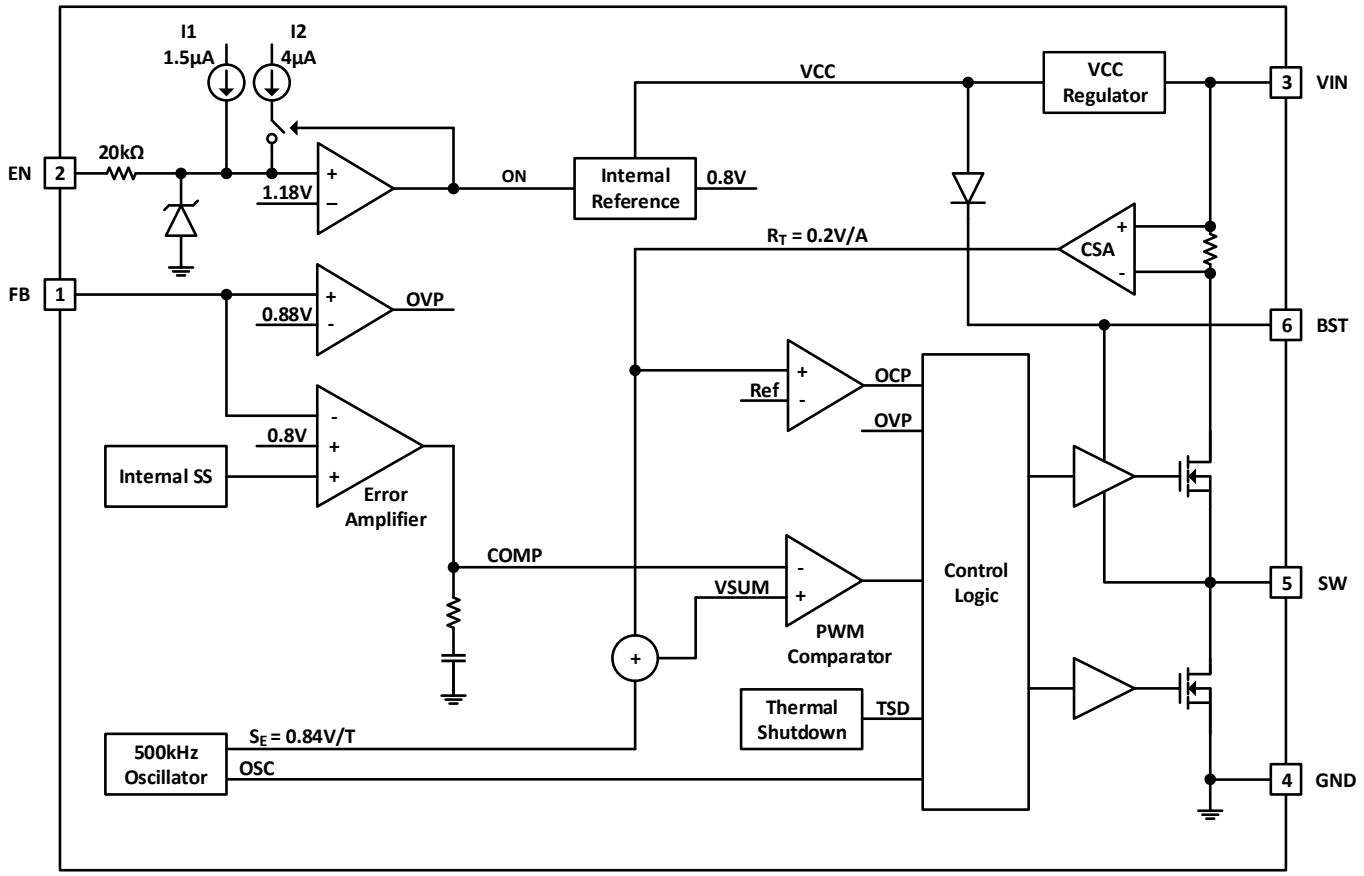

Figure 4. Functional Block Diagram

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Absolute Maximum Ratings (Note 4) (@ T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Rating	Unit
VIN	Supply Pin Voltage	-0.3 to +35.0 (DC) -0.3 to +40.0 (400ms)	V
V_{FB}	Feedback Pin Voltage	-0.3 to +6.0	V
V_{EN}	Enable/UVLO Pin Voltage	-0.3 to +35.0	V
V_{SW}	Switch Pin Voltage	-0.3 to VIN + 0.3 (DC) -2.5 to VIN + 2.0 (20ns)	V
V_{BST}	Bootstrap Pin Voltage	V_{SW} - 0.3 to V_{SW} + 6.0	V
T_{STG}	Storage Temperature	-65 to +150	°C
T_J	Junction Temperature	+160	°C
T_L	Lead Temperature	+260	°C
ESD Susceptibility (Note 5)			
HBM	Human Body Model	±3000	V
CDM	Charged Device Model	±2000	V

Notes: 4. Stresses greater than the *Absolute Maximum Ratings* specified above can cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability can be affected by exposure to absolute maximum rating conditions for extended periods of time.
5. Semiconductor devices are ESD sensitive and can be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

Thermal Resistance (Note 6)

Symbol	Parameter	Rating		Unit
θ_{JA}	Junction to Ambient	TSOT26	89	°C/W
θ_{JC}	Junction to Case	TSOT26	39	°C/W

Note: 6. Test condition for TSOT26: Device mounted on FR-4 substrate, single-layer PC board, 2oz copper, with minimum recommended pad layout.

Recommended Operating Conditions (Note 7) (@ T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
VIN	Supply Voltage	3.8	32	V
VOUT	Output Voltage	0.8	VIN	V
T_A	Operating Ambient Temperature	-40	+125	°C
T_J	Operating Junction Temperature	-40	+150	°C

Note: 7. The device function is not guaranteed outside of the recommended operating conditions.

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Electrical Characteristics (@ T_J = +25°C, VIN = 12V, unless otherwise specified. Min/Max limits apply across the recommended operating junction temperature range, -40°C to +150°C, and input voltage range, 3.8V to 32V, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{SHDN}	Shutdown Supply Current	V_{EN} = 0V	—	1	—	μA
I_Q	Quiescent Supply Current	AP63300Q: V_{EN} = Floating, V_{FB} = 1.0V	—	22	—	μA
		AP63301Q: V_{EN} = Floating, V_{FB} = 1.0V	—	280	—	μA
POR	VIN Power-on Reset Rising Threshold	—	—	3.5	3.7	V
UVLO	VIN Undervoltage Lockout Falling Threshold	—	—	3.06	—	V
$R_{DS(ON)1}$	High-Side Power MOSFET On-Resistance (Note 8)	—	—	75	—	mΩ
$R_{DS(ON)2}$	Low-Side Power MOSFET On-Resistance (Note 8)	—	—	40	—	mΩ
I_{PEAK_LIMIT}	HS Peak Current Limit (Note 8)	From Drain to Source	3.8	4.5	5.2	A
I_{VALLEY_LIMIT}	LS Valley Current Limit (Note 8)	From Source to Drain	—	4.0	—	A
f_{SW}	Oscillator Frequency	CCM	450	500	550	kHz
t_{ON_MIN}	Minimum On-Time	—	—	80	—	ns
V_{FB}	Feedback Voltage	CCM	0.792	0.800	0.808	V
V_{EN_H}	EN Logic High Threshold	—	—	1.18	1.25	V
V_{EN_L}	EN Logic Low Threshold	—	1.03	1.09	—	V
I_{EN}	EN Input Current	V_{EN} = 1.5V	—	5.5	—	μA
		V_{EN} = 1V	1.0	1.5	2.0	μA
t_{SS}	Soft-Start Time	—	—	4	—	ms
T_{SD}	Thermal Shutdown (Note 8)	—	—	+160	—	°C
T_{Hys}	Thermal Shutdown Hysteresis (Note 8)	—	—	+25	—	°C

Note: 8. Compliance to the datasheet limits is assured by one or more methods: production test, characterization, and/or design.

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Typical Performance Characteristics (AP63300Q/AP63301Q @ T_A = +25°C, VIN = 12V, VOUT = 5V, BOM = Table 1, unless otherwise specified.)

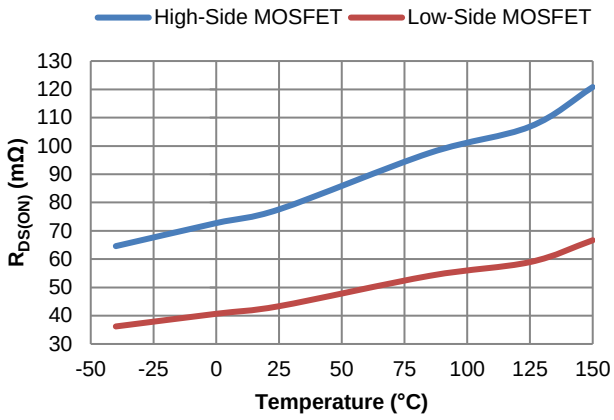

Figure 5. Power MOSFET $R_{DS(ON)}$ vs. Temperature

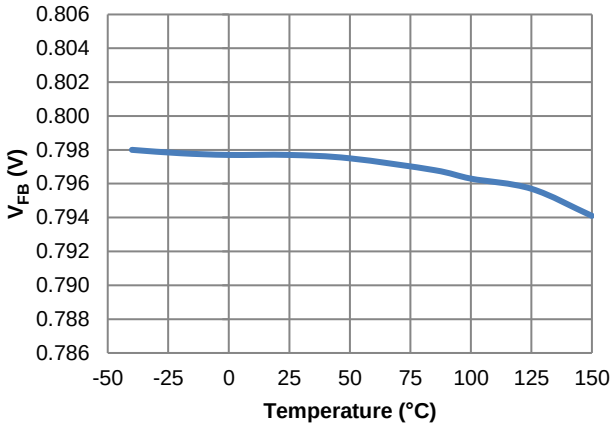

Figure 6. Feedback Voltage vs. Temperature, IOUT = 1A

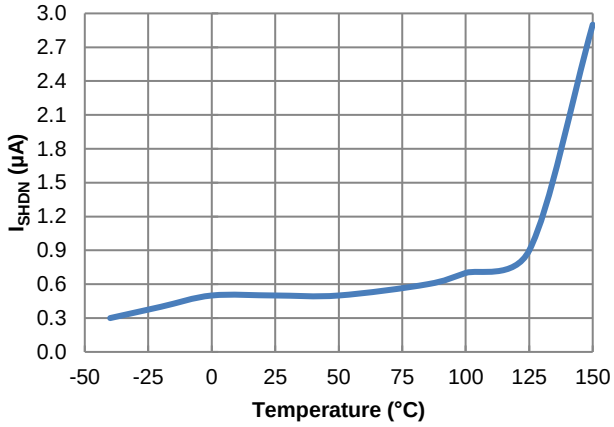

Figure 7. I_{SHDN} vs. Temperature

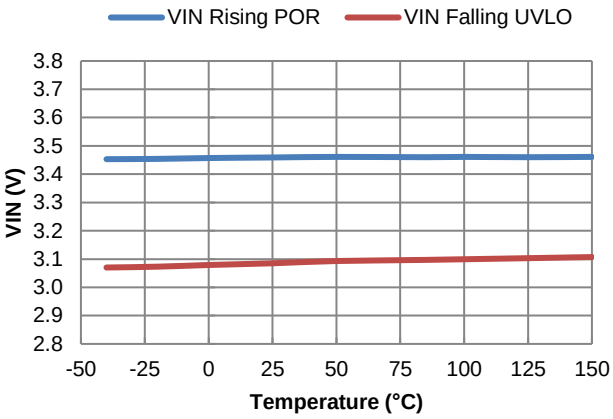

Figure 8. VIN Power-On Reset and UVLO vs. Temperature

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Typical Performance Characteristics (AP63300Q/AP63301Q @ T_A = +25°C, VIN = 12V, VOUT = 5V, BOM = Table 1, unless otherwise specified.) (continued)

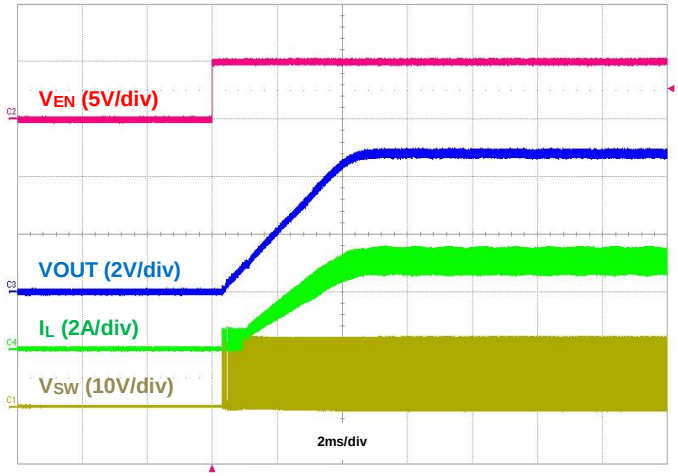

Figure 9. Startup using EN, IOUT = 3A

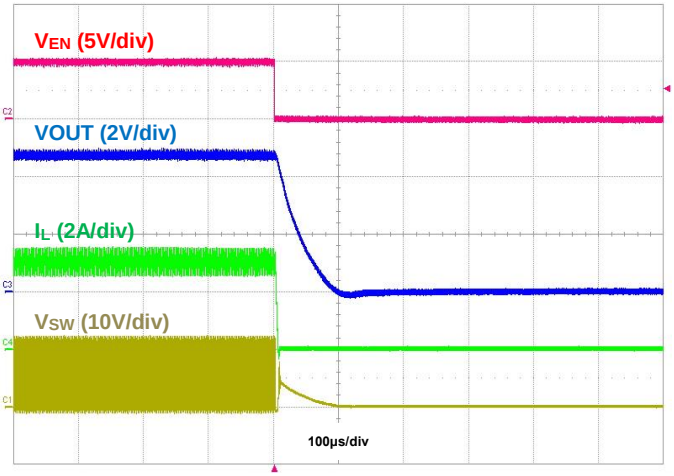

Figure 10. Shutdown using EN, IOUT = 3A

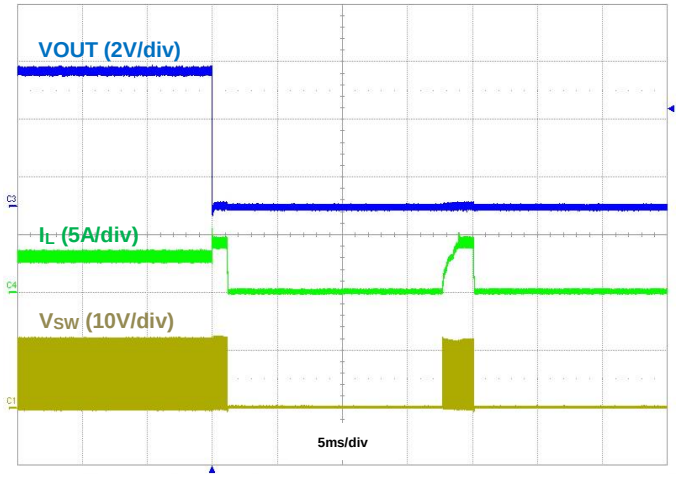

Figure 11. Output Short Protection, IOUT = 3A

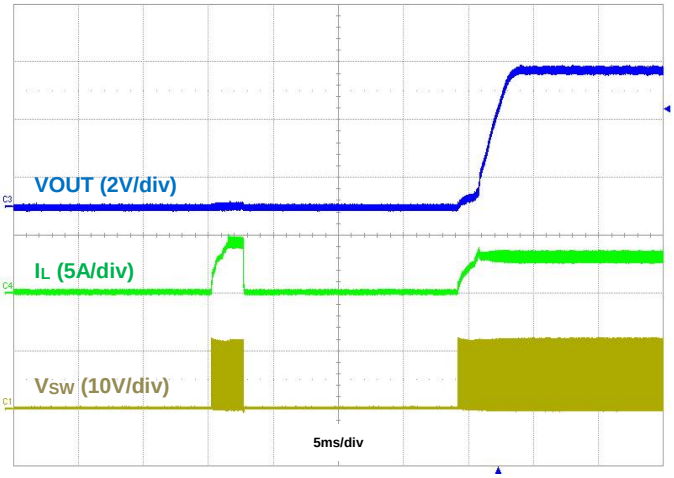

Figure 12. Output Short Recovery, IOUT = 3A

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Typical Performance Characteristics (AP63300Q @ T_A = +25°C, VIN = 12V, VOUT = 5V, BOM = Table 1, unless otherwise specified.)

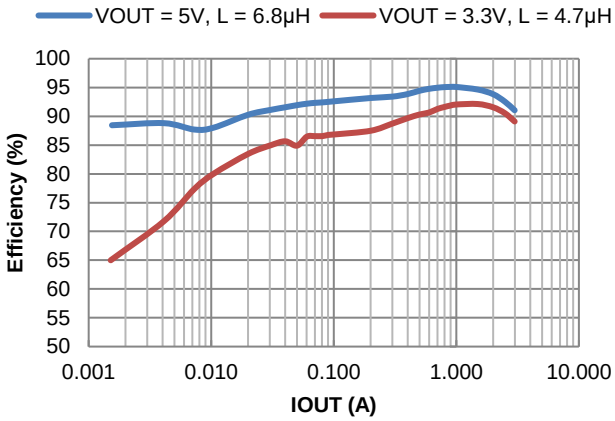

Figure 13. Efficiency vs. Output Current, VIN = 12V

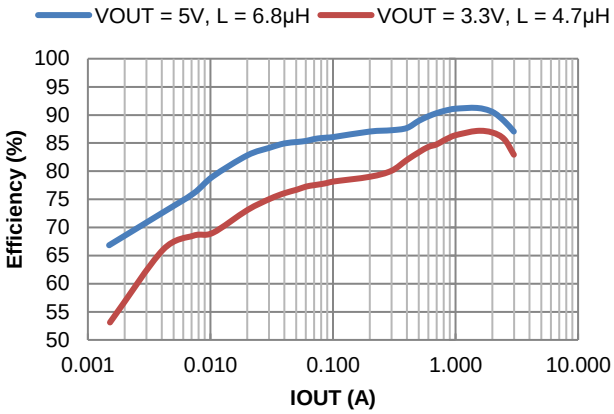

Figure 14. Efficiency vs. Output Current, VIN = 24V

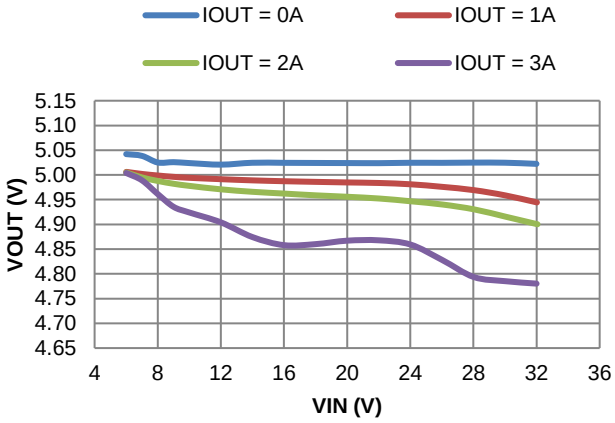

Figure 15. Line Regulation

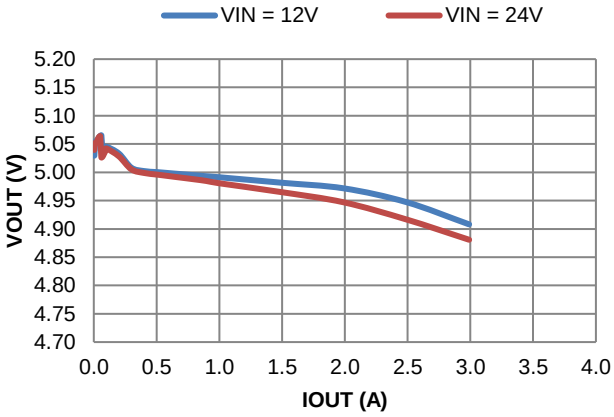

Figure 16. Load Regulation

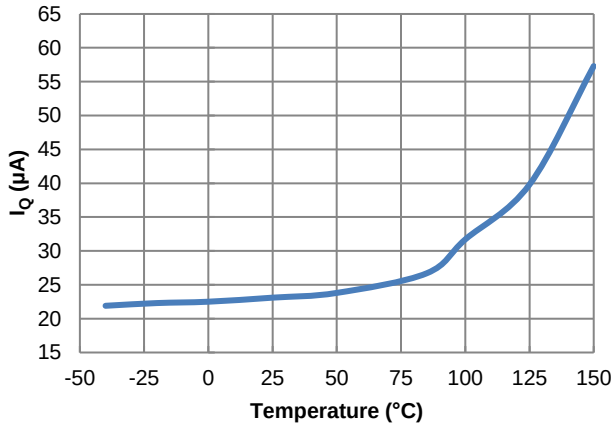

Figure 17. I_Q vs. Temperature

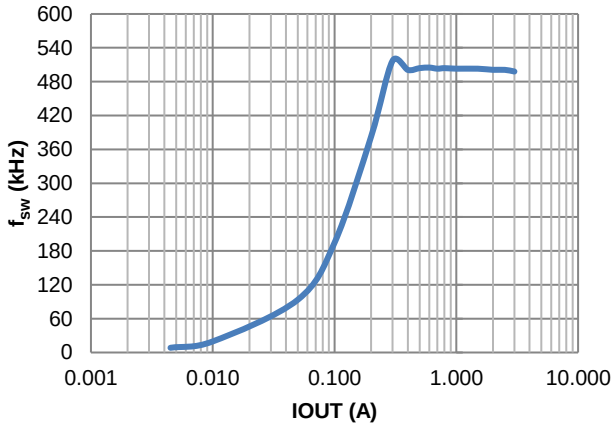

Figure 18. f_{sw} vs. Load

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Typical Performance Characteristics (AP63300Q @ T_A = +25°C, VIN = 12V, VOUT = 5V, BOM = Table 1, unless otherwise specified.) (continued)

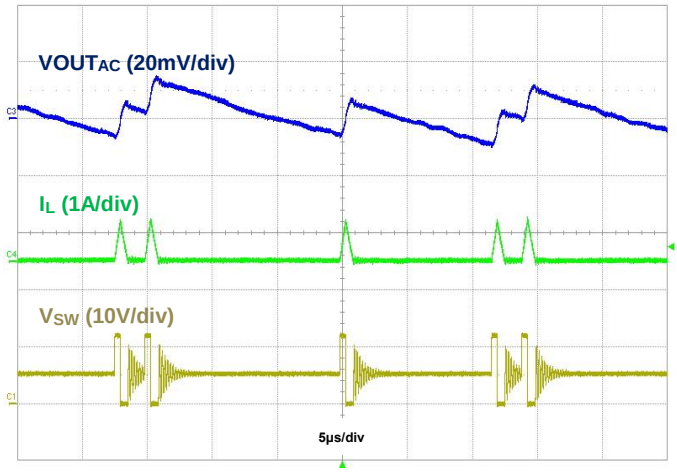

Figure 19. Output Voltage Ripple, VOUT = 5V, IOUT = 50mA

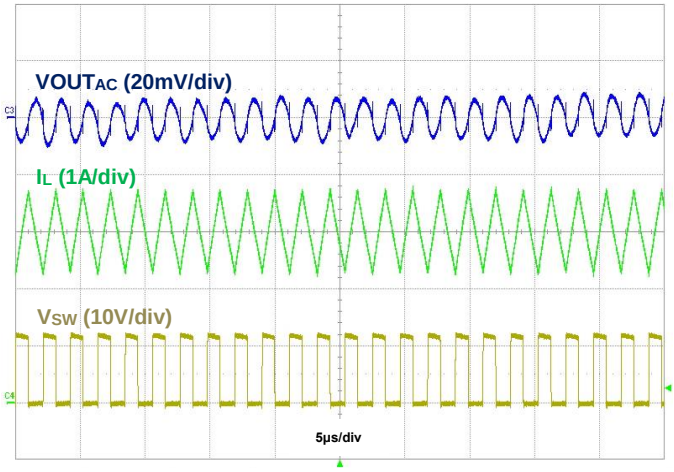

Figure 20. Output Voltage Ripple, VOUT = 5V, IOUT = 3A

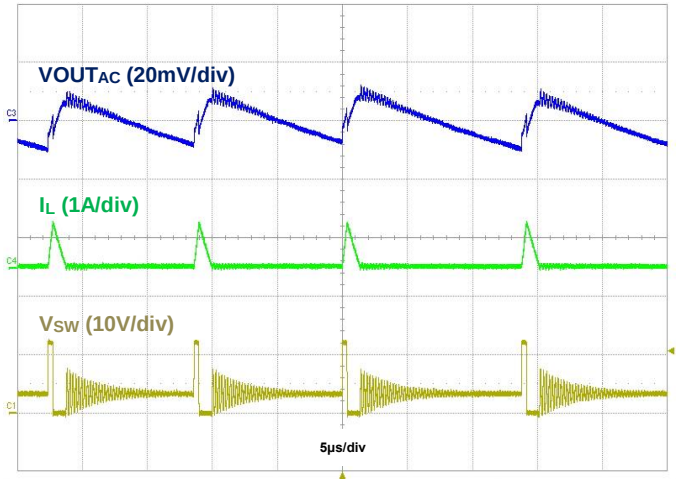

Figure 21. Output Voltage Ripple, VOUT = 3.3V, IOUT = 50mA

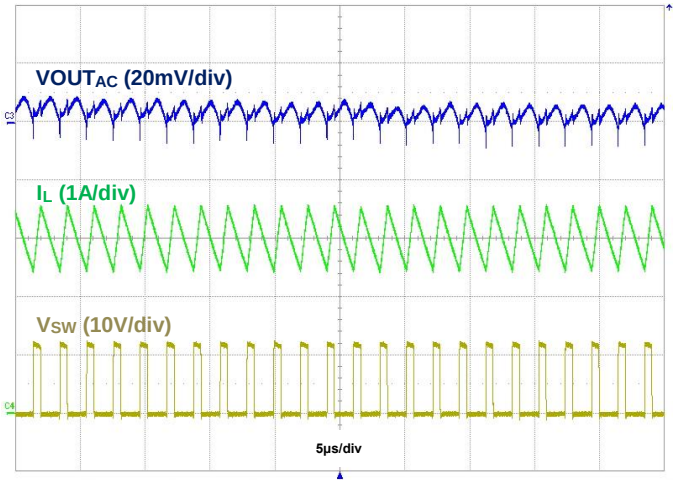

Figure 22. Output Voltage Ripple, VOUT = 3.3V, IOUT = 3A

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Typical Performance Characteristics (AP63300Q @ T_A = +25°C, VIN = 12V, VOUT = 5V, BOM = Table 1, unless otherwise specified.) (continued)

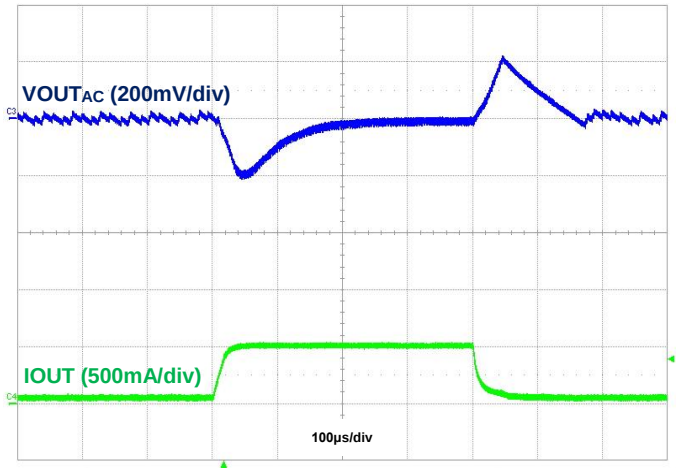

Figure 23. Load Transient, IOUT = 50mA to 500mA to 50mA

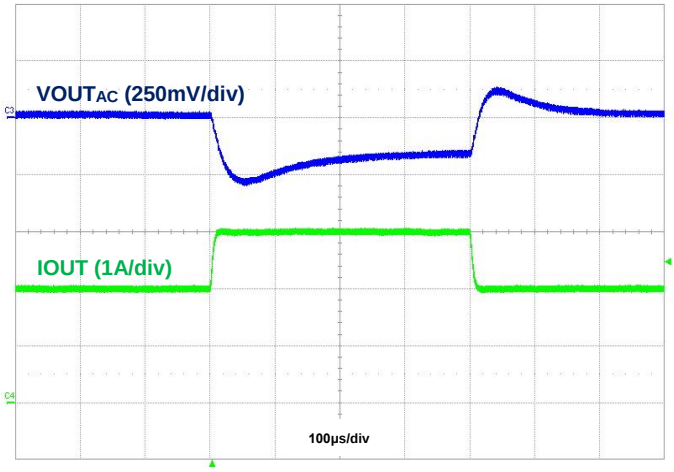

Figure 24. Load Transient, IOUT = 2A to 3A to 2A

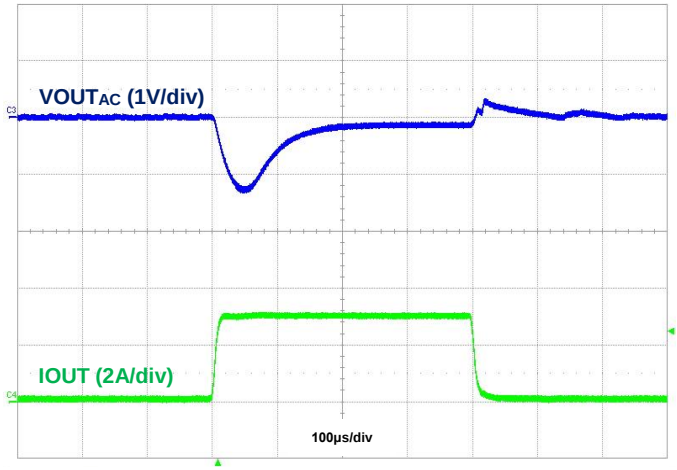

Figure 25. Load Transient, IOUT = 50mA to 3A to 50mA

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Typical Performance Characteristics (AP63301Q @ T_A = +25°C, VIN = 12V, VOUT = 5V, BOM = Table 1, unless otherwise specified.)

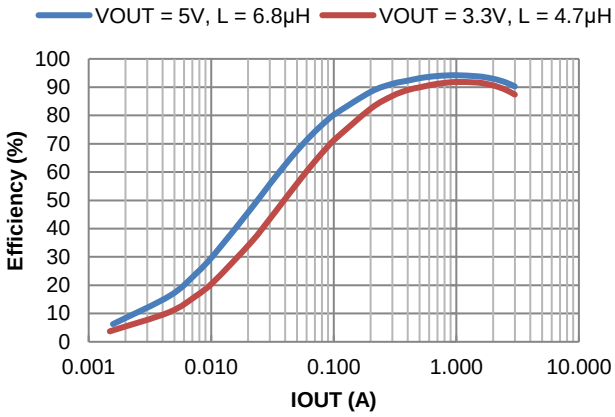

Figure 26. Efficiency vs. Output Current, VIN = 12V

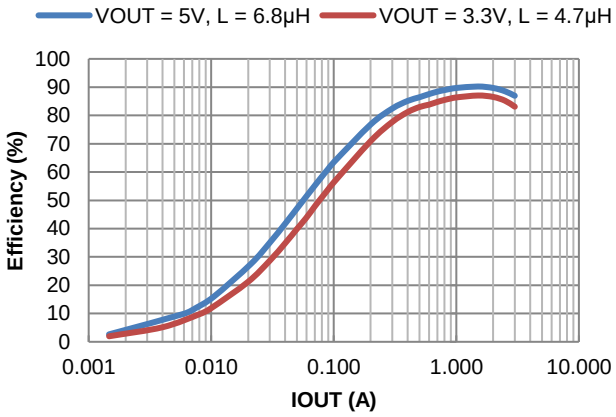

Figure 27. Efficiency vs. Output Current, VIN = 24V

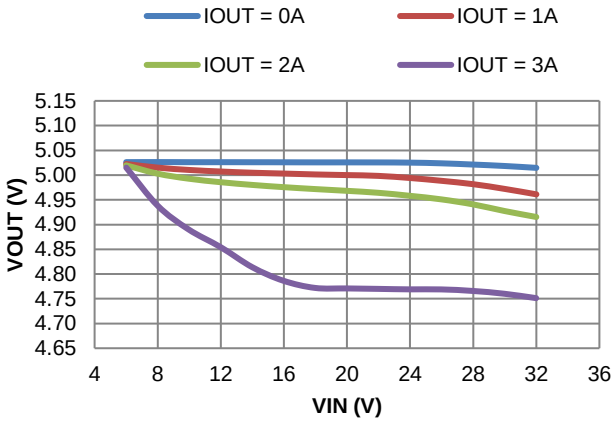

Figure 28. Line Regulation

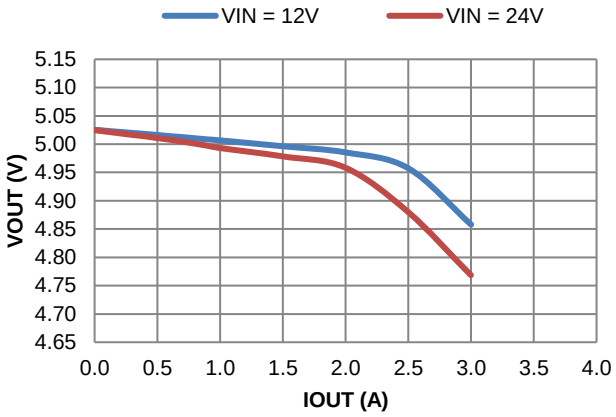

Figure 29. Load Regulation

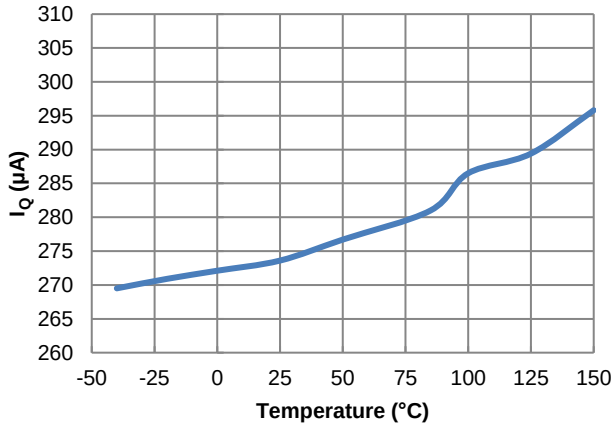

Figure 30. I_Q vs. Temperature

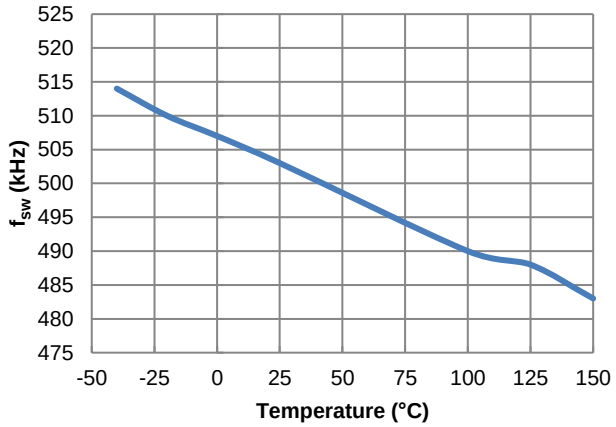

Figure 31. f_{sw} vs. Temperature, IOUT = 0A

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Typical Performance Characteristics (AP63301Q @ T_A = +25°C, VIN = 12V, VOUT = 5V, BOM = Table 1, unless otherwise specified.) (continued)

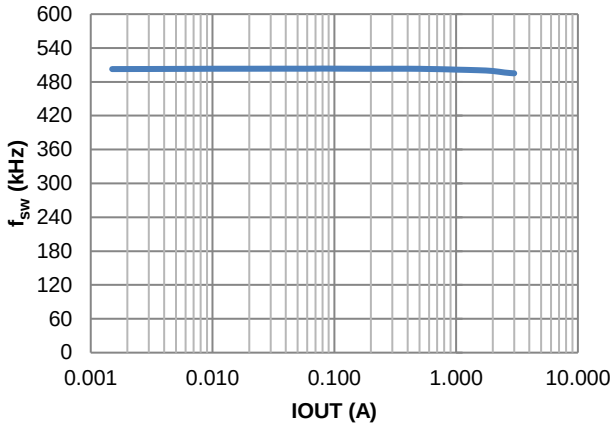

Figure 32. f_{sw} vs. Load

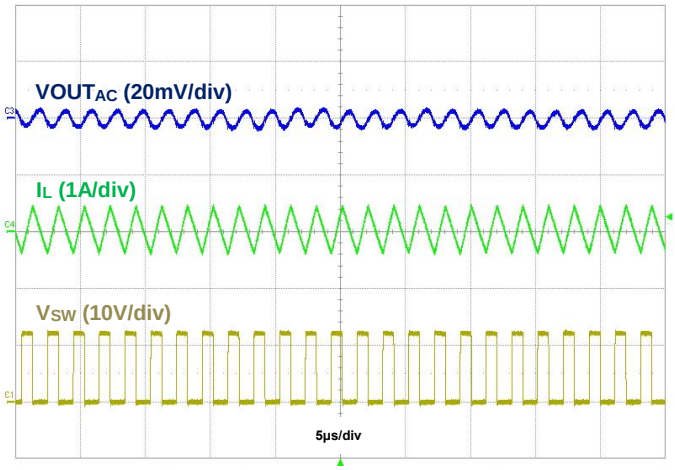

Figure 33. Output Voltage Ripple, VOUT = 5V, IOUT = 50mA

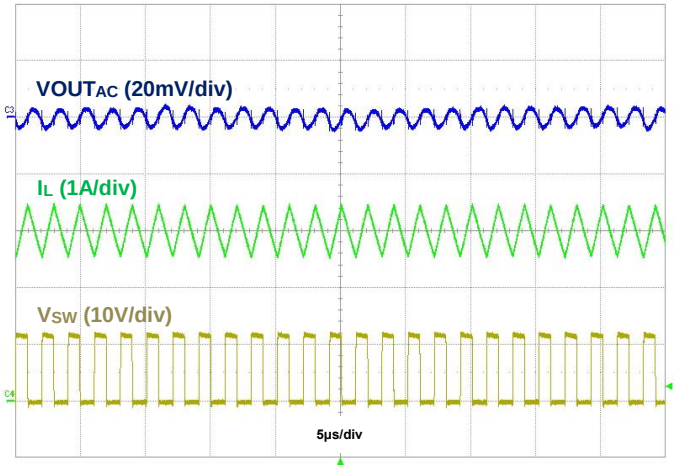

Figure 34. Output Voltage Ripple, VOUT = 5V, IOUT = 3A

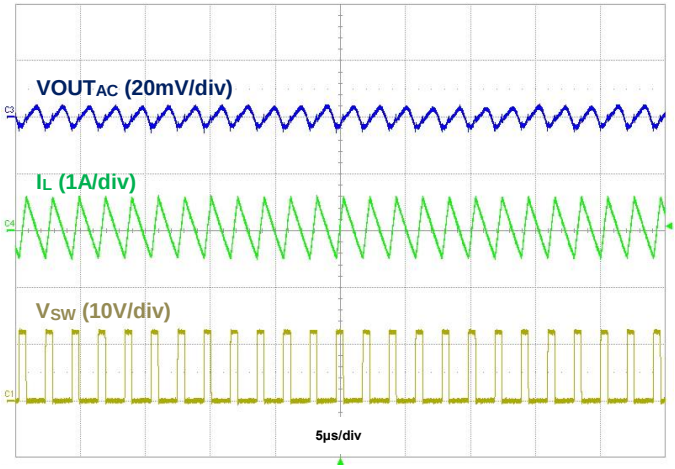

Figure 35. Output Voltage Ripple, VOUT = 3.3V, IOUT = 50mA

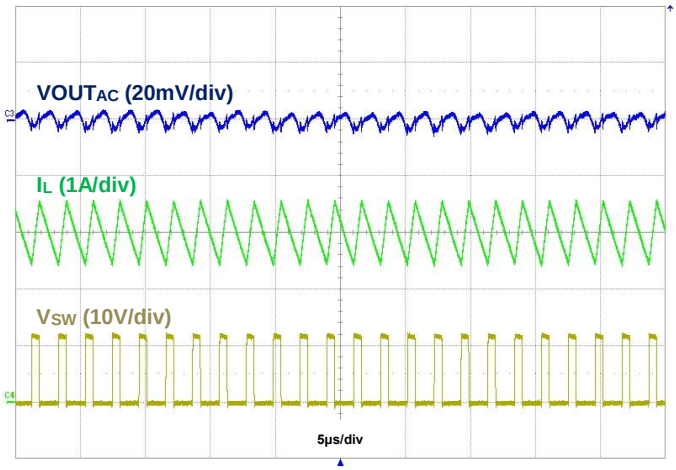

Figure 36. Output Voltage Ripple, VOUT = 3.3V, IOUT = 3A

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Typical Performance Characteristics (AP63301Q @ T_A = +25°C, VIN = 12V, VOUT = 5V, BOM = Table 1, unless otherwise specified.) (continued)

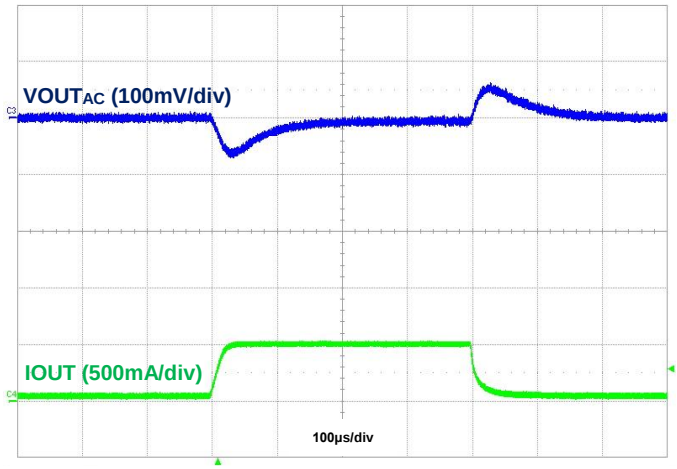

Figure 37. Load Transient, IOUT = 50mA to 500mA to 50mA

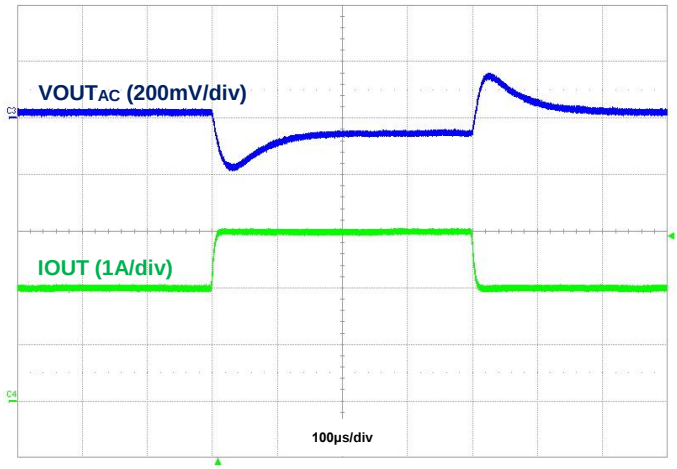

Figure 38. Load Transient, IOUT = 2A to 3A to 2A

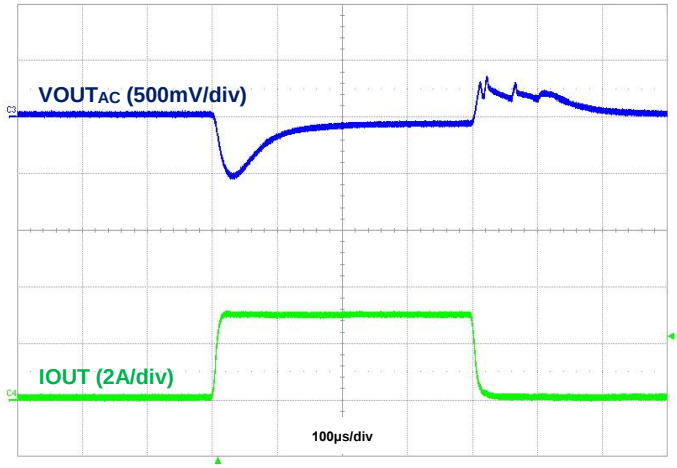

Figure 39. Load Transient, IOUT = 50mA to 3A to 50mA

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Application Information

1 Pulse Width Modulation (PWM) Operation

The AP63300Q/AP63301Q device is an automotive-compliant, 3.8V-to-32V input, 3A output, EMI friendly, fully integrated synchronous buck converter. Refer to the block diagram in Figure 4. The device employs fixed-frequency peak current mode control. The internal 500kHz clock's rising edge initiates turning on the integrated high-side power MOSFET, Q1, for each cycle. When Q1 is on, the inductor current rises linearly and the device charges the output capacitor. The current across Q1 is sensed and converted to a voltage with a ratio of R_T via the CSA block. The CSA output is combined with an internal slope compensation, S_E, resulting in V_{SUM}. When V_{SUM} rises higher than the COMP node, the device turns off Q1 and turns on the low-side power MOSFET, Q2. The inductor current decreases when Q2 is on. On the rising edge of next clock cycle, Q2 turns off and Q1 turns on. This sequence repeats every clock cycle.

The error amplifier generates the COMP voltage by comparing the voltage on the FB pin with an internal 0.8V reference. An increase in load current causes the feedback voltage to drop. The error amplifier thus raises the COMP voltage until the average inductor current matches the increased load current. This feedback loop regulates the output voltage. The internal slope compensation circuitry prevents subharmonic oscillation when the duty cycle is greater than 50% for peak current mode control.

The peak current mode control, integrated loop compensation network, and built-in 4ms soft-start time simplifies the AP63300Q/AP63301Q footprint as well as minimizes the external component count.

In order to provide a small output ripple during light load conditions, the AP63301Q operates in PWM regardless of output load.

2 Pulse Frequency Modulation (PFM) Operation

In heavy load conditions, the AP63300Q operates in forced PWM mode. As the load current decreases, the internal COMP node voltage also decreases. At a certain limit, if the load current is low enough, the COMP node voltage is clamped and is prevented from decreasing any further. The voltage at which COMP is clamped corresponds to the 930mA PFM peak inductor current limit. As the load current approaches zero, the AP63300Q enters PFM mode to increase the converter power efficiency at light load conditions. When the inductor current decreases to 60mA, zero cross detection circuitry on the low-side power MOSFET, Q2, forces it off. The buck converter does not sink current from the output when the output load is light and while the device is in PFM. Because the AP63300Q works in PFM during light load conditions, it can achieve power efficiency of up to 88% at a 5mA load condition.

The quiescent current of AP63300Q is 22μA typical under a no-load, non-switching condition.

3 Enable

When disabled, the device shutdown supply current is only 1μA. When applying a voltage greater than the EN logic high threshold (typical 1.18V, rising), the AP63300Q/AP63301Q enables all functions and the device initiates the soft-start phase. The EN pin is a high-voltage pin and can be directly connected to VIN to automatically start up the device as VIN increases. An internal 1.5μA pull-up current source connected from the internal LDO-regulated VCC to the EN pin guarantees that if EN is left floating, the device still automatically enables once the voltage reaches the EN logic high threshold. The AP63300Q/AP63301Q has a built-in 4ms soft-start time to prevent output voltage overshoot and inrush current. When the EN voltage falls below its logic low threshold (typical 1.09V, falling), the internal SS voltage discharges to ground and device operation disables.

The EN pin can also be used to adjust the undervoltage lockout thresholds. See **Undervoltage Lockout (UVLO)** section for more details.

Alternatively, a small ceramic capacitor can be added from EN to GND. When EN is not driven externally, this capacitor increases the time needed for the EN pin voltage to reach its logic high threshold, which delays the startup of the output voltage. This is useful when sequencing multiple power rails to minimize input inrush current. When the EN pin voltage starts from 0V, the amount of capacitance for a given delay time is approximated by:

$$C_d[nF] \approx 1.27 \cdot t_d[ms] \quad \text{Eq. 1}$$

Where:

- C_d is the time delay capacitance in nF
- t_d is the delay time in ms

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Application Information (continued)

4 Electromagnetic Interference (EMI) Reduction with Ringing-Free Switching Node and Frequency Spread Spectrum (FSS)

In some applications, the system must meet EMI standards. In relation to high frequency radiation EMI noise, the switching node's (SW's) ringing amplitude is especially critical. To dampen high frequency radiated EMI noise, the AP63300Q/AP63301Q device implements a proprietary, multi-level gate driver scheme that achieves a ringing-free switching node without sacrificing the switching node's rise and fall slew rates as well as the converter's power efficiency.

To further improve EMI reduction, the AP63300Q device also implements FSS with a switching frequency jitter of ±6%. FSS reduces conducted and radiated interference at a particular frequency by spreading the switching noise over a wider frequency band and by not allowing emitted energy to stay in any one frequency for a significant period of time.

5 Adjusting Undervoltage Lockout (UVLO)

Undervoltage lockout is implemented to prevent the IC from insufficient input voltages. The AP63300Q/AP63301Q device has a UVLO comparator that monitors the input voltage and the internal bandgap reference. The AP63300Q/AP63301Q disables if the input voltage falls below 3.06V. In this UVLO event, both the high-side and low-side power MOSFETs turn off.

Some applications may desire higher VIN UVLO threshold voltages than is provided by the default setup. A 4µA hysteresis pull-up current source on the EN pin along with an external resistive divider (R3 and R4) configures the VIN UVLO threshold voltages as shown in Figure 40.

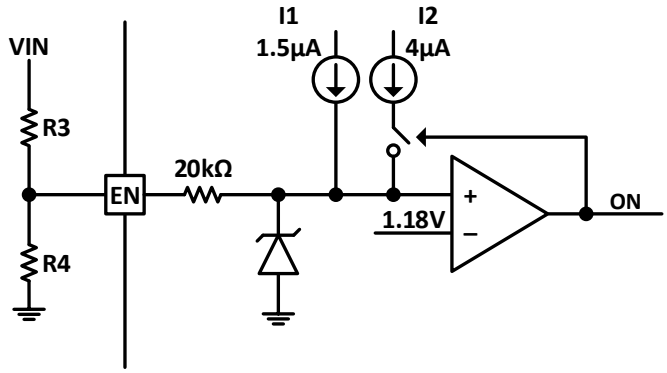

Figure 40. Adjusting UVLO

The resistive divider resistor values are calculated by:

$$R3 = \frac{0.924 \cdot V_{ON} - V_{OFF}}{4.114\mu A} \quad \text{Eq. 2}$$

$$R4 = \frac{1.09 \cdot R3}{V_{OFF} - 1.09V + 5.5\mu A \cdot R3} \quad \text{Eq. 3}$$

Where:

- V_{ON} is the rising edge VIN voltage to enable the regulator and is greater than 3.7V
- V_{OFF} is the falling edge VIN voltage to disable the regulator and is greater than 3.26V

6 Output Overvoltage Protection (OVP)

The AP63300Q/AP63301Q implements output OVP circuitry to minimize output voltage overshoots during decreasing load transients. The high-side power MOSFET turns off, and the low-side power MOSFET turns on, when the feedback voltage exceeds 110% of the 0.8V internal reference voltage in order to prevent the output voltage from continuing to increase.

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Application Information (continued)

7 Overcurrent Protection (OCP)

The AP63300Q/AP63301Q has cycle-by-cycle peak current limit protection by sensing the current through the internal high-side power MOSFET, Q1. While Q1 is on, the internal sensing circuitry monitors its conduction current. Once the current through Q1 exceeds the peak current limit, Q1 immediately turns off. If Q1 consistently hits the peak current limit for 512 cycles, the buck converter enters hiccup mode and shuts down. After 8192 cycles of down time, the buck converter restarts powering up. Hiccup mode reduces the power dissipation in the overcurrent condition.

8 Thermal Shutdown (TSD)

If the junction temperature of the device reaches the thermal shutdown limit of +160°C, the AP63300Q/AP63301Q shuts down both its high-side and low-side power MOSFETs. When the junction temperature reduces to the required level (+135°C typical), the device initiates a normal power-up cycle with soft-start.

9 Power Derating Characteristics

To prevent the regulator from exceeding the maximum recommended operating junction temperature, some thermal analysis is required. The regulator's temperature rise is given by:

$$T_{RISE} = PD \cdot (\theta_{JA}) \quad \text{Eq. 4}$$

Where:

- PD is the power dissipated by the regulator
- θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature

The junction temperature, T_J, is given by:

$$T_J = T_A + T_{RISE} \quad \text{Eq. 5}$$

Where:

- T_A is the ambient temperature of the environment

For the TSOT26 package, the θ_{JA} is 89°C/W. The actual junction temperature should not exceed the maximum recommended operating junction temperature of +150°C when considering the thermal design. Figure 41 shows a typical derating curve versus ambient temperature.

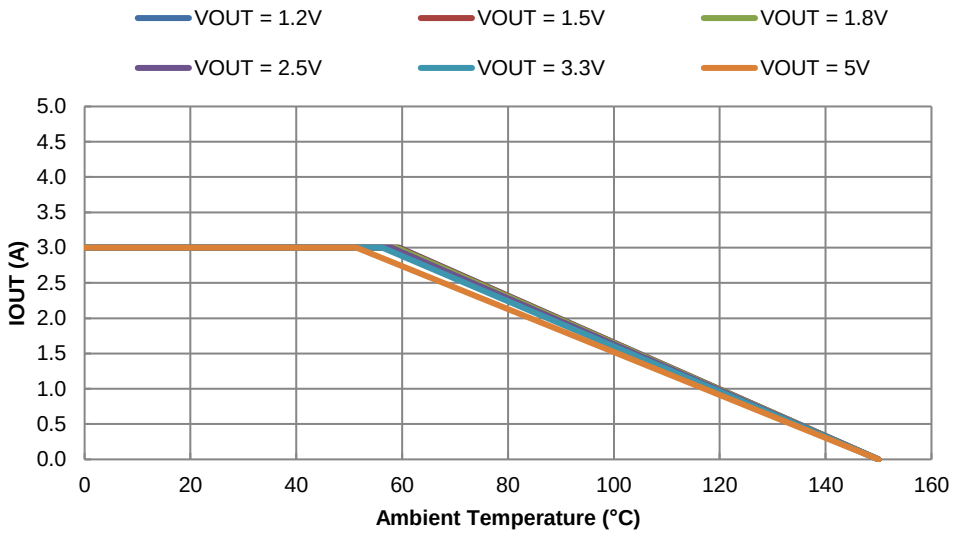

Figure 41. Output Current Derating Curve vs. Ambient Temperature, VIN = 12V

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Application Information (continued)

10 Setting the Output Voltage

The AP63300Q/AP63301Q has adjustable output voltages starting from 0.8V using an external resistive divider. An optional external capacitor, C4 in Figure 1, of 10pF to 220pF improves the transient response. The resistor values of the feedback network are selected based on a design trade-off between efficiency and output voltage accuracy. There is less current consumption in the feedback network for high resistor values, which improves efficiency at light loads. However, values too high cause the device to be more susceptible to noise affecting its output voltage accuracy. R1 can be determined by the following equation:

$$\mathbf{R1 = R2 \cdot \left(\frac{VOUT}{0.8V} - 1\right)} \quad \textbf{Eq. 6}$$

Table 1 shows a list of recommended component selections for common AP63300Q/AP63301Q output voltages referencing Figure 1.

Table 1. Recommended Component Selections

AP63300Q/AP63301Q							
Output Voltage (V)	**R1 (kΩ)**	**R2 (kΩ)**	**L (µH)**	**C1 (µF)**	**C2 (µF)**	**C3 (nF)**	**C4 (pF)**
1.2	15.0	30.1	2.2	10	3 x 22	100	OPEN
1.5	26.1	30.1	3.3	10	3 x 22	100	OPEN
1.8	37.4	30.1	3.3	10	2 x 22	100	OPEN
2.5	63.4	30.1	4.7	10	2 x 22	100	56
3.3	93.1	30.1	4.7	10	2 x 22	100	56
5.0	158.0	30.1	6.8	10	2 x 22	100	47
12.0	422.0	30.1	10.0	10	2 x 22	100	12

11 Inductor

Calculating the inductor value is a critical factor in designing a buck converter. For most designs, the following equation can be used to calculate the inductor value:

$$\mathbf{L = \frac{VOUT \cdot (VIN - VOUT)}{VIN \cdot \Delta I_L \cdot f_{sw}}} \quad \textbf{Eq. 7}$$

Where:

- ΔI_L is the inductor current ripple
- f_{SW} is the buck converter switching frequency

For AP63300Q/AP63301Q, choose ΔI_L to be 30% to 40% of the maximum load current of 3A.

The inductor peak current is calculated by:

$$\mathbf{I_{L_{PEAK}} = I_{LOAD} + \frac{\Delta I_L}{2}} \quad \textbf{Eq. 8}$$

Peak current determines the required saturation current rating, which influences the size of the inductor. Saturating the inductor decreases the converter efficiency while increasing the temperatures of the inductor and the internal power MOSFETs. Therefore, choosing an inductor with the appropriate saturation current rating is important. For most applications, it is recommended to select an inductor of approximately 2.2µH to 10µH with a DC current rating of at least 35% higher than the maximum load current. For highest efficiency, the inductor's DC resistance should be less than 30mΩ. Use a larger inductance for improved efficiency under light load conditions.

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Application Information (continued)

11 Input Capacitor

The input capacitor reduces both the surge current drawn from the input supply as well as the switching noise from the device. The input capacitor must sustain the ripple current produced during the on-time of Q1. It must have a low ESR to minimize power dissipation due to the RMS input current.

The RMS current rating of the input capacitor is a critical parameter and must be higher than the RMS input current. As a rule of thumb, select an input capacitor with an RMS current rating greater than half of the maximum load current.

Due to large dI/dt through the input capacitor, electrolytic or ceramic capacitors with low ESR should be used. If using a tantalum capacitor, it must be surge protected or else capacitor failure could occur. Using a ceramic capacitor of 10µF or greater is sufficient for most applications.

12 Output Capacitor

The output capacitor keeps the output voltage ripple small, ensures feedback loop stability, and reduces both the overshoots and undershoots of the output voltage during load transients. During the first few microseconds of an increasing load transient, the converter recognizes the change from steady-state and enters 100% duty cycle to supply more current to the load. However, the inductor limits the change to increasing current depending on its inductance. Therefore, the output capacitor supplies the difference in current to the load during this time. Likewise, during the first few microseconds of a decreasing load transient, the converter recognizes the change from steady-state and sets the on-time to minimum to reduce the current supplied to the load. However, the inductor limits the change in decreasing current as well. Therefore, the output capacitor absorbs the excess current from the inductor during this time.

The effective output capacitance, COUT, requirements can be calculated from the equations below.

The ESR of the output capacitor dominates the output voltage ripple. The amount of ripple can be calculated by:

$$\mathbf{VOUT_{Ripple}} = \mathbf{\Delta I_L} \cdot \left(\mathbf{ESR} + \frac{\mathbf{1}}{\mathbf{8} \cdot \mathbf{f_{sw}} \cdot \mathbf{COUT}} \right) \quad \textbf{Eq. 9}$$

Output capacitors with large capacitance and low ESR are the best option. For most applications, a total capacitance of 2 x 22µF to 3 x 22µF using ceramic capacitors is sufficient. To meet the load transient requirements, the calculated COUT should satisfy the following inequality:

$$\mathbf{COUT} > \mathbf{max}\left(\frac{\mathbf{L} \cdot \mathbf{I_{Trans}^2}}{\mathbf{\Delta V_{Overshoot}} \cdot \mathbf{VOUT}}, \frac{\mathbf{L} \cdot \mathbf{I_{Trans}^2}}{\mathbf{\Delta V_{Undershoot}} \cdot (\mathbf{VIN} - \mathbf{VOUT})} \right) \quad \textbf{Eq. 10}$$

Where:

- I_{Trans} is the load transient
- $\Delta V_{Overshoot}$ is the maximum output overshoot voltage
- $\Delta V_{Undershoot}$ is the maximum output undershoot voltage

14 Bootstrap Capacitor and Low-Dropout (LDO) Operation

To ensure proper operation, a ceramic capacitor must be connected between the BST and SW pins to supply the drive voltage for the high-side power MOSFET. A 100nF ceramic capacitor is sufficient. If the bootstrap capacitor voltage falls below 2.3V, the boot undervoltage protection circuit turns Q2 on for 220ns to refresh the bootstrap capacitor and raise its voltage back above 2.85V. The bootstrap capacitor's voltage is always maintained to ensure enough driving capability for Q1. This operation may arise during long periods of no switching such as in PFM with light load conditions. Another event that requires the refreshing of the bootstrap capacitor is when the input voltage drops close to the output voltage. Under this condition, the regulator enters low-dropout mode by holding Q1 on for multiple clock cycles. To prevent the bootstrap capacitor from discharging, Q2 is forced to refresh. The effective duty cycle is approximately 100% so that it acts as an LDO to maintain the output voltage regulation.

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Layout

PCB Layout

1. The AP63300Q/AP63301Q works at 3A load current so heat dissipation is a major concern in the layout of the PCB. 2oz copper for both the top and bottom layers is recommended.
2. Place the input capacitors as closely across VIN and GND as possible.
3. Place the inductor as close to SW as possible.
4. Place the output capacitors as close to GND as possible.
5. Place the feedback components as close to FB as possible.
6. If using four or more layers, use at least the 2nd and 3rd layers as GND to maximize thermal performance.
7. Add as many vias as possible around both the GND pin and under the GND plane for heat dissipation to all the GND layers.
8. Add as many vias as possible around both the VIN pin and under the VIN plane for heat dissipation to all the VIN layers.
9. See Figure 42 for more details.

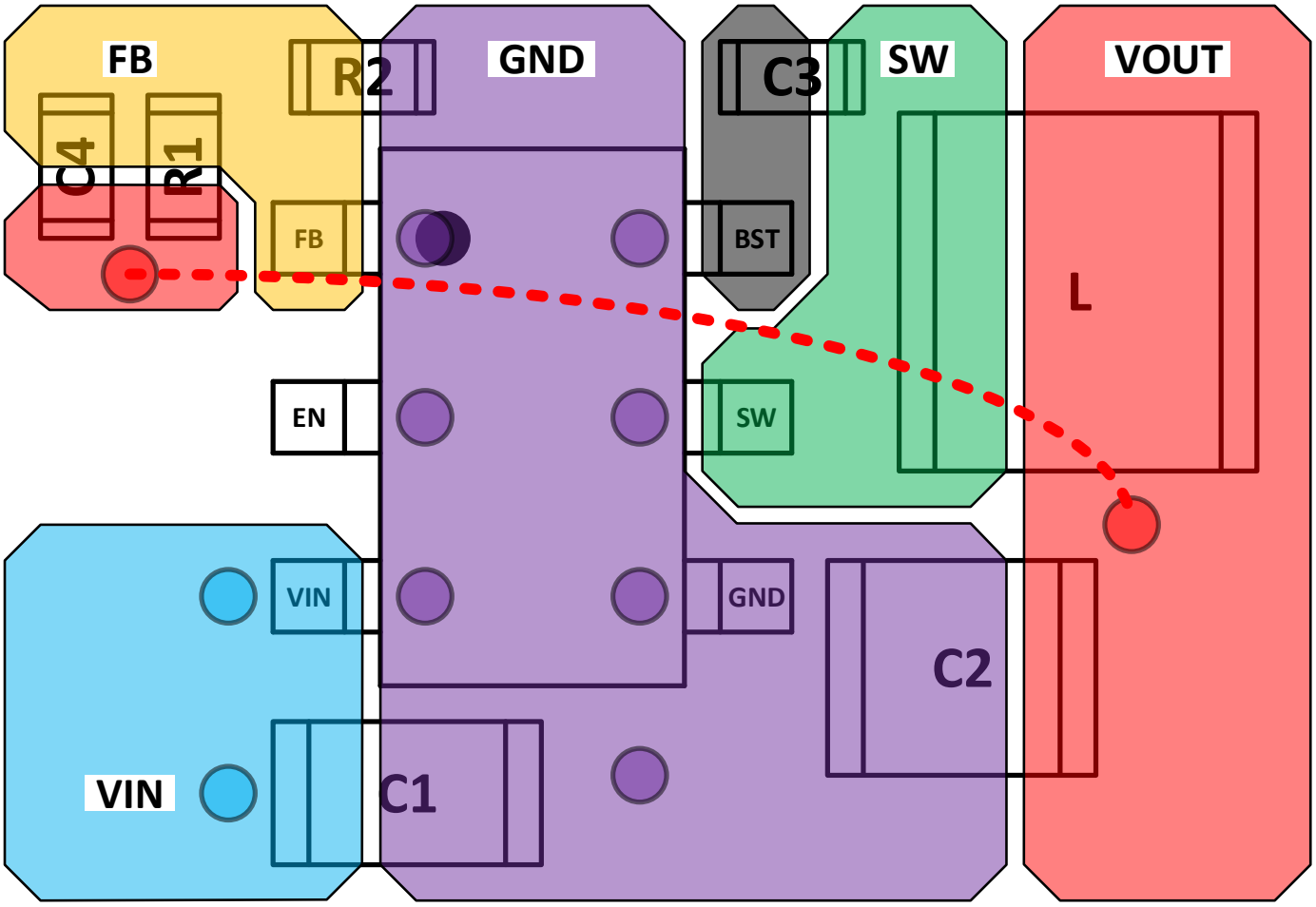

Figure 42. Recommended PCB Layout

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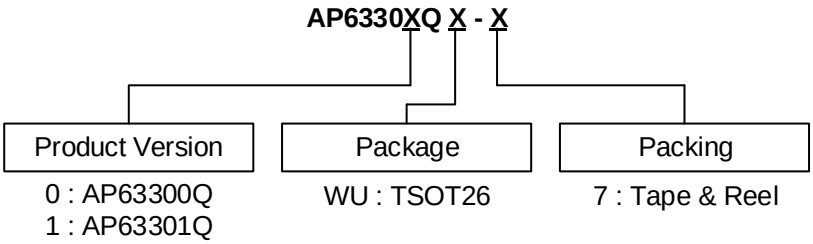
Ordering Information

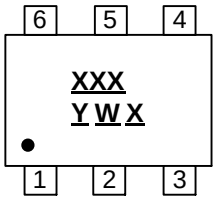


Part Number	Operation Mode	FSS Feature	Package Code	Tape and Reel	
				Quantity	Part Number Suffix
AP63300QWU-7	PFM/PWM	Yes	WU	3,000	-7
AP63301QWU-7	PWM Only	No	WU	3,000	-7

Marking Information

TSOT26

(Top View)



XXX : Identification Code
Y : Year 0~9
W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents
52 and 53 week
X : Internal Code

Part Number	Package	Identification Code
AP63300QWU-7	TSOT26	T6Q
AP63301QWU-7	TSOT26	T7Q

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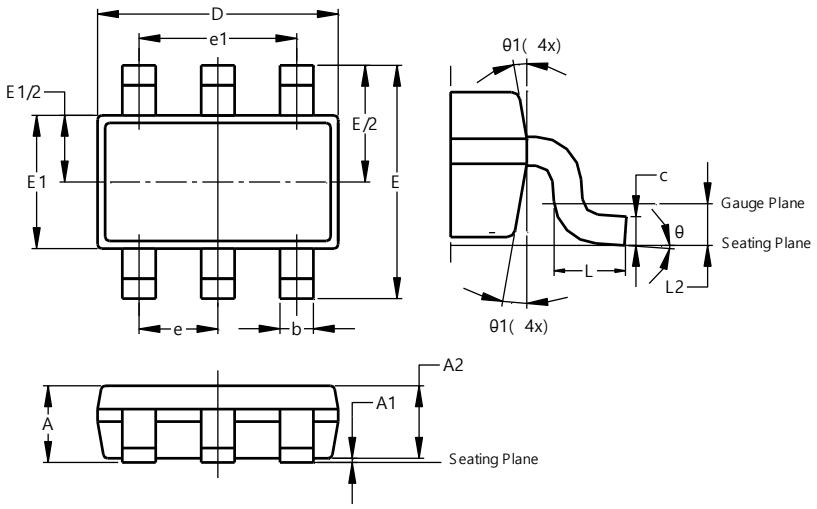
Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

TSOT26

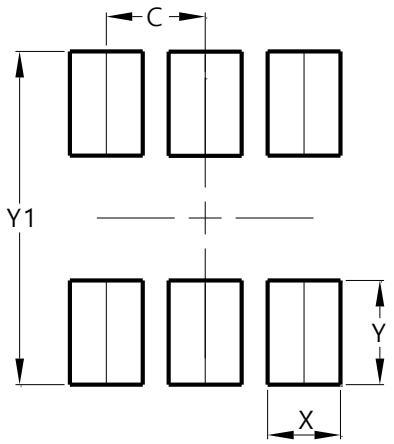


TSOT26			
Dim	**Min**	**Max**	**Typ**
A	—	1.00	—
A1	0.010	0.100	—
A2	0.840	0.900	—
D	2.800	3.000	2.900
E	2.800 BSC		
E1	1.500	1.700	1.600
b	0.300	0.450	—
c	0.120	0.200	—
e	0.950 BSC		
e1	1.900 BSC		
L	0.30	0.50	—
L2	0.250 BSC		
θ	0°	8°	4°
θ1	4°	12°	—
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

TSOT26



Dimensions	Value (in mm)
C	0.950
X	0.700
Y	1.000
Y1	3.200

Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.013 grams (Approximate)

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