

Dual Channel LDO Regulators with Enable Function

Features

- I Dropout : 150mV @ 100mA ($V_{OUT} \geq 2.8V$)
- I Operating Voltage Range : +2.7V to +7.0V
- I Output Voltage Range : +1.2V to +3.9V
- I Output Current : 250 mA / Channel (Typ.)
- I Low Power Consumption :
8 μ A (Typ.) / Channel
- I Standby Current : 0.01 μ A (Typ.)
- I Highly Accurate : $\pm 2\%$ ($V_{OUT} \geq 2.0V$)
- I High Ripple Rejection Rate : 70 dB
- I Output Current Limit Protection :
350mA / Channel
- I Short Circuit Protection (150mA)
- I Output ON/OFF Control Function
- I Low ESR Capacitor Compatible
- I SOT-26, UFN-6 Packages
- I RoHS Compliant and 100% Lead (Pb)-Free and Green (Halogen Free with Commercial Standard)

Applications

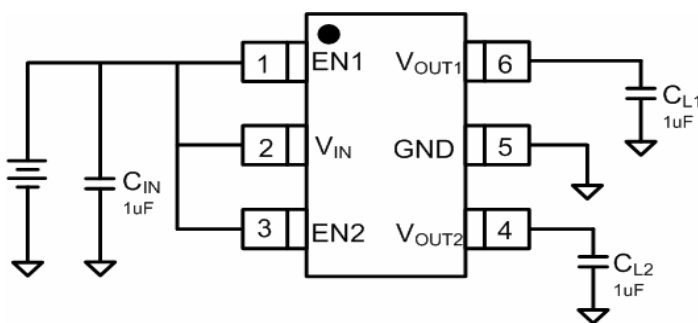
- | | |
|---|---|
| <ul style="list-style-type: none"> I Mobile phones (PDC, GSM, CDMA, IMT2000 etc.) and Cordless phones I Radio communication equipment | <ul style="list-style-type: none"> I Portable games I Cameras, Video recorders I Portable AV equipment |
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General Description

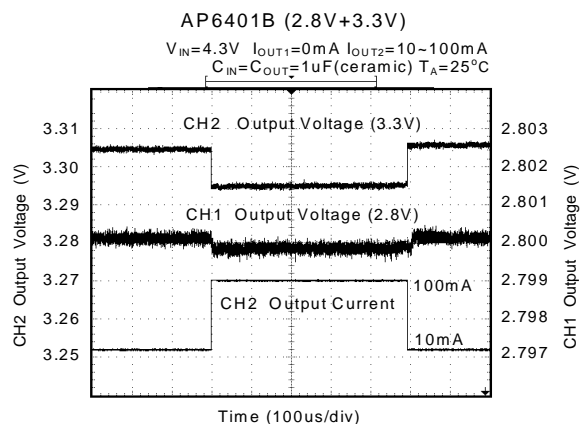
The AP6401 series are highly accurate, dual, low noise, CMOS LDO voltage regulators with enable function. The EN function allows the output of each regulator to be turned off independently, resulting in greatly reduced power consumption. The AP6401 series have the soft start function to suppress the inrush current. The current limiters' fold back circuit (it happens when over 350mA per channel) also operates as a short protection for the output current limiter. The output voltage for each regulator is set independently by metal trimming. It's also available to offer the honors other types of V_{OUT} between +1.2V ~+3.9V except the options shown on ordering information.

This series are fully compatible with low ESR ceramic capacitors, reducing cost and improving output stability. This high level output stability is maintained even during frequent load fluctuations, due to the excellent transient response performance and high PSRR achieved across a broad range of frequency. It is available in the SOT26, UFN-6 and DFN-6 'chip-scaled' package.

Simplified Application Circuit



Cross Talk



Ordering Information

<p>AP6401 - </p> <p style="margin-left: 100px;">└─ Package Code</p> <p style="margin-left: 60px;">└─ Lead Free Code</p> <p style="margin-left: 10px;">└─ Output Type Code</p>	<p>Output Type Code : ($V_{OUT1}+V_{OUT2}$)</p> <table style="width: 100%; border: none;"> <tr> <td>A : 3.3V+3.3V</td> <td>P : 1.5V+2.5V</td> </tr> <tr> <td>B : 2.8V+3.3V</td> <td>Q : 1.2V+2.5V</td> </tr> <tr> <td>C : 2.5V+3.3V</td> <td>R : 1.8V+1.8V</td> </tr> <tr> <td>D : 1.8V+3.3V</td> <td>S : 1.5V+1.8V</td> </tr> <tr> <td>E : 1.5V+3.3V</td> <td>T : 1.2V+1.8V</td> </tr> <tr> <td>F : 1.2V+3.3V</td> <td>U : 1.5V+1.5V</td> </tr> <tr> <td>G : 2.8V+2.8V</td> <td>V : 1.2V+1.5V</td> </tr> <tr> <td>H : 2.5V+2.8V</td> <td>W : 2.85V+2.85V</td> </tr> <tr> <td>J : 1.8V+2.8V</td> <td>1 : 3.0V+3.3V</td> </tr> <tr> <td>K : 1.5V+2.8V</td> <td>2 : 1.8V+3.0V</td> </tr> <tr> <td>L : 1.2V+2.8V</td> <td>3 : 3.0V+3.0V</td> </tr> <tr> <td>M : 2.5V+2.5V</td> <td>4 : 1.3V+2.8V</td> </tr> <tr> <td>N : 1.8V+2.5V</td> <td></td> </tr> </table> <p>Lead Free Code :</p> <p>P : Commercial Standard, Lead (Pb) Free and Phosphorous (P) Free Package</p> <p>G : Green (Halogen Free with Commercial Standard)</p> <p>Package Code :</p> <table style="width: 100%; border: none;"> <tr> <td>V : SOT23-6</td> <td>U : UFN-6</td> </tr> </table>	A : 3.3V+3.3V	P : 1.5V+2.5V	B : 2.8V+3.3V	Q : 1.2V+2.5V	C : 2.5V+3.3V	R : 1.8V+1.8V	D : 1.8V+3.3V	S : 1.5V+1.8V	E : 1.5V+3.3V	T : 1.2V+1.8V	F : 1.2V+3.3V	U : 1.5V+1.5V	G : 2.8V+2.8V	V : 1.2V+1.5V	H : 2.5V+2.8V	W : 2.85V+2.85V	J : 1.8V+2.8V	1 : 3.0V+3.3V	K : 1.5V+2.8V	2 : 1.8V+3.0V	L : 1.2V+2.8V	3 : 3.0V+3.0V	M : 2.5V+2.5V	4 : 1.3V+2.8V	N : 1.8V+2.5V		V : SOT23-6	U : UFN-6
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Absolute Maximum Ratings

Parameter		Symbol	Ratings	Units
Input Voltage		V_{IN}	7.0	V
Output Current		$I_{OUT1} + I_{OUT2}$	700	mA
Output Voltage		V_{OUT}	$V_{SS}-0.3 \sim V_{IN}+0.3$	V
EN Pin Voltage		V_{EN}	$V_{SS}-0.3 \sim V_{IN}+0.3$	V
Junction Temperature		T_J	-40 ~ +150	°C
Thermal Resistance	SOT-23-6	θ_{JA}	250	°C/W
	UFN-6			
Power Dissipation	SOT-23-6	P_D	400	mW
	UFN-6		500	
Operating Ambient Temperature		T_{OPR}	-40 ~ +85	°C
Storage Temperature		T_{STG}	-55 ~ +125	°C
Lead Temperature (soldering, 10sec)			+260	°C

Note :

* The power dissipation of UFN-6 would be 500 mW normally with the 0.5X0.5 square inches cooper area connected to the bottom pad. However, it could be up to 1000mW with larger cooper area.

Electrical Characteristics

($T_A=25^{\circ}\text{C}$, for each channel)

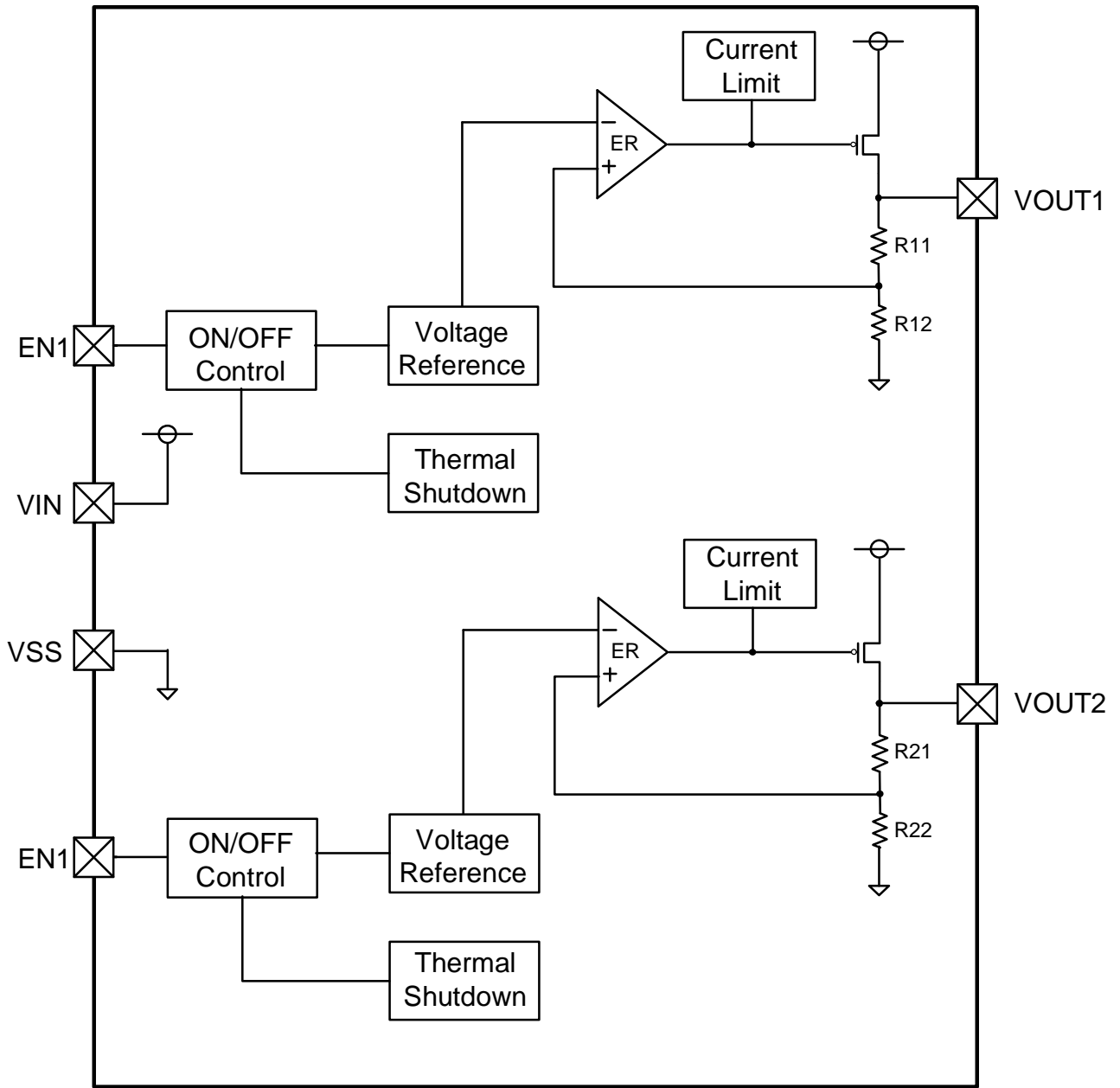
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage		2.7		7.0	V
V_{OUT}	Output Voltage	$V_{IN}=V_{OUT}+1.0\text{V}$, $I_{OUT}=30\text{mA}$, $V_{OUT}>2.0\text{V}$	-2%	V_{OUT}	+2%	V
		$V_{IN}=V_{OUT}+1.0\text{V}$, $I_{OUT}=30\text{mA}$, $V_{OUT}\leq 2.0\text{V}$	-0.04	V_{OUT}	+0.04	V
I_{MAX}	Output Current	$V_{OUT}+1.0\text{V}\leq V_{IN}\leq 6\text{V}$ (see note *1)		250		mA
V_{DROP}	Dropout Voltage	$I_{OUT}=100\text{mA}$		150	250	mV
I_{SS}	Supply Current	$V_{IN}=V_{EN}=V_{OUT}+1.0\text{V}$, $I_{OUT}=0\text{mA}$		8	15	μA
I_{STB}	Standby Current	$V_{IN}=V_{OUT}+1.0\text{V}$, $V_{EN}=V_{SS}$		0.01	1	μA
ΔV_{LINE}	Line Regulation	$V_{OUT}+1.0\text{V}\leq V_{IN}\leq 6.0\text{V}$, $I_{OUT}=0\text{mA}$		0.2	0.3	%/V
ΔV_{LOAD}	Load Regulation	$V_{IN}=V_{OUT}+1.0\text{V}$, $1\text{mA}\leq I_{OUT}\leq 100\text{mA}$		0.02	0.03	%/mA
T_C	Temperature Characteristics	$I_{OUT}=30\text{mA}$, $-25^{\circ}\text{C}\leq T_{OPR}\leq +85^{\circ}\text{C}$		± 100		ppm/ $^{\circ}\text{C}$
I_{LIM}	Current Limiter	$V_{IN}=V_{OUT}+1.0\text{V}$, $V_{IN}=V_{EN}$		350		mA
I_{SHORT}	Short-Circuit Current	$V_{IN}=V_{OUT}+1.0\text{V}$, $V_{IN}=V_{EN}$		150		mA
PSRR	Ripple Rejection Rate	$I_{OUT}=30\text{mA}$, $F=1\text{KHz}$		70		dB
V_{IH}	EN Pin Input Voltage "H"	(see note *2)	$0.6V_{IN}$			V
V_{IL}	EN Pin Input Voltage "L"	(see note *2)			$0.3V_{IN}$	V
T_{TST}	Thermal Shutdown Temperature			150		$^{\circ}\text{C}$
T_{TSH}	Thermal Shutdown Hysteresis			40		$^{\circ}\text{C}$

Note :

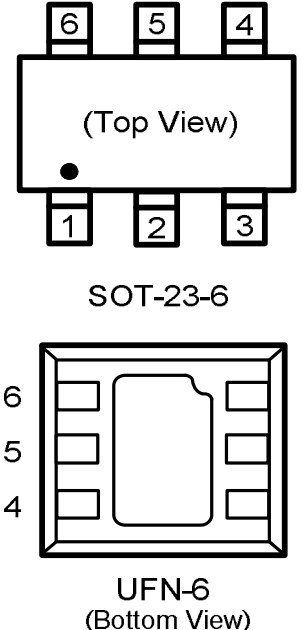
*1) Measured using a double sided board with 1" x 2" square inches of copper area connected to the GND pins for "heat spreading".

*2) EN pin input voltage must be always less than or equal to input voltage.

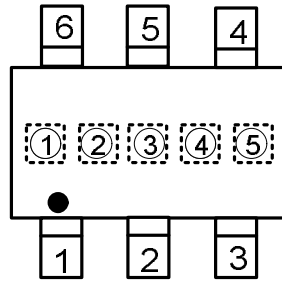
Function Block Diagram



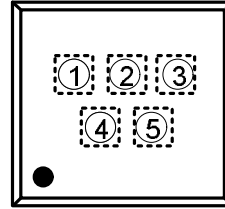
Pin Assignment & Pin Description

 <p>(Top View) SOT-23-6</p> <p>(Bottom View) UFN-6</p>	Pin Number		Pin Name	Function
	SOT-26	UFN-6		
	1	3	EN1	V _{OUT1} Enable Control Pin
	2	2	V _{IN}	Power Input
	3	1	EN2	V _{OUT2} Enable Control Pin
	4	6	V _{OUT2}	Voltage Output 2
	5	4	GND	Ground
	6	5	V _{OUT1}	Voltage Output 1

Package Marking Information



SOT-23-6
(Top View)



UFN-6
(Top View)

①、② Represents Products Series

Mark	Products Series
01	AP6401X-PV/U

③ Represents Type of Output Vpltage

Mark	Products Series	Voltage	Mark	Products Series	Voltage
A	AP6401A-PV/U	3.3V+3.3V	N	AP6401N-PV/U	1.8V+2.5V
B	AP6401B-PV/U	2.8V+3.3V	P	AP6401P-PV/U	1.5V+2.5V
C	AP6401C-PV/U	2.5V+3.3V	Q	AP6401Q-PV/U	1.2V+2.5V
D	AP6401D-PV/U	1.8V+3.3V	R	AP6401R-PV/U	1.8V+1.8V
E	AP6401E-PV/U	1.5V+3.3V	S	AP6401S-PV/U	1.5V+1.8V
F	AP6401F-PV/U	1.2V+3.3V	T	AP6401T-PV/U	1.2V+1.8V
G	AP6401G-PV/U	2.8V+2.8V	U	AP6401U-PV/U	1.5V+1.5V
H	AP6401H-PV/U	2.5V+2.8V	V	AP6401V-PV/U	1.2V+1.5V
J	AP6401J-PV/U	1.8V+2.8V	W	AP6401W-PV/U	2.85V+2.85V
K	AP6401K-PV/U	1.5V+2.8V	1	AP64011-PV/U	3.0V+3.3V
L	AP6401L-PV/U	1.2V+2.8V	2	AP64012-PV/U	1.8V+3.0V
M	AP6401M-PV/U	2.5V+2.5V	3	AP64013-PV/U	3.0V+3.0V

④、⑤ Represents Production Date Code

Note :

* There are two under-lines on 4th & 5th digit for Green package.

* There are no under-lines on 4th & 5th digit for Pb-Free package.

Detail Description

The AP6401 series are highly accurate, dual, low noise, CMOS LDO voltage regulators with enable function. The output voltage for each regulator is set independently by metal trimming. It's also available to offer other types of V_{OUT} between +1.2V~+3.9V except the options shown on ordering information. As illustrated in function block diagram, it consists of a reference, error amplifier, a P-channel pass transistor, an ON/OFF control logic and an internal feedback voltage divider.

The band gap reference is connected to the error amplifier, which compares the reference with the feedback voltage and amplifies the voltage difference. If the feedback voltage is lower than the reference voltage, the pass-transistor gate is pulled lower, which allows more current to pass to the V_{OUT} pin and increases the output voltage. If the feedback voltage is too high, the pass transistor gate is pulled up to decrease the output voltage.

The output voltage is feed back through an internal resistive divider connected to V_{OUT} pin. Additional blocks include an output current limiter, thermal sensor, and shutdown logic.

Internal P-channel Pass Transistor

Each channel of AP6401 features a P-channel MOSFET pass transistor. Unlike similar designs using PNP pass transistors, P-channel MOSFETs require no base drive, which reduces quiescent current. PNP-based regulators also waste considerable current in dropout when the pass transistor saturates, and use high base-drive currents under large loads. The AP6401 does not suffer from these problems and consumes only 8 μ A (Typ.) per channel of current consumption under heavy loads as well as in dropout conditions.

Enable Function

EN1 and EN2 pin start and stop the corresponding outputs independently. When the EN pin is switched to the power off level, the operation of all internal circuit stops, the build-in P-channel MOSFET output transistor between pins V_{IN} and V_{OUT} is switched off, allowing current consumption to be drastically reduced.

Current Limit

Each channel of AP6401 includes a fold back current limiter. It monitors and controls the pass transistor's gate voltage, estimates the output current, and limits the output current within 350mA.

Thermal Overload Protection

Thermal overload protection limits total power dissipation of AP6401. When the junction temperature exceeds $T_J = +150^{\circ}\text{C}$, a thermal sensor turns off the pass transistor, allowing the IC to cool down. The thermal sensor turns the pass transistor on again after the junction temperature cools down by 40°C , resulting in a pulsed output during continuous thermal overload conditions.

Thermal overload protection is designed to protect the AP6401 in the event of fault conditions. For continuous operation, the absolute maximum operating junction temperature rating of $T_J = +125^{\circ}\text{C}$ should not be exceeded.

Operating Region and Power Dissipation

Maximum power dissipation of the AP6401 depends on the thermal resistance of the case and printed circuit board, the temperature difference between the die junction and ambient air, and the rate of airflow. The power dissipation across the devices is $P = I_{OUT} \times (V_{IN} - V_{OUT})$. The resulting maximum power dissipation is:

$$P_{MAX} = \frac{(T_J - T_A)}{\theta_{JC} + \theta_{CA}} = \frac{(T_J - T_A)}{\theta_{JA}}$$

Where $(T_J - T_A)$ is the temperature difference between the AP6401 die junction and the surrounding air, θ_{JC} is the thermal resistance of the package chosen, and θ_{CA} is the thermal resistance through the printed circuit board, copper traces and other materials to the surrounding air. For better heat-sinking, the copper area should be equally shared between the V_{IN} , V_{OUT} , and GND pins.

The thermal resistance θ_{JA} of SOT-23-6 package of AP6401 is $250^{\circ}\text{C}/\text{W}$. Based on a maximum operating junction temperature 125°C with an ambient of 25°C , the maximum power dissipation will be:

$$P_{MAX} = \frac{(T_J - T_A)}{q_{JC} + q_{CA}} = \frac{(125 - 25)}{250} = 0.40W$$

Thermal characteristics were measured using a double sided board with 1" x 2" square inches of copper area connected to the GND pin for "heat spreading".

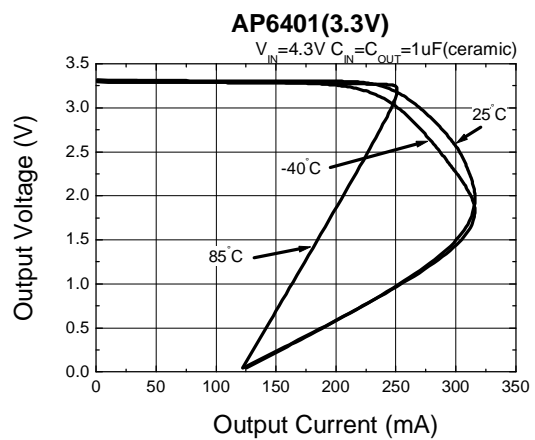
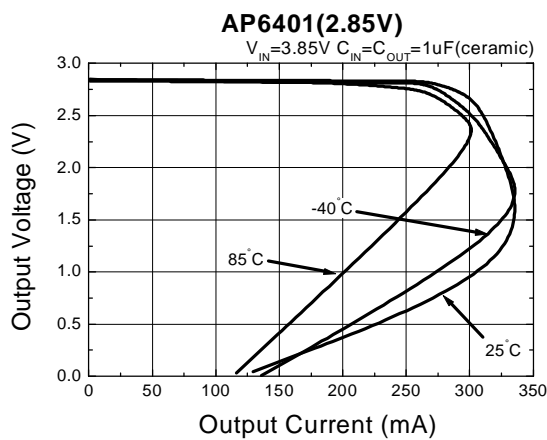
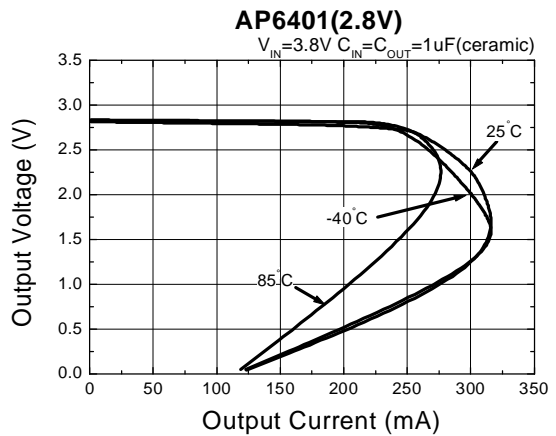
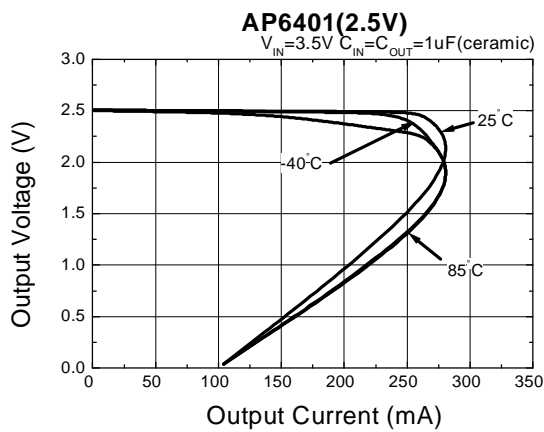
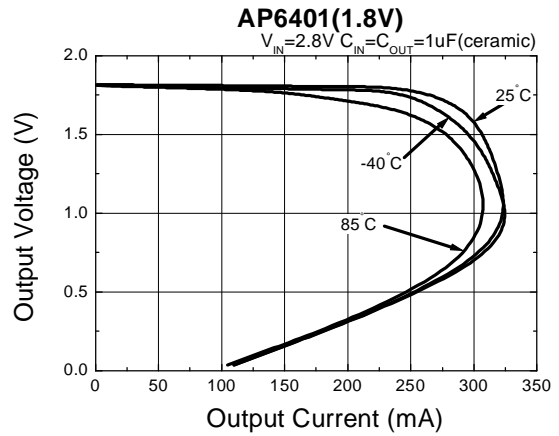
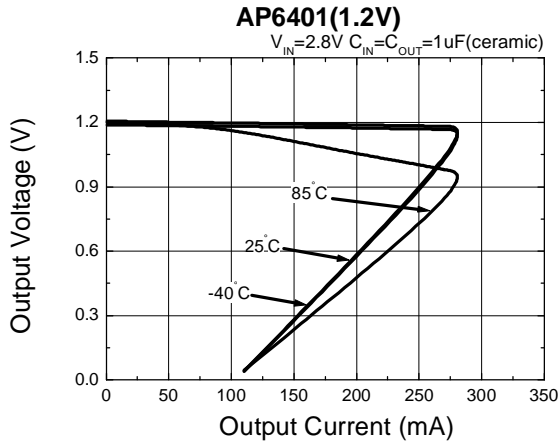
Dropout Voltage

A regulator's minimum input-output voltage differential, or dropout voltage, determines the lowest usable supply voltage. In battery-powered systems, this will determine the useful end-of-life battery voltage. The AP6401 use a P- channel MOSFET pass transistor, its dropout voltage is a function of drain-to-source on-resistance $R_{DS(ON)}$ multiplied by the load current.

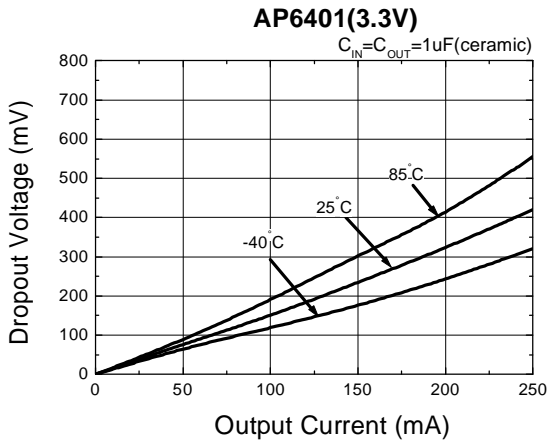
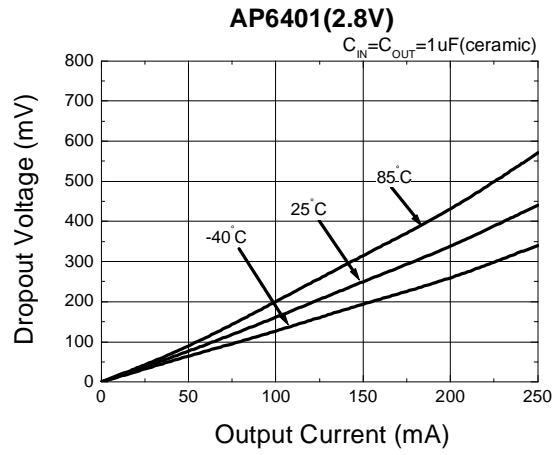
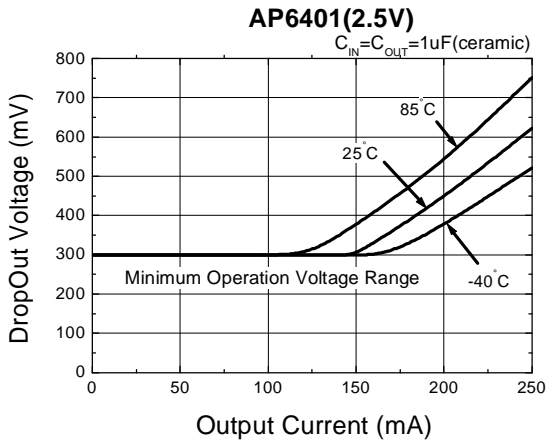
$$V_{DROPOUT} = V_{IN} - V_{OUT} = R_{DS(ON)} \times I_{OUT}$$

Typical Operating Characteristics

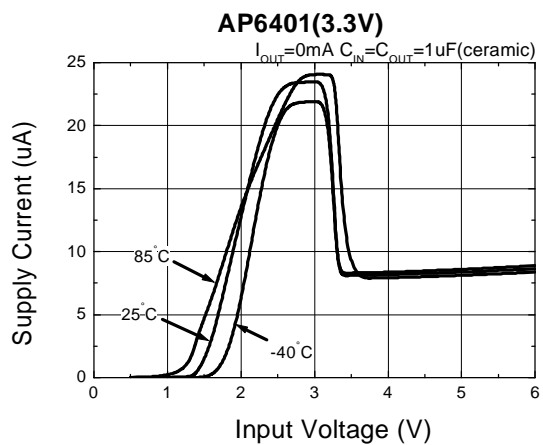
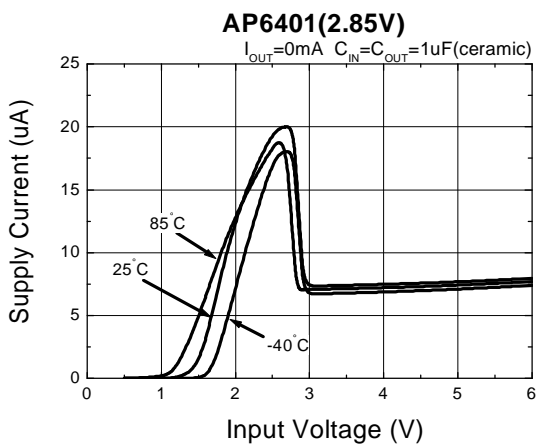
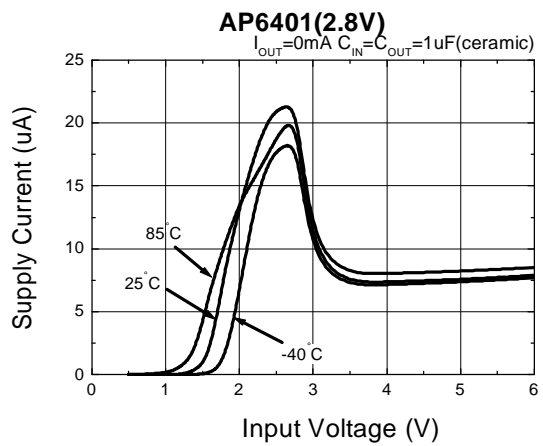
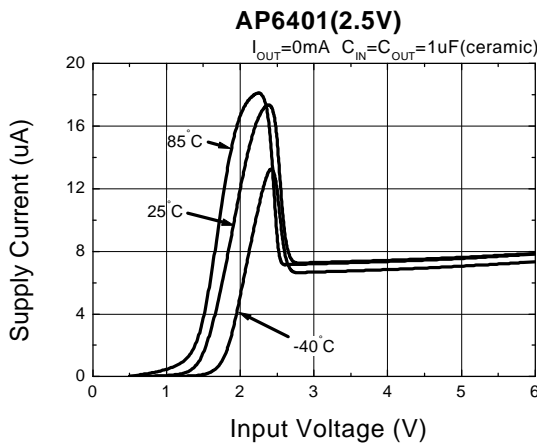
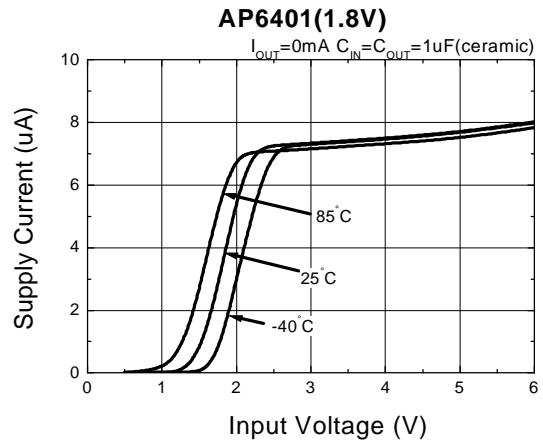
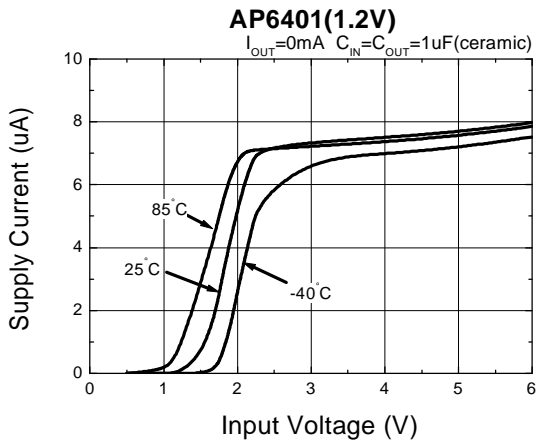
(1) Output Voltage vs. Output Current



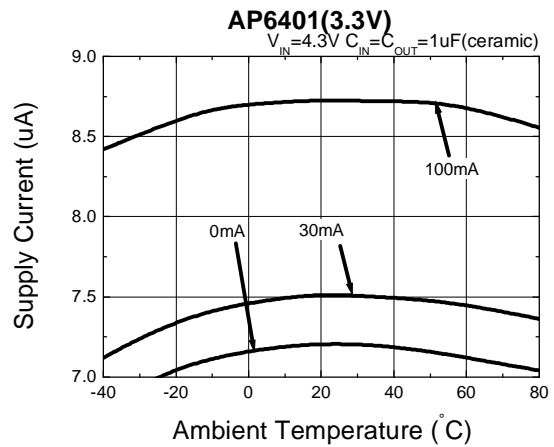
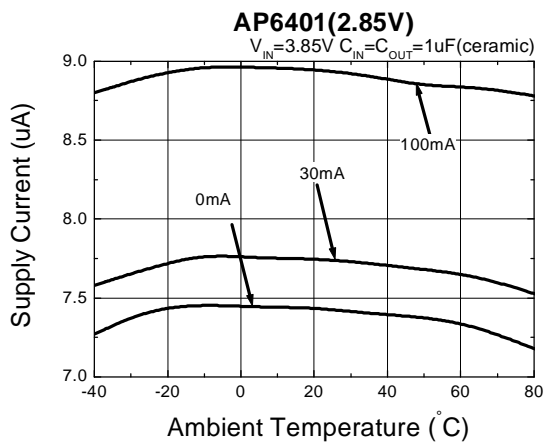
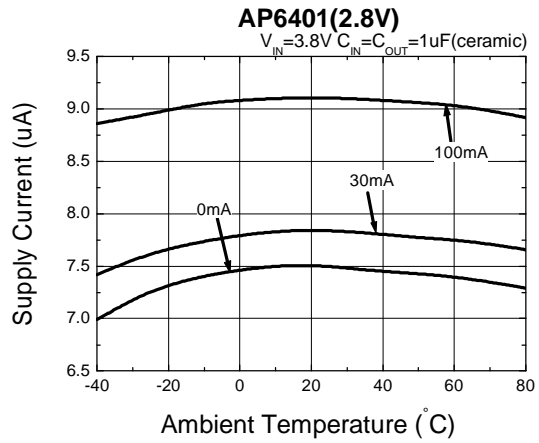
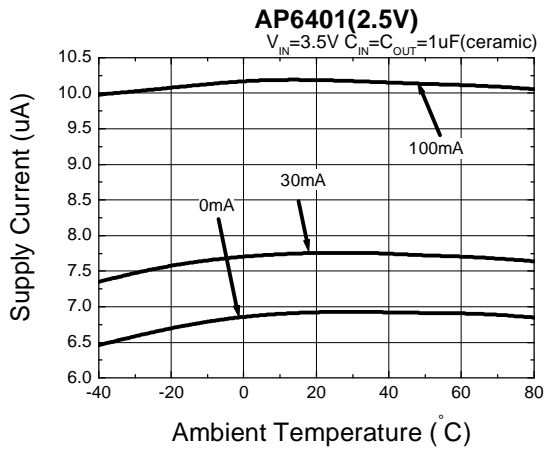
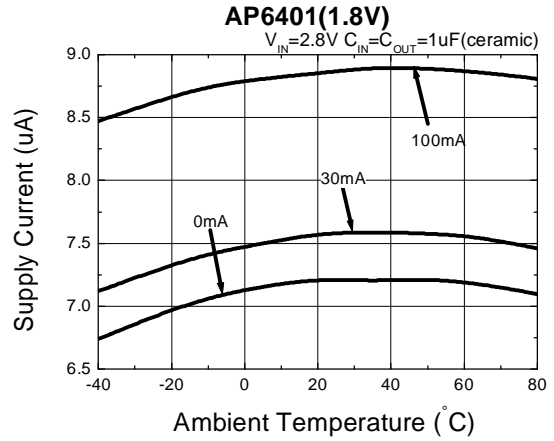
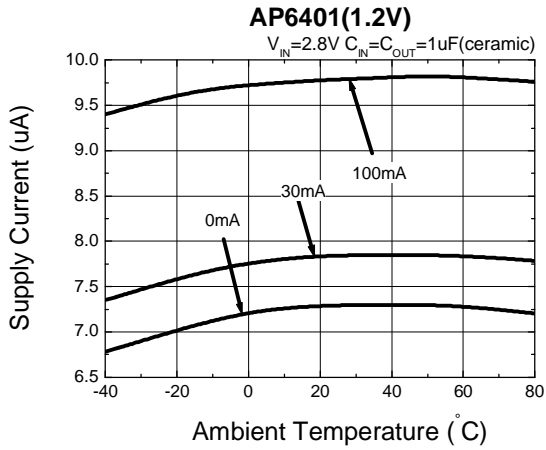
(2) Dropout Voltage vs. Output Current



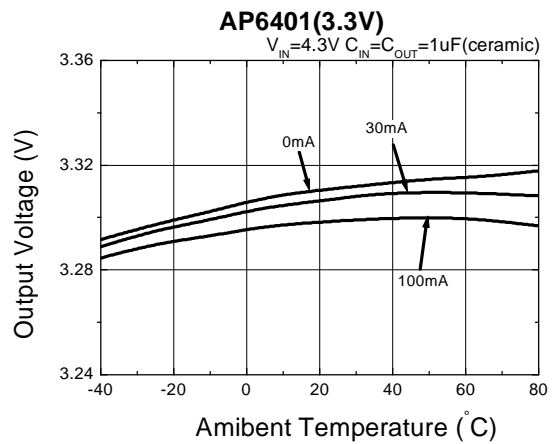
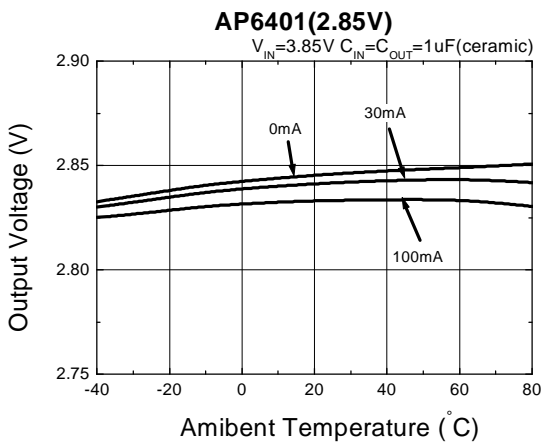
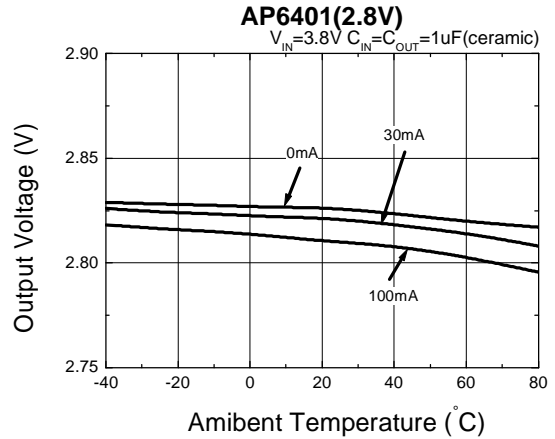
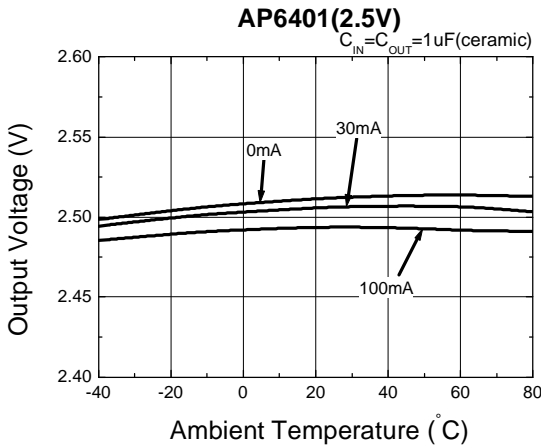
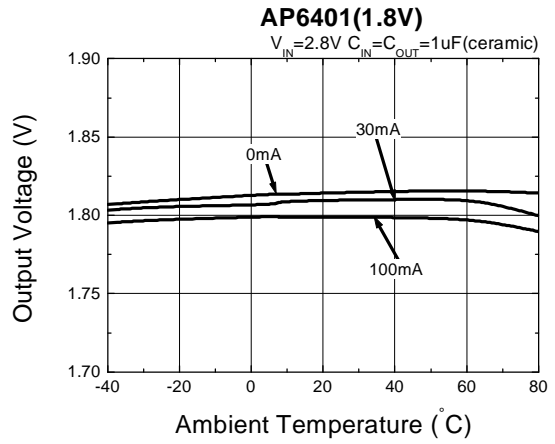
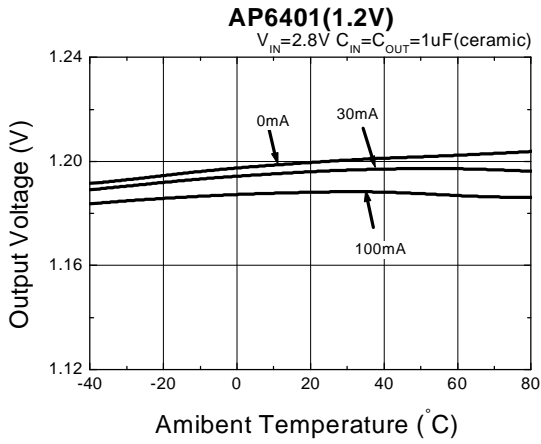
(3) Supply Current vs. Input Voltage



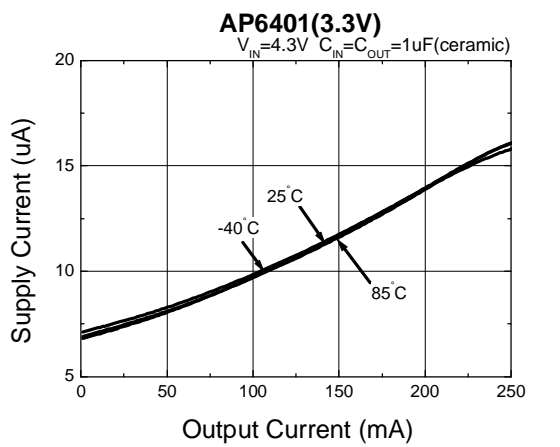
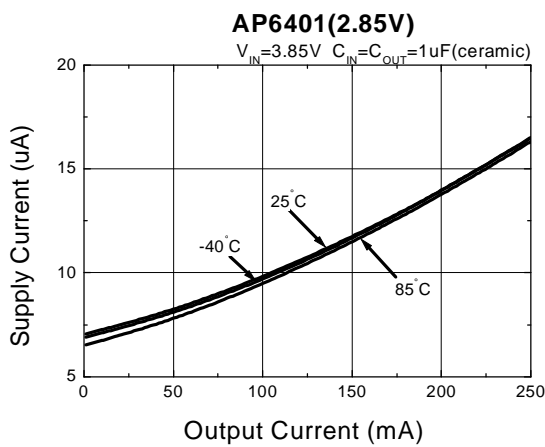
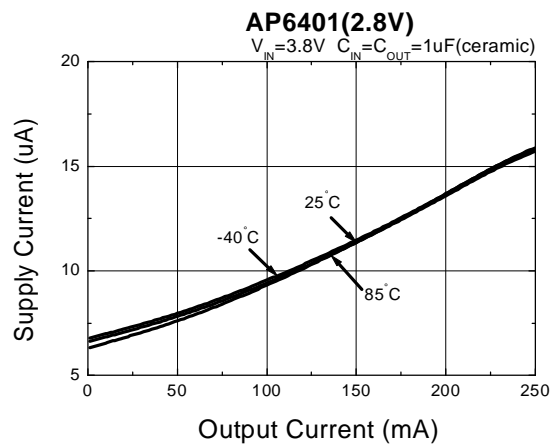
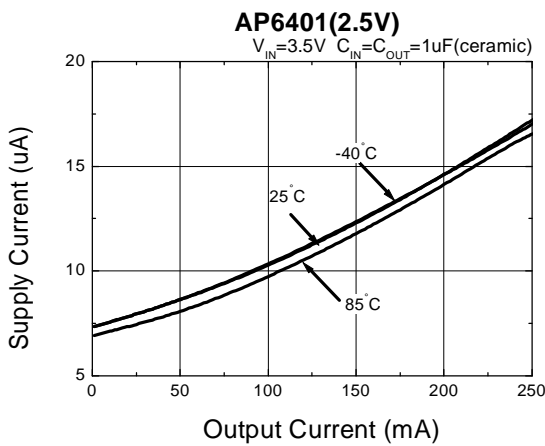
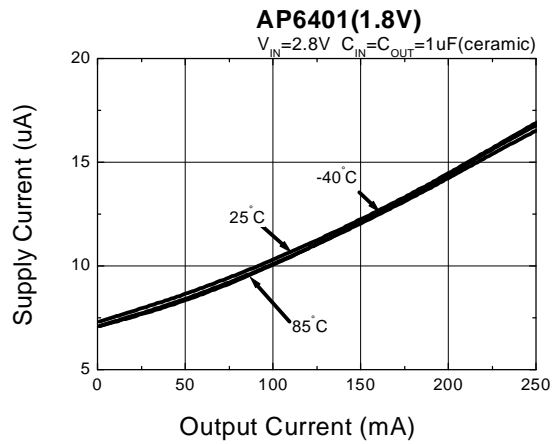
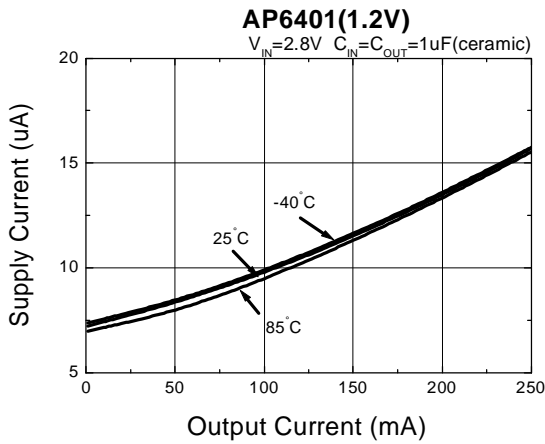
(4) Supply Current vs. Ambient Temperature



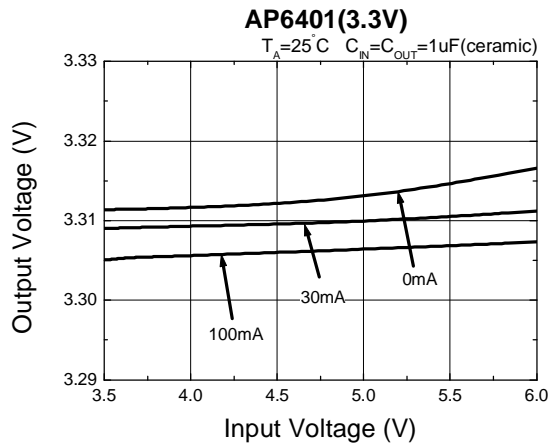
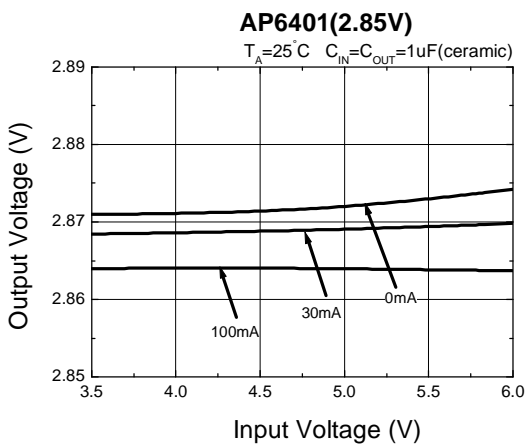
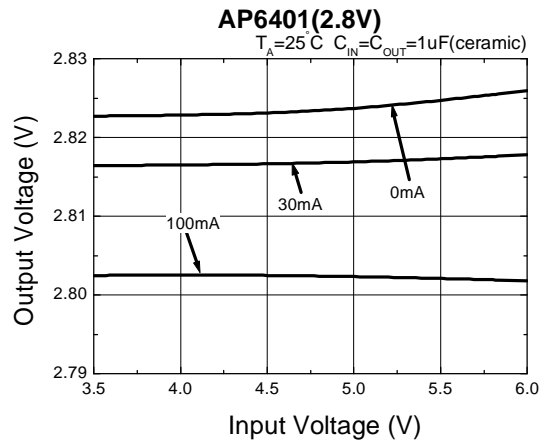
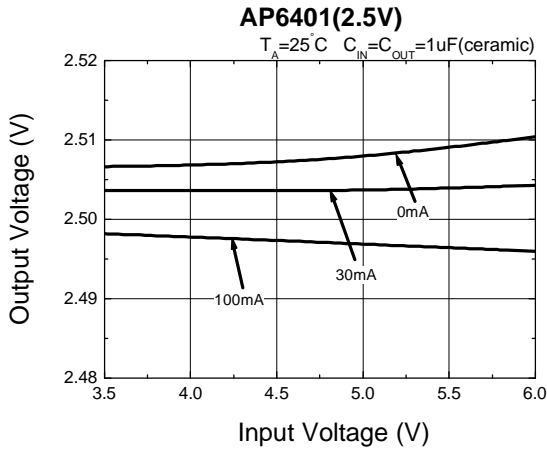
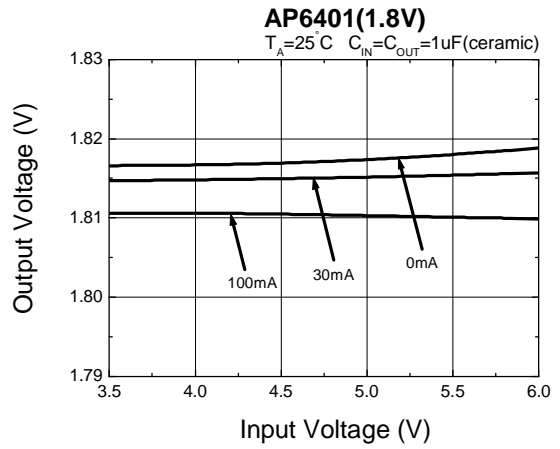
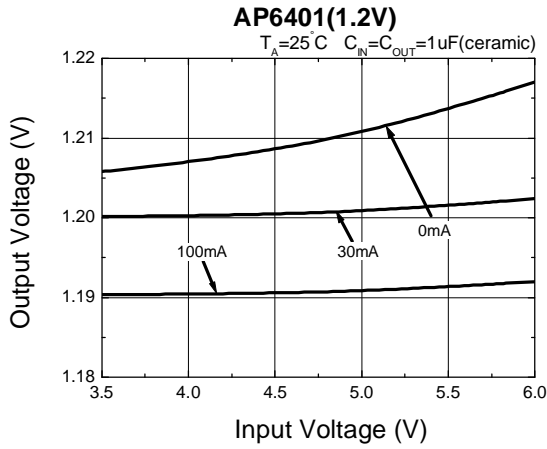
(5) Output Voltage vs. Ambient Temperature



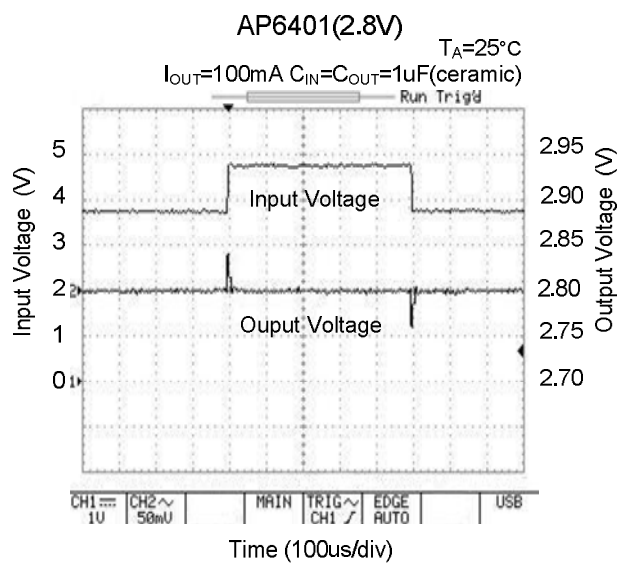
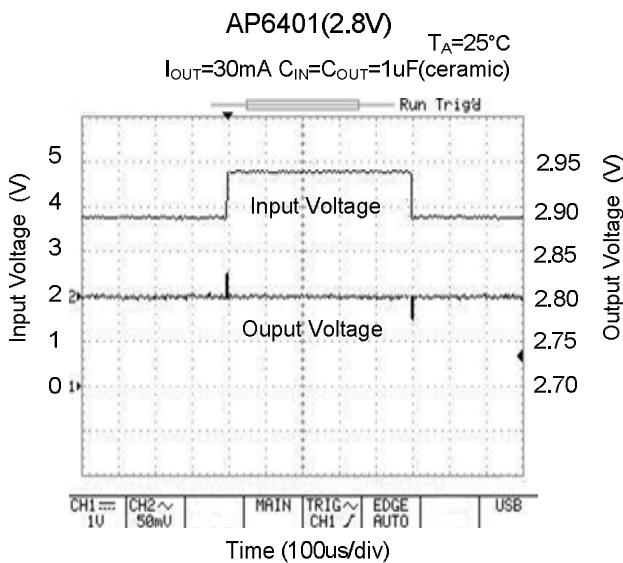
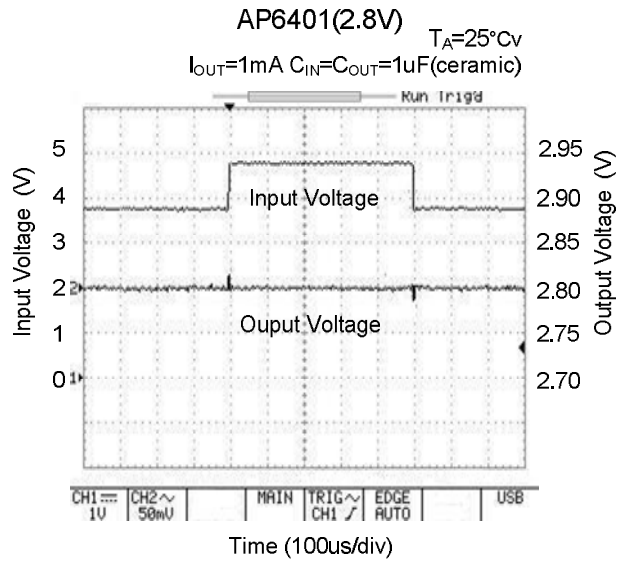
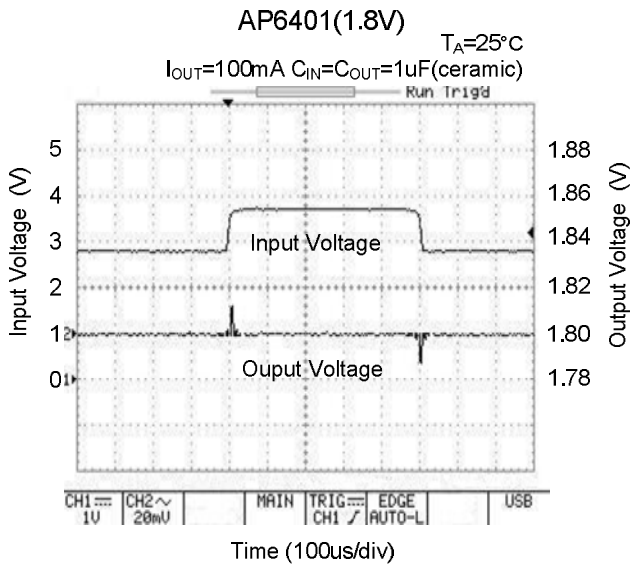
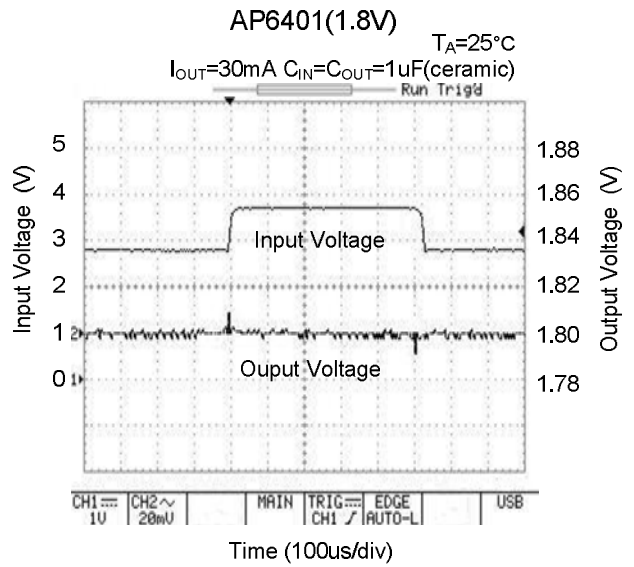
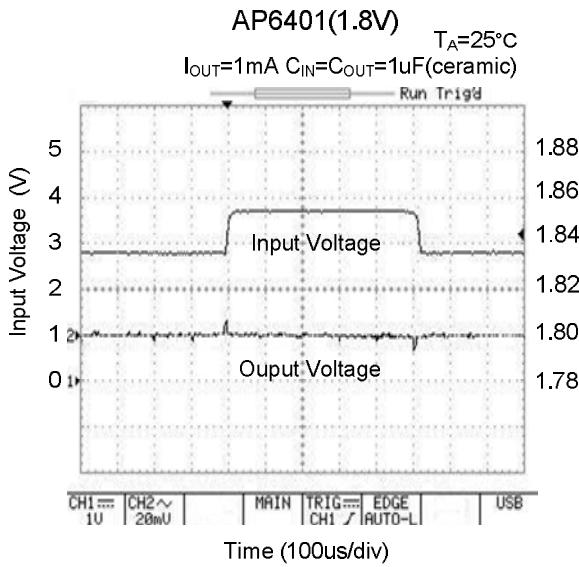
(6) Supply Current vs. Output Current



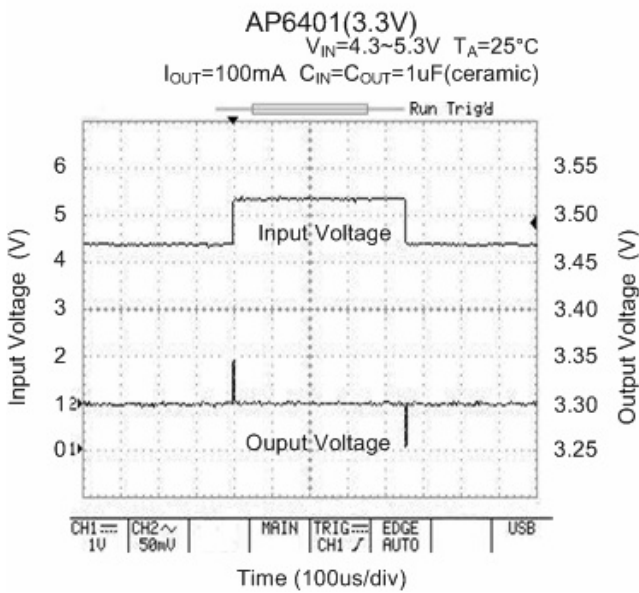
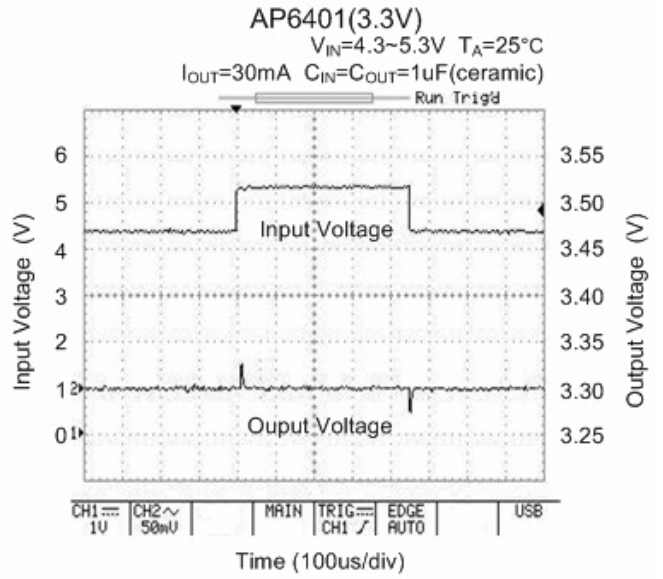
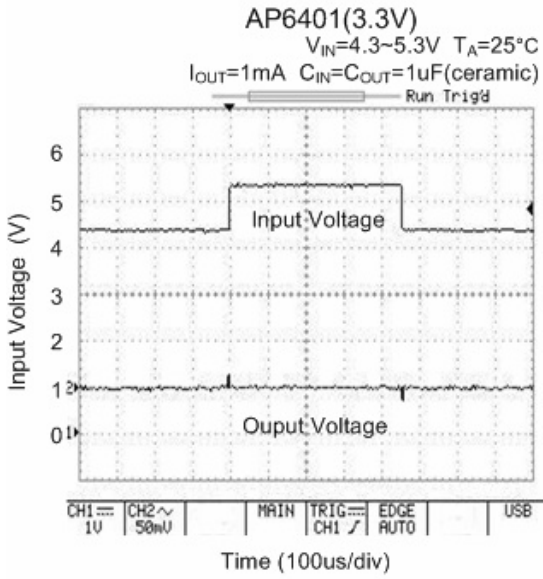
(7) Output Voltage vs. Input Voltage



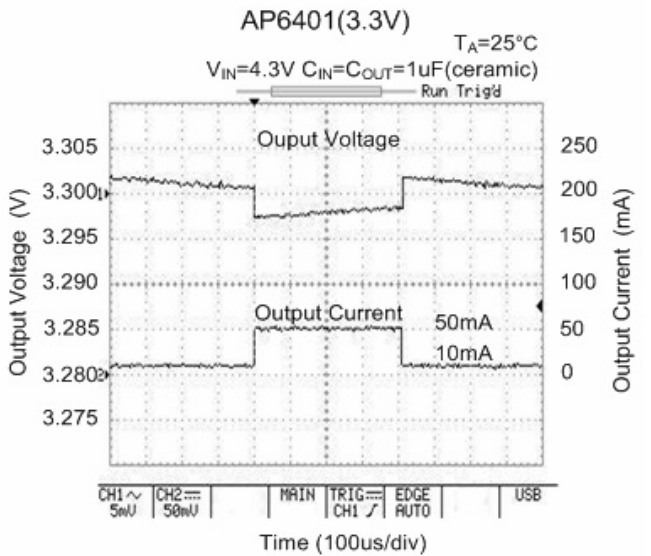
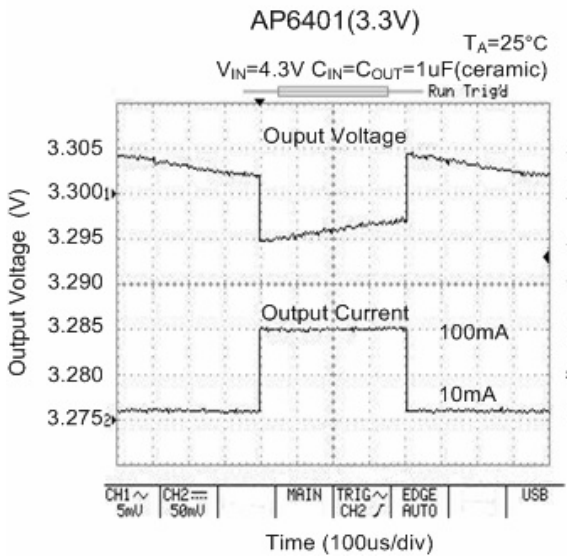
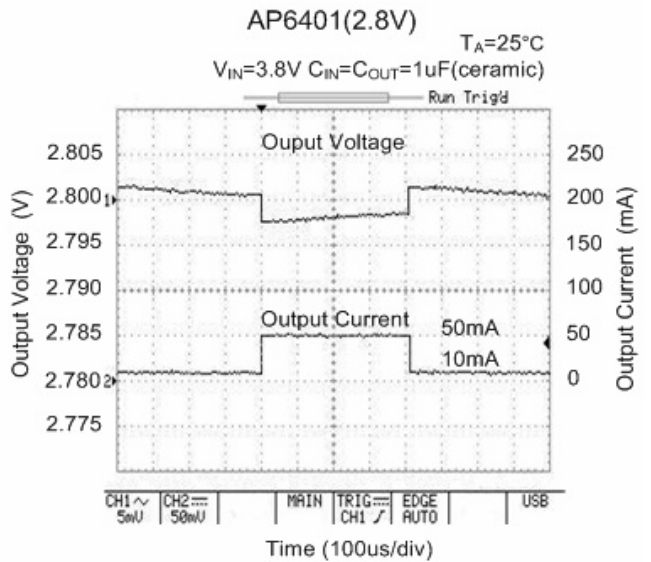
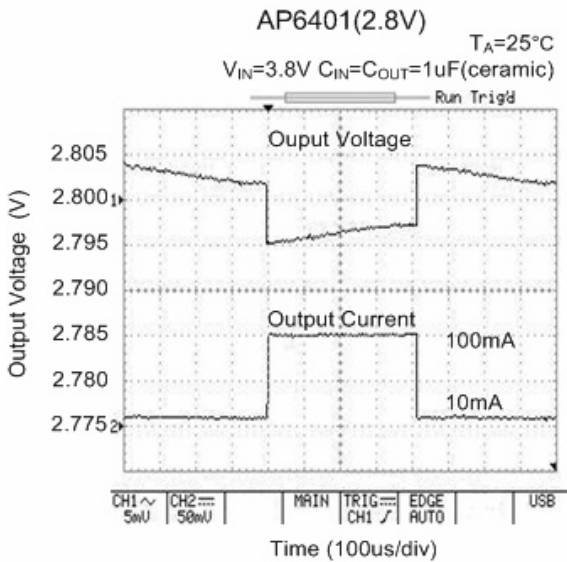
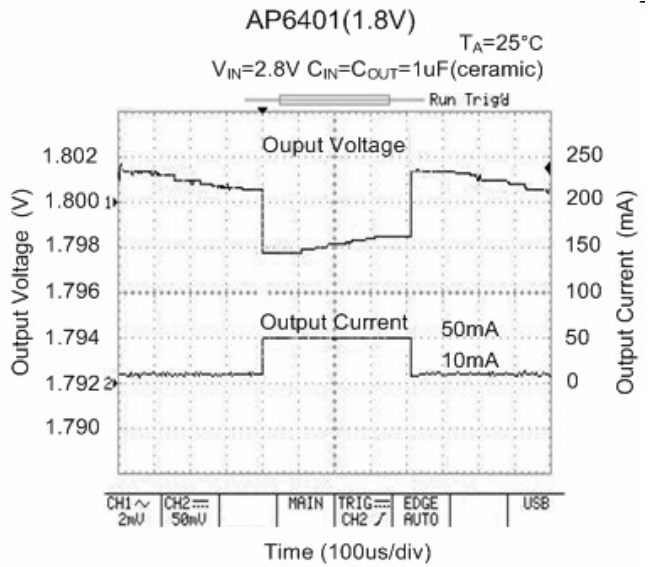
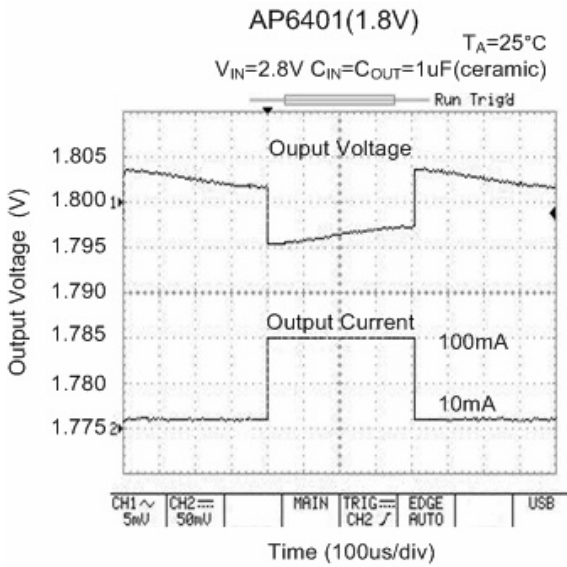
(8) Input Transient Response



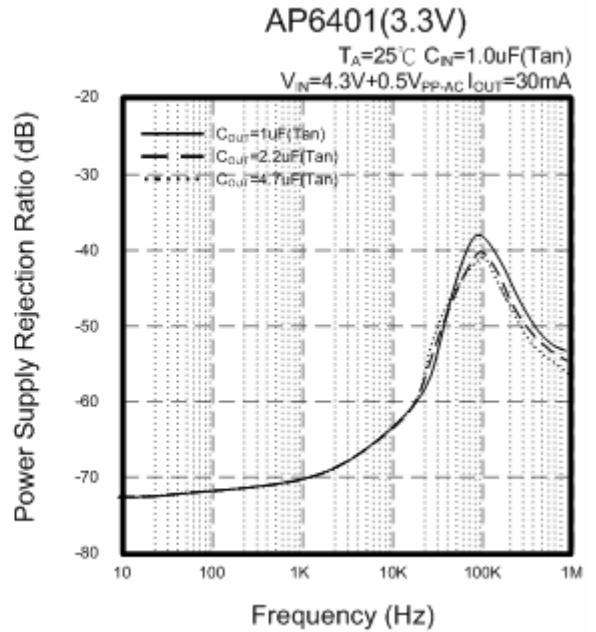
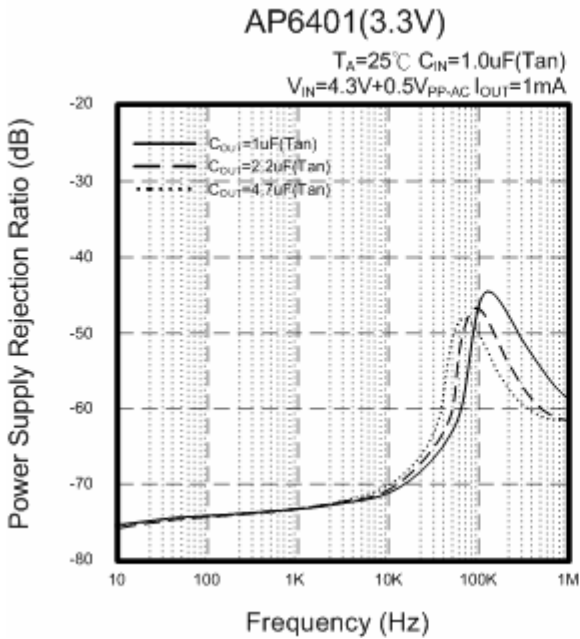
(8) Input Transient Response (Continued)



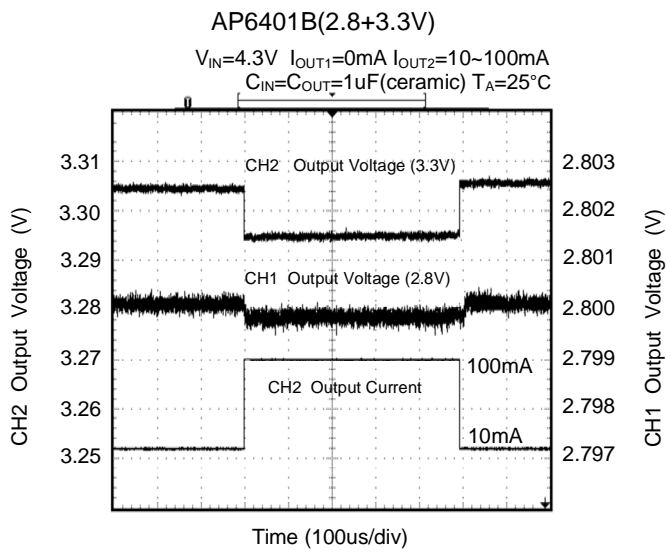
(9) Load Transient Response



(10) Power Supply Rejection Ratio



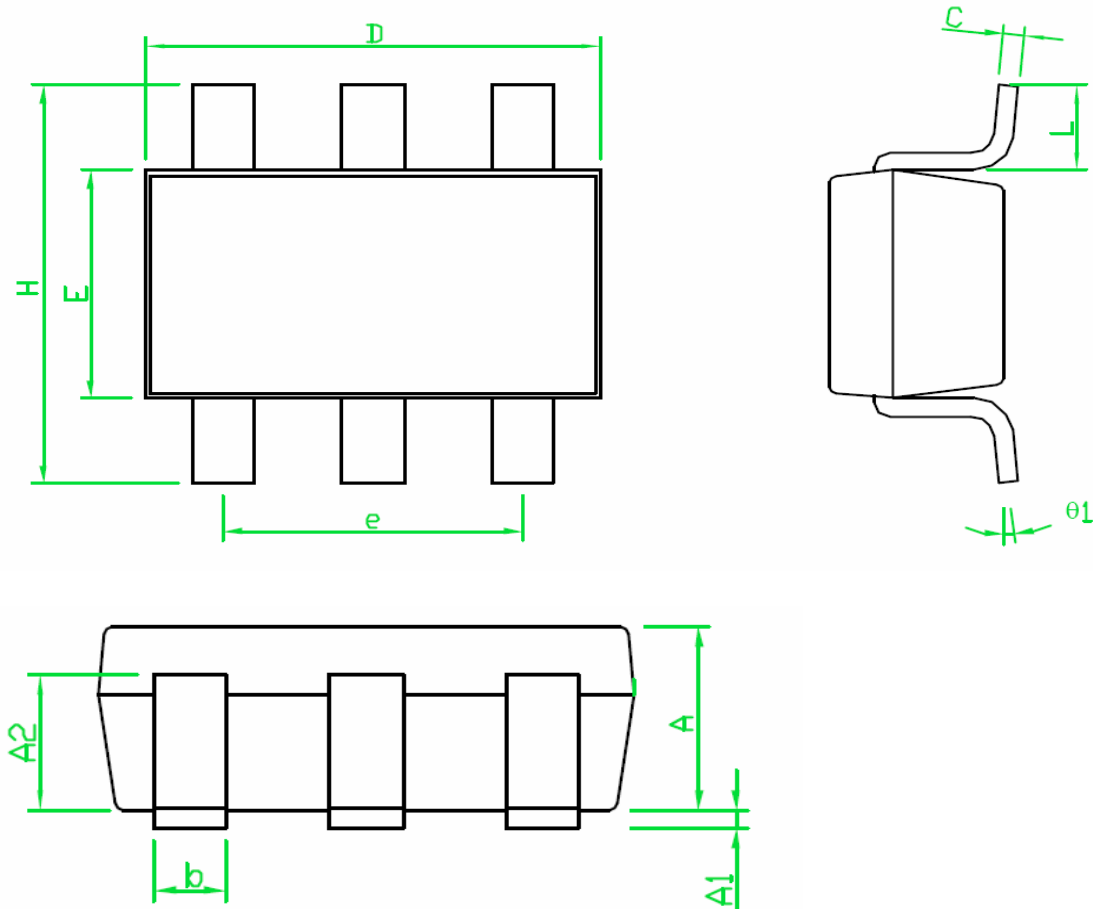
(11) Cross Talk



AP6401 Series

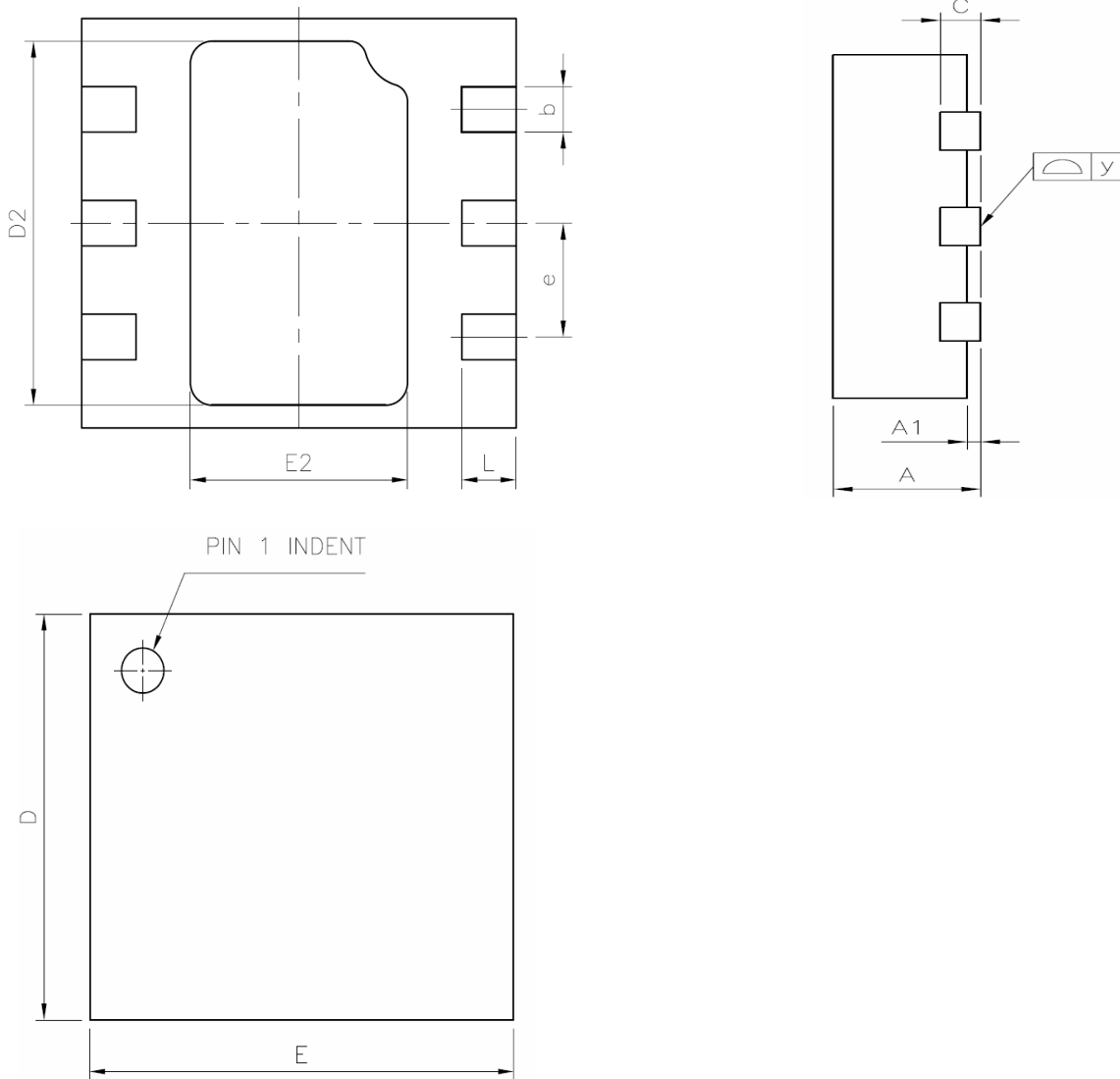
Package Outline

A) SOT-26



SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	1.00	1.10	1.30
A1	0.00	---	0.10
A2	0.70	0.80	0.90
b	0.35	0.40	0.50
C	0.10	0.15	0.25
D	2.70	2.90	3.10
E	1.40	1.60	1.80
e	---	1.90(TYP)	---
H	2.60	2.80	3.00
L	0.37	---	---
θ1	1°	5°	9°

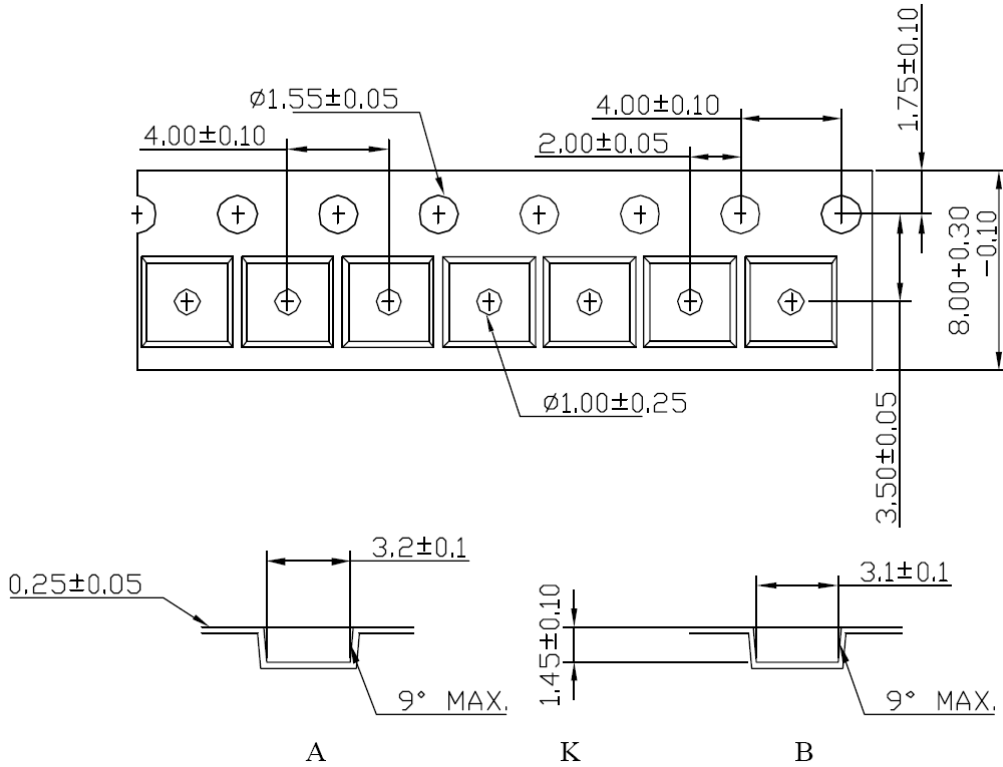
B) UFN-6



Dimension	mm		
	Min.	Nom.	Max.
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
C	---	0.15 REF	---
D	1.60	1.80	1.90
D2	1.55	1.60	1.65
E	1.90	2.00	2.10
E2	0.95	1.00	1.05
e	---	0.50	---
L	0.20	0.25	0.30
y	0.00	---	0.075

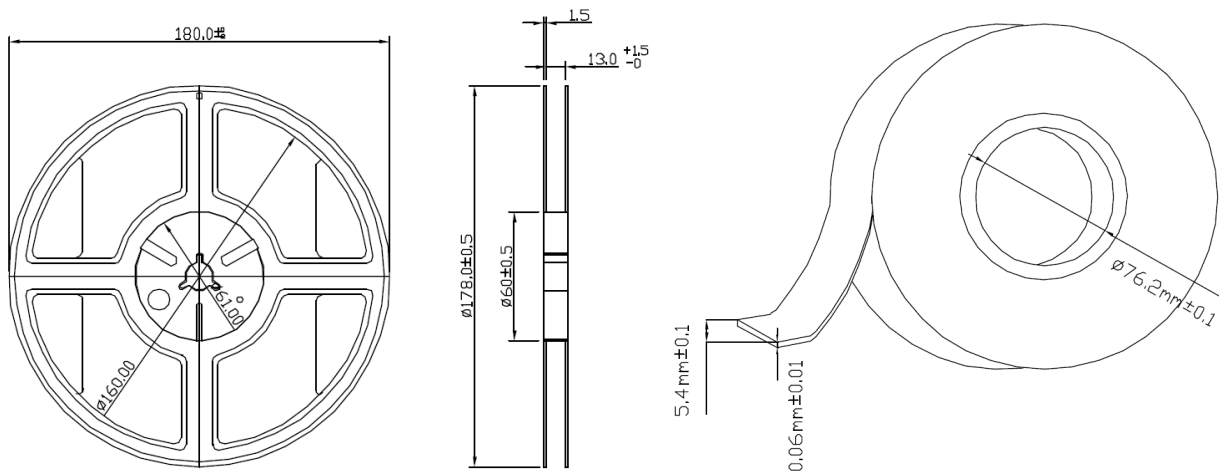
Carrier Tape & Reel Dimensions

A) SOT-26

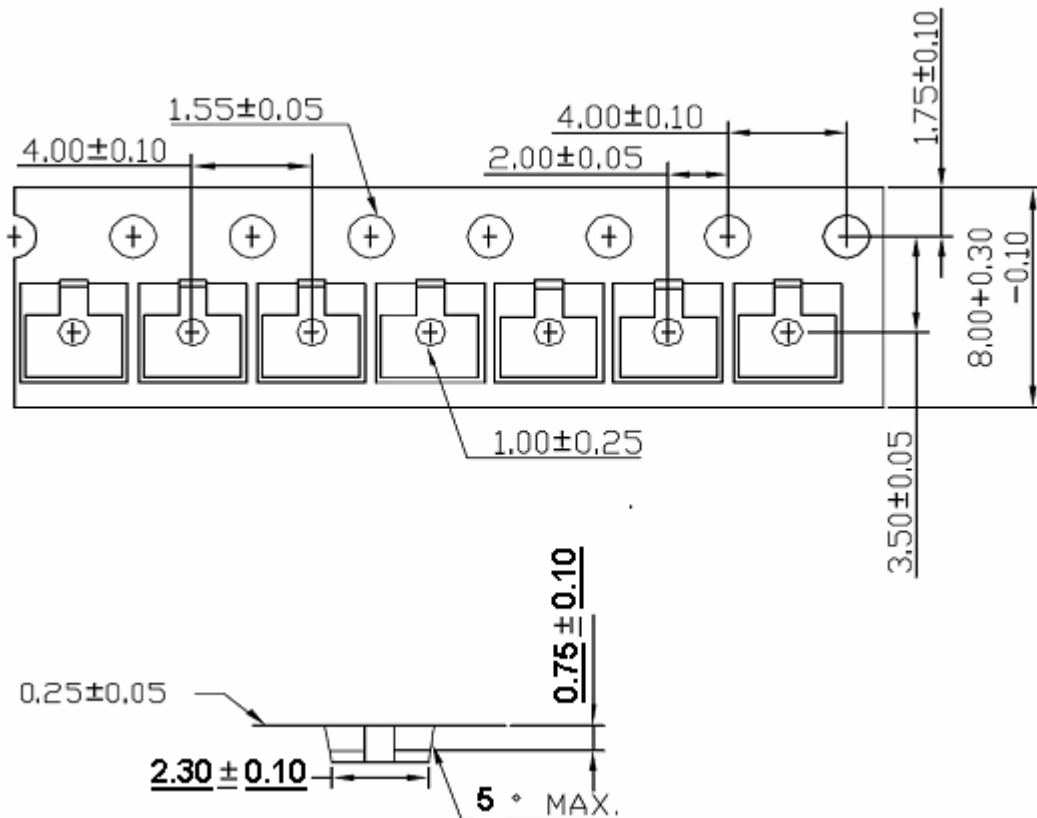


Notes:

1. Material: black advantek polystyrene.
2. Dim in mm.
3. 10 sprocket hole pitch cumulative tolerance ± 0.2 .
4. Camber not to exceed 1 mm in 100mm.
5. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
6. Surface resistance less than or equal to $1.0 \times 10^3 \sim 10$ ohms/sq.
7. A and B measured on a plane 0.3mm above the bottom of the pocket.
8. K measured from a plane on the inside bottom of the pocket to the to surface of the carrier.

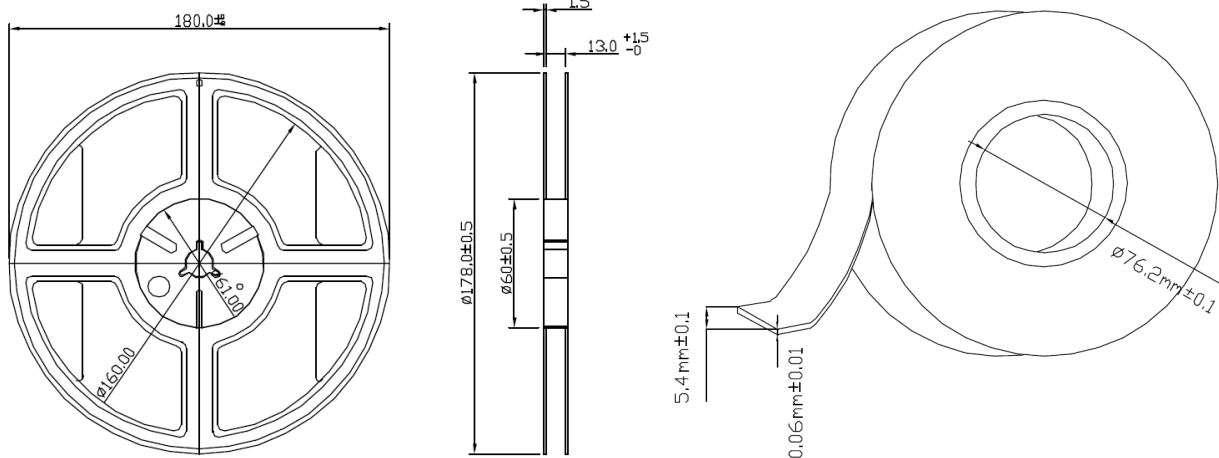


B) UFN-6

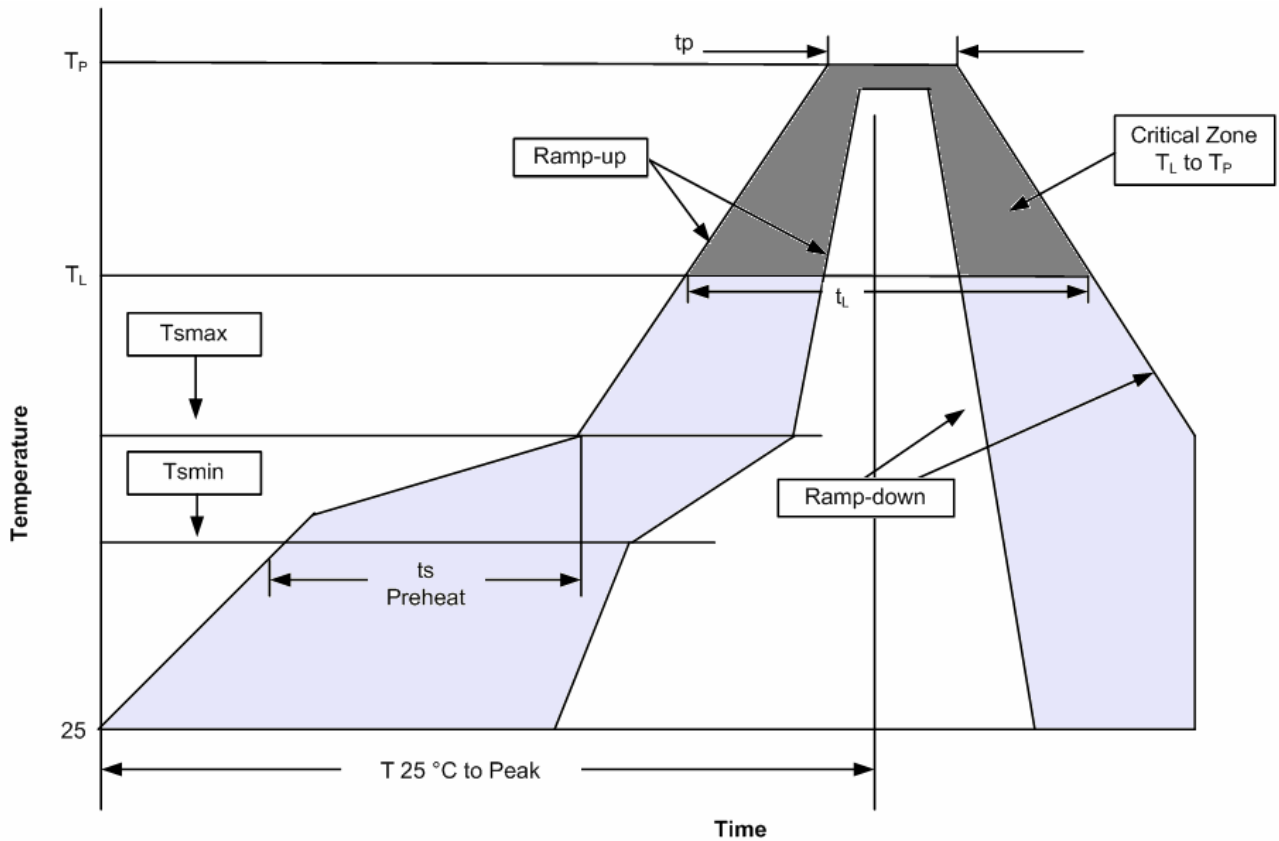


Notes:

1. Material: black advantek polystyrene.
2. Cover tape width : 5.40 ± 0.10 .
3. Cover tape color : transparent.
4. Surface resistance less than or equal to $1.0 \times 10^4 \sim 11$ ohms/sq.
5. 10 sprocket hole pitch cumulative tolerance ± 0.20 max.
6. Camber not to exceed 1 mm in 100mm.
7. MOLS# WBFBP -06C(2.0X2.0X0.5)
8. Dim in mm.



Reflow Condition (IR/Convection or VPR Reflow)



Classification Reflow Profiles

Profile Feature	Pb-Free / Green Assembly
Average ramp-up rate (T _L to T _P)	3°C/second max
Preheat - Temperature Min (T _{smin}) - Temperature Max (T _{smax}) - Time (min to max) (t _s)	150°C 200°C 60-180 seconds
Time maintained above: - Temperature (T _L) - Time (t _L)	217°C 60-150 seconds
Peak/Classification Temperature (T _P)	See table 1
Time within 5°C of actual Peak Temperature (t _p)	20-40 seconds
Ramp-down Rate	6°C/second max
Time 25°C to Peak Temperature	8 minutes max

Notes :

- 1) All temperatures refer to topside of the package.
- 2) Measured on the body surface.

Classification Reflow Profiles (Continued)

Table 1. Pb-free / Green Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm ³ <350	Volume mm ³ 350~2000	Volume mm ³ ≥2000
<2.5 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6-2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*

Notes :

* Tolerance: The device manufacturer/supplier shall assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.