



正基科技股份有限公司

# SPECIFICATION

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PRODUCT NAME : AP6441

	APPROVED	CHECKED	PREPARED	DCC ISSUE
NAME				



# AMPAK

## AP6441

WiFi 11a/b/g/n +Bluetooth 4.0 +NFC  
SIP Module Spec Sheet

# Revision History

Date	Revision Content	Revised By	Version
2012/10/18	- Initial released	Brian	1.0
2012/12/18	- Pin definition modify	Joe	1.1
2013/01/23	- Pin definition modify	Joe	1.2
2013/04/26	- Specification modify	Joe	1.3
2013/05/06	- BT Frequency Band modified	Brian	1.4
2013/12/10	- Block Diagram modified	Brian	1.5
2014/03/10	- Introduction modified	Brian	1.6

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# 1. Introduction

AMPAK Technology would like to announce a low-cost and low-power consumption module, with integrated dual band (2.4GHz/5GHz) IEEE 802.11 a/b/g and single-stream IEEE 802.11n MAC/baseband/radio and Bluetooth 4.0. It also integrates a low power NFC controller .

The integrated module provides SDIO V2.0 Host interface for Wi-Fi, high-speed UART is provided for the Bluetooth Host interface. Separate independent interface I2C for NFC are also provided.

This compact module is a total solution for a combination of WiFi dual mode + BT4.0 + NFC technologies. The module is specifically developed for mobiles, tablets or handheld wireless system devices.

## 2. Features

### IEEE 802.11x Key Features

- Dual-band 2.4GHz/5GHz 802.11a/b/g/n.
- Single-stream IEEE 802.11n support for 20MHz and 40MHz channels provides PHY layer rates up to 150Mbps.
- WLAN host interface options: SDIO v2.0 — up to 50 MHz clock rate
- Support a single antenna shared between WLAN and Bluetooth.
- Security: WEP, WPS, WPA, WPA2, WMM, WAPI, AES,...

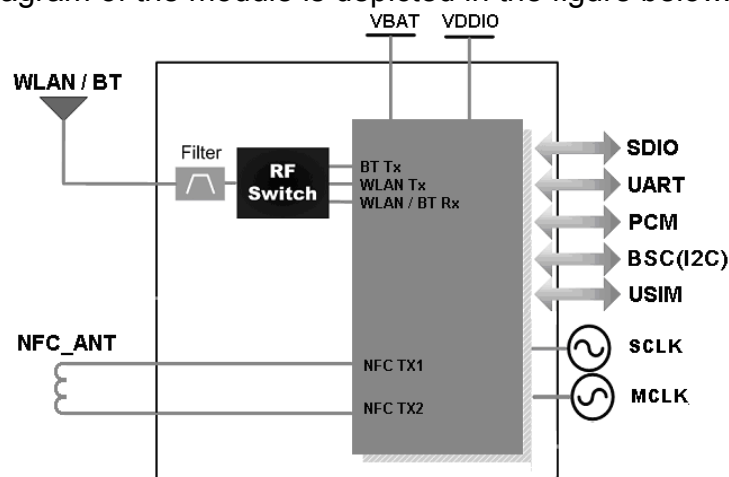
### Bluetooth Features

- Bluetooth V4.0(BLE) Low Energy with provisions for supporting future specifications.
- Bluetooth Class1 or Class2 transmitter operation.
- BT host digital interface UART(up to 4 Mbps) with support all Bluetooth4.0 package types
- Multipoint operation with up to seven active ACL links, three active SCO and eSCO connections.
- Full support for power savings modes (standard sniff, deep sleep modes)
- ECI - enhanced coexistence support, ability to coordinate BT SCO transmissions around WLAN receives

### NFC Features

- Reader/Writer (R/W) mode
- Active and Passive Peer-to-Peer (P2P) mode
- Tag/card Emulation mode with supports dual Single Wire Protocol (SWP) interfaces for SWP\_0/SWP\_1 dual UICC SIM card.
- Lead Free design which is compliant with ROHS requirements.

A simplified block diagram of the module is depicted in the figure below.



## 3. Deliverables

### 3.1 Deliverables

The following products and software will be part of the product.

- Module with packaging
- Evaluation Kits
- Software utility for integration, performance test.
- Product Datasheet.
- Agency certified pre-tested report with the adapter board.

### 3.2 Regulatory certifications

The product delivery is a pre-tested module, without the module level certification. For module approval, the platform's antennas are required for the certification.

## 4. General Specification

### 4.1 General Specification

Model Name	AP6441
Product Description	Supports Wi-Fi dual mode /Bluetooth/NFC
Dimension	L x W x H: 12.0 x 12.0 x 1.5 (typical) mm
WiFi Interface	SDIOV2.0 (4bit/1bit)
BT Interface	UART/ PCM
NFC Interface	I2C
Operating temperature	-30°C to 85°C
Storage temperature	-40°C to 85°C
Humidity	Operating Humidity 10% to 95% Non-Condensing

### 4.2 Voltages

#### 4.2.1 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
VBAT	Input supply Voltage	-0.5	5	V
VDDIO	Digital/Bluetooth/SDIO/ I/O Voltage	-0.5	3.6	V

#### 4.2.2 Recommended Operating Rating

The module requires two power supplies: VBAT and VDDIO.

	Min.	Typ.	Max.	Unit
Operating Temperature	-30	25	85	deg.C
VBAT	3.0	3.6	4.8	V
VDDIO	1.6	3.3	3.4	V



## 5. WiFi RF Specification

### 5.1 2.4GHz & 5GHz RF Specification

Conditions : VBAT=3.6V ; VDDIO=3.3V ; Temp:25°C

Feature	Description
WLAN Standard	IEEE 802.11a/b/g/n, WiFi compliant
Frequency Range	2.400 GHz ~ 2.497 GHz (2.4 GHz ISM Band) 4.900 GHz ~ 5.845 GHz (5.0 GHz ISM Band)
Number of Channels	2.4GHz : Ch1 ~ Ch14 5.0GHz : Please see the table <sup>1</sup>
Modulation	802.11a : OFDM /64-QAM, 16-QAM, QPSK, BPSK 802.11b : DQPSK, DBPSK, CCK 802.11 g/n : OFDM /64-QAM, 16-QAM, QPSK, BPSK
Output Power	802.11a /54Mbps : 13 dBm ± 1.5 dB @ EVM ≤ -25dB
	802.11b /11Mbps : 16 dBm ± 1.5 dB @ EVM ≤ -9dB
	802.11g /54Mbps : 15 dBm ± 1.5 dB @ EVM ≤ -25dB
	802.11n /MCS7 : 14 dBm ± 1.5 dB @ EVM ≤ -28dB
Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0 PER @ -88 dBm, typical
	- MCS=1 PER @ -84 dBm, typical
	- MCS=2 PER @ -82 dBm, typical
	- MCS=3 PER @ -80 dBm, typical
	- MCS=4 PER @ -77 dBm, typical
	- MCS=5 PER @ -74dBm, typical
	- MCS=6 PER @ -72 dBm, typical
- MCS=7 PER @ -70 dBm, typical	
Receive Sensitivity (11n,40MHz) @10% PER	- MCS=0 PER @ -87 dBm, typical
	- MCS=1 PER @ -83 dBm, typical
	- MCS=2 PER @ -81 dBm, typical
	- MCS=3 PER @ -79 dBm, typical
	- MCS=4 PER @ -77 dBm, typical
	- MCS=5 PER @ -76 dBm, typical
	- MCS=6 PER @ -71 dBm, typical
- MCS=7 PER @ -69 dBm, typical	
Receive Sensitivity (11g) @10% PER	- 6Mbps PER @ -89 dBm, typical
	- 9Mbps PER @ -88 dBm, typical
	- 12Mbps PER @ -86 dBm, typical

	- 18Mbps PER @ -84 dBm, typical
	- 24Mbps PER @ -82 dBm, typical
	- 36Mbps PER @ -78 dBm, typical
	- 48Mbps PER @ -75 dBm, typical
	- 54Mbps PER @ -72 dBm, typical
Receive Sensitivity (11b) @8% PER	- 1Mbps PER @ -95 dBm, typical
	- 2Mbps PER @ -94 dBm, typical
	- 5.5Mbps PER @ -90 dBm, typical
	- 11Mbps PER @ -87 dBm, typical
Receive Sensitivity (11a) @10% PER	- 6Mbps PER @ -88 dBm, typical
	- 9Mbps PER @ -86 dBm, typical
	- 12Mbps PER @ -84 dBm, typical
	- 18Mbps PER @ -82 dBm, typical
	- 24Mbps PER @ -80 dBm, typical
	- 36Mbps PER @ -78 dBm, typical
	- 54Mbps PER @ -72 dBm, typical
Data Rate	802.11a : 6, 9, 12, 18, 24, 36, 48, 54Mbps
	802.11b : 1, 2, 5.5, 11Mbps
	802.11g : 6, 9, 12, 18, 24, 36, 48, 54Mbps
	802.11n: MCS0, MCS1, MCS2, MCS3, MCS4, MCS5, MCS6, MCS7
Maximum Input Level	802.11b : -10 dBm
	802.11a/g/n : -20 dBm
Antenna Reference	Small antennas with 0~2 dBi peak gain

<sup>1</sup>5GHz Channel table

Band (GHz)	Operating Channel Numbers	Channel center frequencies(MHz)
5.15GHz~5.25GHz	36	5180
	40	5200
	44	5220
	48	5240
5.25GHz~5.35GHz	52	5260
	56	5280
	60	5300
	64	5320
5.5GHz~5.7GHz	100	5500
	104	5520
	108	5540
	112	5560
	116	5580
	120	5600
	124	5620

	128	5640
	132	5660
	136	5680
	140	5700
5.725GHz~5.825GHz	149	5745
	153	5765
	157	5785
	161	5805

## 6. Bluetooth Specification

### 6.1 Bluetooth Specification

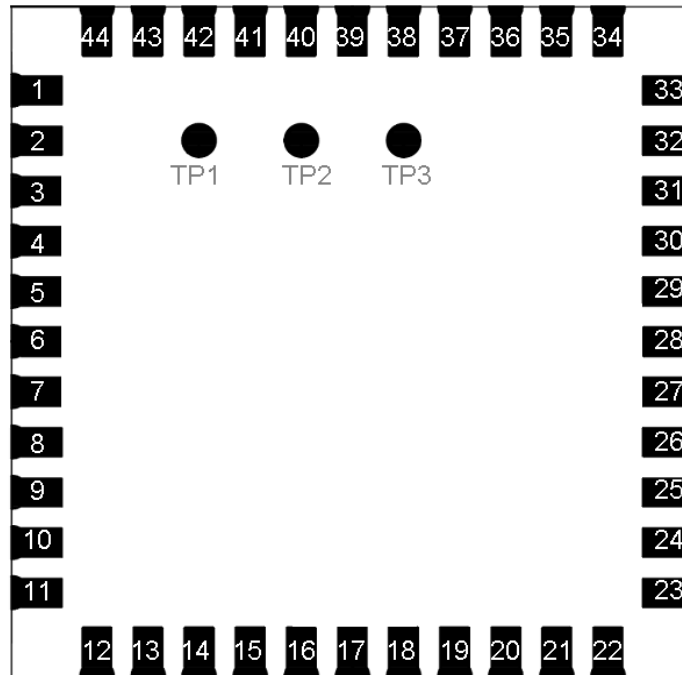
Conditions : VBAT=3.6V ; VDDIO=3.3V ; Temp:25°C

Feature	Description		
<b>General Specification</b>			
Bluetooth Standard	Bluetooth V4.0 of 1, 2 and 3 Mbps.		
Host Interface	UART		
Antenna Reference	Small antennas with 0~2 dBi peak gain		
Frequency Band	2402 MHz ~ 2480 MHz		
Number of Channels	79 channels		
Modulation	FHSS, GFSK, DPSK, DQPSK		
<b>RF Specification</b>			
	<b>Min.</b>	<b>Typical.</b>	<b>Max.</b>
Output Power (Class 1.5)		10 dBm	
Output Power (Class 2)		2 dBm	
Sensitivity @ BER=0.1% for GFSK (1Mbps)		-86 dBm	
Sensitivity @ BER=0.01% for $\pi/4$ -DQPSK (2Mbps)		-86 dBm	
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)		-80 dBm	
Maximum Input Level	GFSK (1Mbps):-20dBm		
	$\pi/4$ -DQPSK (2Mbps) :-20dBm		
	8DPSK (3Mbps) :-20dBm		

# 7. Pin Assignments

## 7.1 Pin Outline

< TOP VIEW >



## 7.2 Pin Definition

NO	Name	Type	Description
1	GND	—	Ground connections
2	WL_BT_ANT	I/O	RF I/O port
3	GND	—	Ground connections
4	NC	—	Floating (Don't connected to ground)
5	N_WAKE	I	HOST wake-up NFC device
6	BT_WAKE	I	HOST wake-up Bluetooth device
7	BT_HOST_WAKE	O	Bluetooth device to wake-up HOST
8	N_HOST_WAKE	O	NFC device to wake-up HOST
9	VBAT	P	Main power voltage source input
10	XTAL_IN	I	XTAL oscillator input
11	XTAL_OUT	O	XTAL oscillator output
12	WL_REG_ON	I	Internal regulators power enable/disable
13	WL_HOST_WAKE	O	WLAN to wake-up HOST

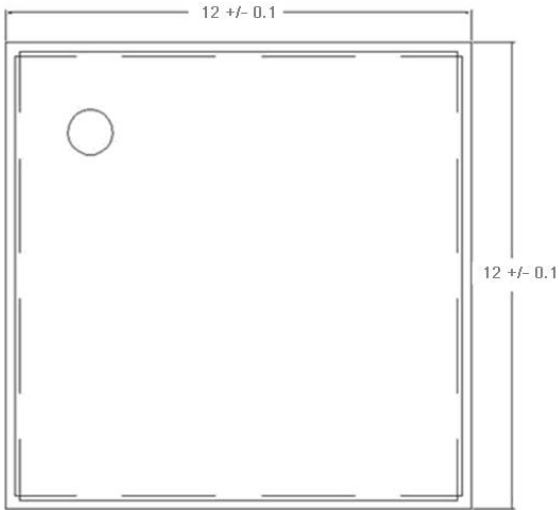
14	SDIO_DATA_2	I/O	SDIO data line 2
15	SDIO_DATA_3	I/O	SDIO data line 3
16	SDIO_DATA_CMD	I/O	SDIO command line
17	SDIO_DATA_CLK	I/O	SDIO clock line
18	SDIO_DATA_0	I/O	SDIO data line 0
19	SDIO_DATA_1	I/O	SDIO data line 1
20	GND	—	Ground connections
21	VIN_LDO_OUT	P	Internal Buck voltage generation pin
22	VDDIO	P	I/O Voltage supply input
23	VIN_LDO	P	Internal Buck voltage generation pin
24	LPO	I	Low power oscillator clock input (32.768KHz)
25	PCM_OUT	O	PCM Data output
26	PCM_CLK	I/O	PCM clock
27	PCM_IN	I	PCM data input
28	PCM_SYNC	I/O	PCM sync signal
29	EE_I2C_SDA	I/O	1.8V EEPROM I2C data line
30	EE_I2C_SCL	I/O	1.8V EEPROM I2C clock line
31	GND	—	Ground connections
32	NC	—	Floating (Don't connected to ground)
33	GND	—	Ground connections
34	BT_RST_N	I	Low asserting reset for Bluetooth core
35	N_I2C_SDA	I	BSC Serial Data Line
36	GND	—	Ground connections
37	N_I2C_SCL	I	BSC Serial Clock
38	N_REG_PU	I	NFC Internal regulators power enable/disable
39	TX2	O	NFC Tx coil output 2
40	TX1	O	NFC Tx coil output 1
41	UART_RTS_N	O	Bluetooth UART interface
42	UART_TXD	O	Bluetooth UART interface
43	UART_RXD	I	Bluetooth UART interface
44	UART_CTS_N	I	Bluetooth UART interface
45	TP1	I/O	NFC_VDDSWPIO(SWP I/O)
46	TP2	O	NFC_VDDSWP_OUT(UICC support out)
47	TP3	I	NFC_VDDSWP_IN(Platform UICC supply in)

# 8. Dimensions

## 8.1 Physical Dimensions

(Unit: mm)

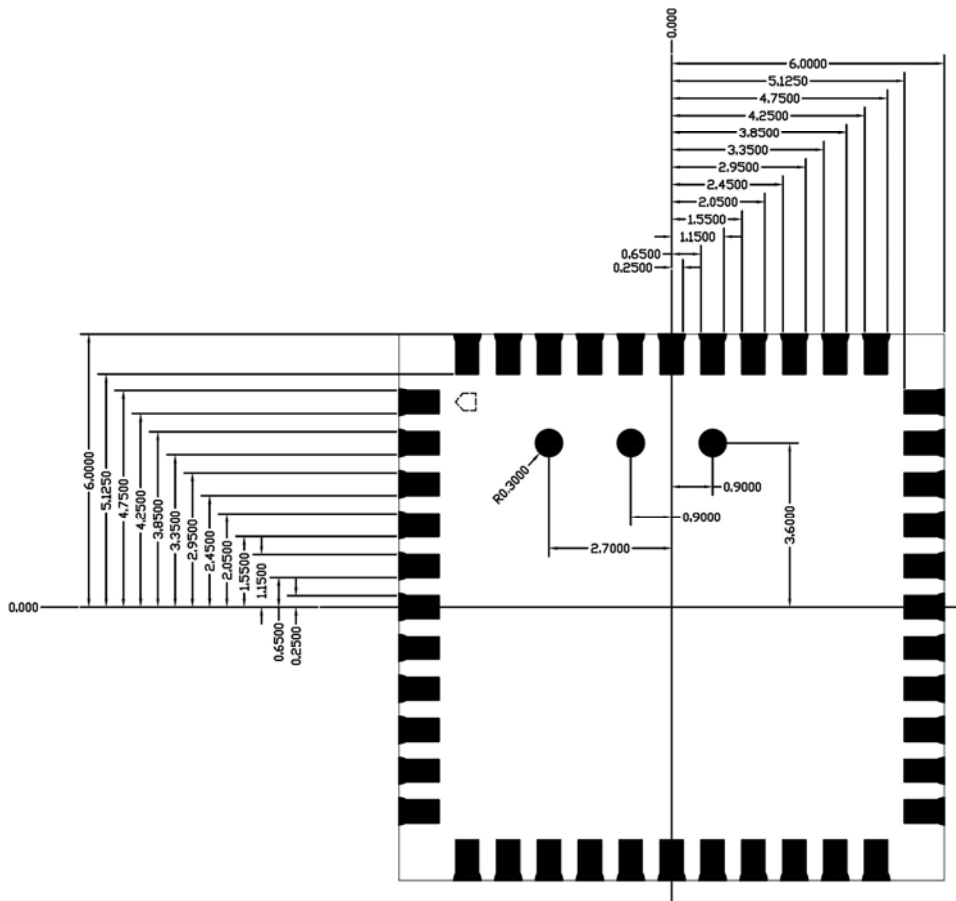
< TOP VIEW >



< Side View >



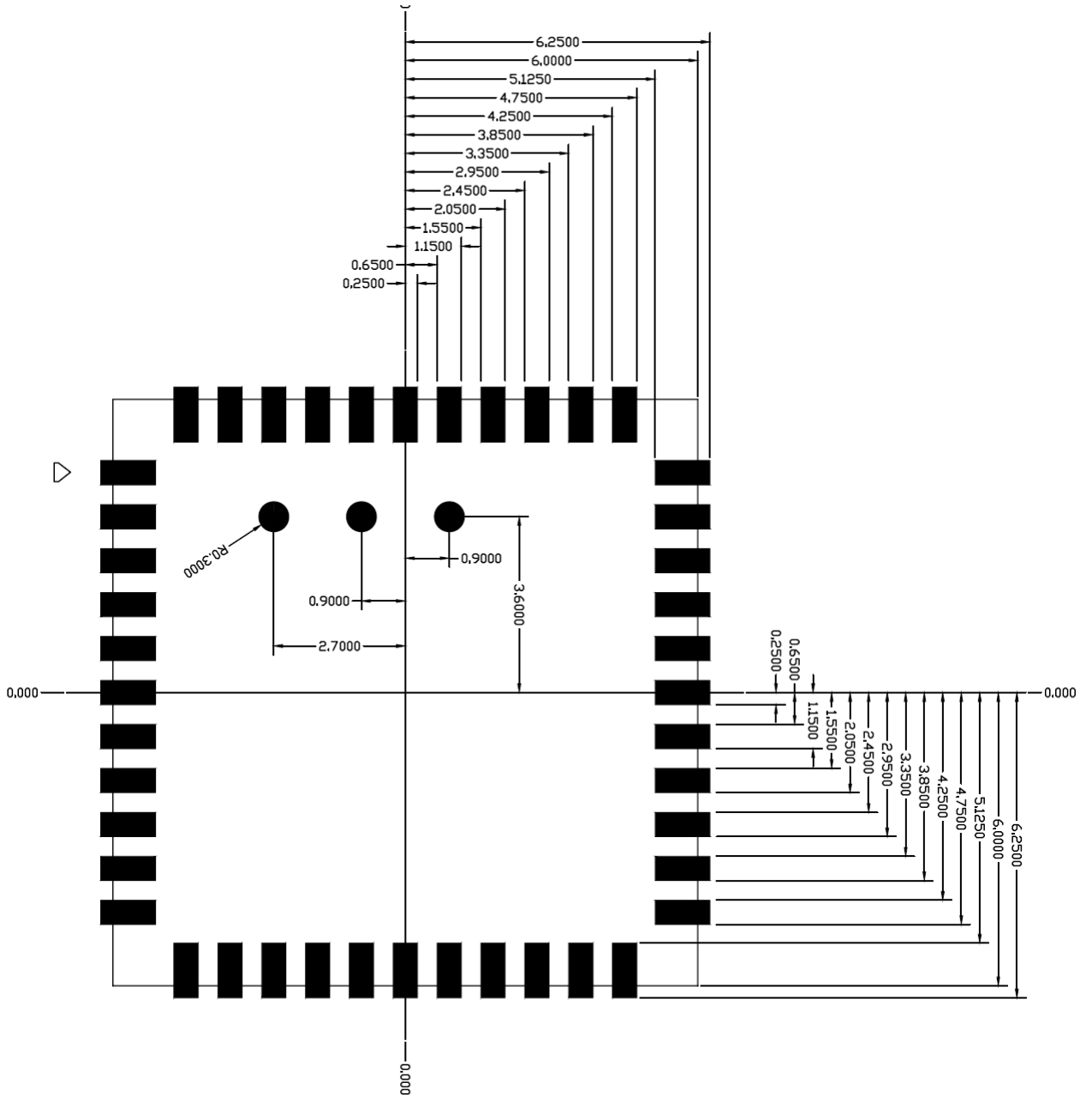
< TOP VIEW >



## 8.2 Layout Recommendation

(Unit: mm)

< TOP VIEW >



## 9. External clock reference

External LPO signal characteristics

Parameter	Specification	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	±30	ppm
Duty cycle	30 - 70	%
Input signal amplitude	400 to 1800	mV, p-p
Signal type	Square-wave	-
Input impedance	>100k <5	Ω pF
Clock jitter (integrated over 300Hz – 15KHz)	<1	Hz
Output high voltage	0.7V <sub>io</sub> - V <sub>io</sub>	V

### 9.1 SDIO Pin Description

The module supports SDIO version 2.0 for 4-bit modes (100 Mbps), and high speed 4-bit (50 MHz clocks – 200 Mbps). It has the ability to stop the SDIO clock and map the interrupt signal into a GPIO pin. This ‘out-of-band’ interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force the control of the gated clocks from within the WLAN chip is also provided.

- ❖ Function 0 Standard SDIO function (Max BlockSize / ByteCount = 32B)
- ❖ Function 1 Backplane Function to access the internal System On Chip (SOC) address space (Max BlockSize / ByteCount = 64B)
- ❖ Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max BlockSize/ByteCount=512B)

SDIO Pin Description

SD 4-Bit Mode	
DATA0	Data Line 0
DATA1	Data Line 1 or Interrupt
DATA2	Data Line 2 or Read Wait
DATA3	Data Line 3
CLK	Clock
CMD	Command Line



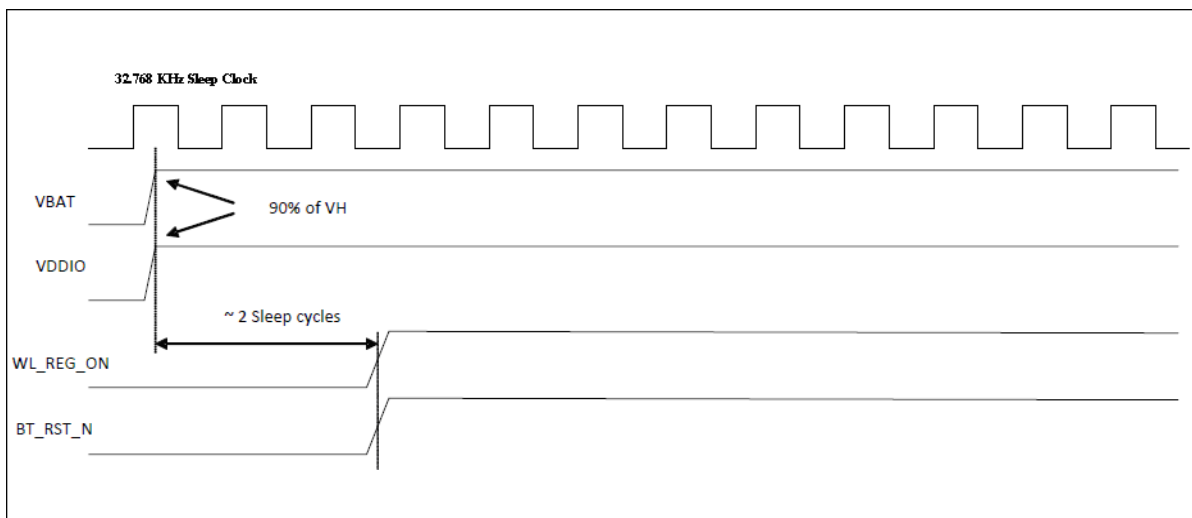
# 10. Host Interface Timing Diagram

## 10.1 Power-up Sequence Timing Diagram

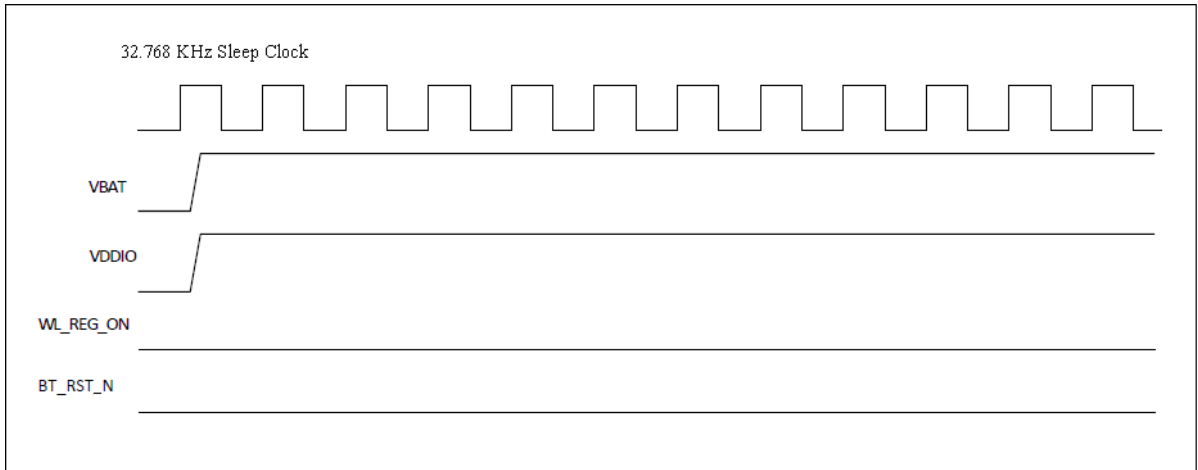
The module has signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN and internal regulator blocks. These signals are described below.

Additionally, diagrams are provided to indicate proper sequencing of the signals for various operating states. The timing value indicated are minimum required values: longer delays are also acceptable.

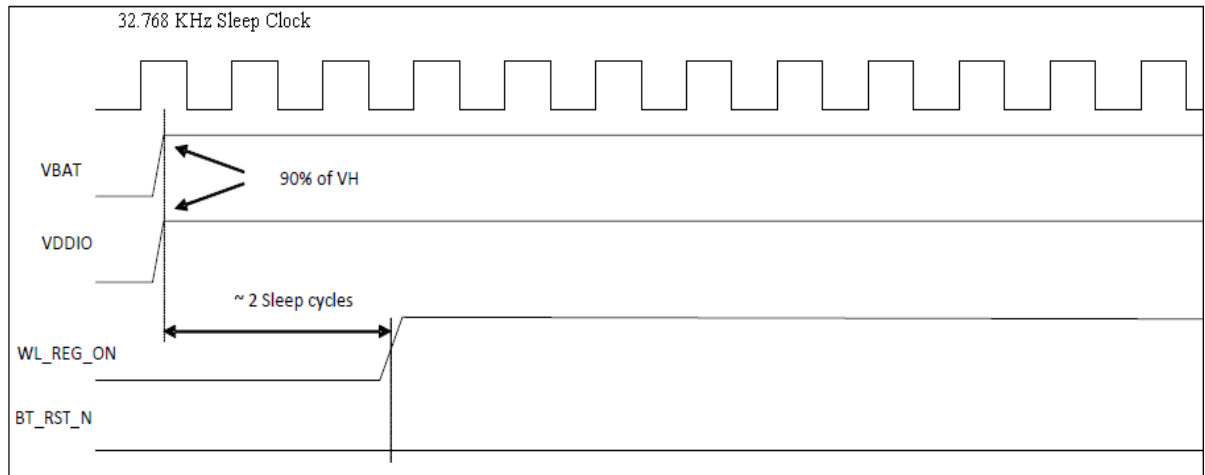
- ※ WL\_REG\_ON: Used by the PMU to power up the WLAN section. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset.
- ※ BT\_RST\_N: Low asserting reset for Bluetooth only. This pin has no effect on WLAN and does not control any PMU functions. This pin must be driven high or low (not left floating).



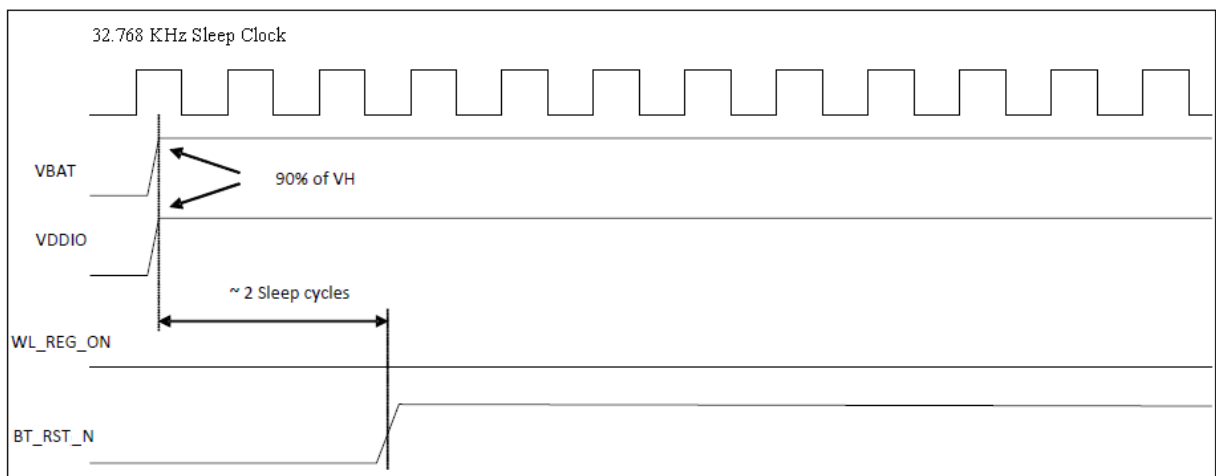
WLAN=ON, Bluetooth=ON



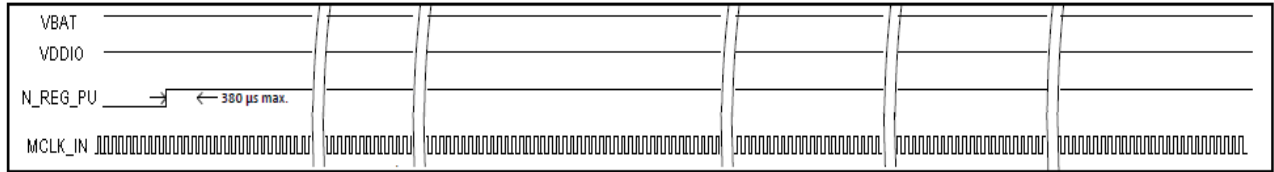
WLAN=OFF, Bluetooth=OFF



WLAN=ON, Bluetooth=OFF

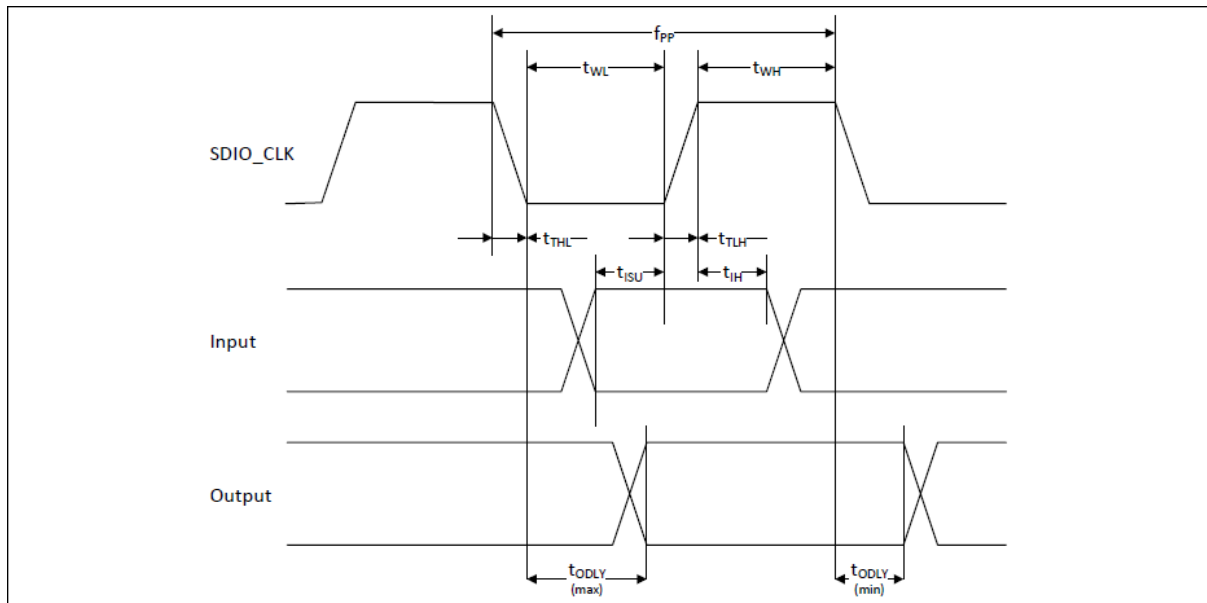


WLAN=OFF, Bluetooth=ON



NFC ON

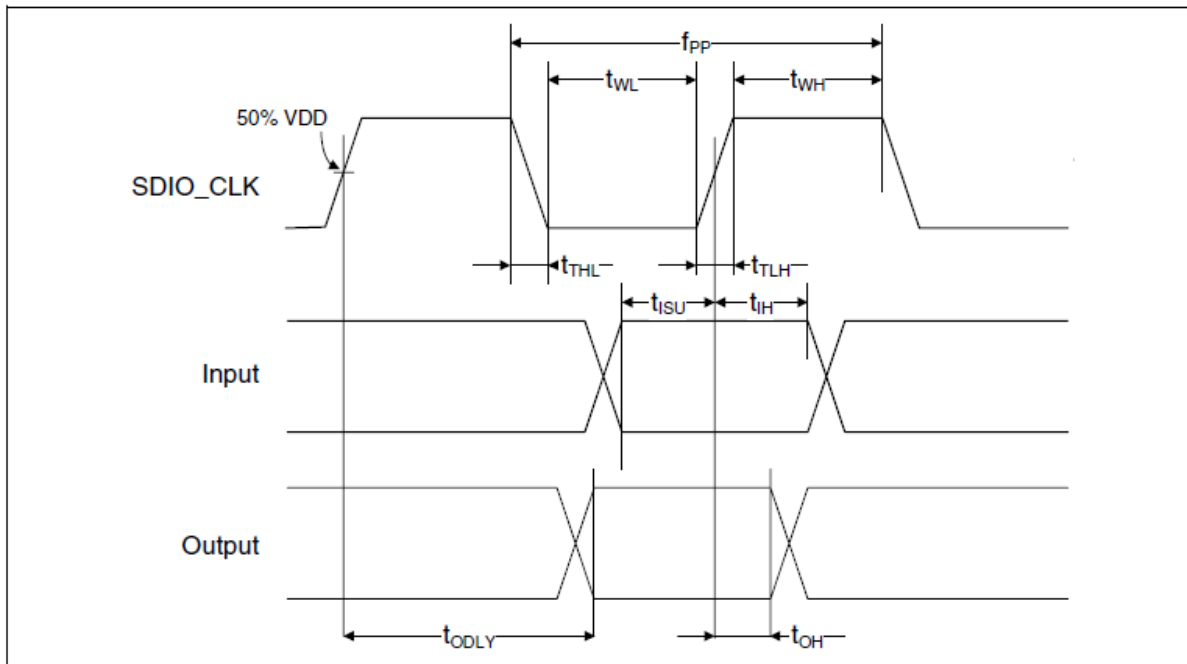
### 10.2 SDIO Default Mode Timing Diagram



Parameter	Symbol	Minimum	Typical	Maximum	Unit
<b>SDIO CLK (All values are referred to minimum VIH and maximum VIL<sup>b</sup>)</b>					
Frequency-Data Transfer mode	f <sub>PP</sub>	0	-	25	MHz
Frequency-Identification mode	f <sub>OD</sub>	0	-	400	kHz
Clock low time	t <sub>WL</sub>	10	-	-	ns
Clock high time	t <sub>WH</sub>	10	-	-	ns
Clock rise time	t <sub>TLH</sub>	-	-	10	ns
Clock low time	t <sub>THL</sub>	-	-	10	ns
<b>Inputs: CMD, DAT (referenced to CLK)</b>					
Input setup time	t <sub>ISU</sub>	5	-	-	ns
Input hold time	t <sub>IH</sub>	5	-	-	ns
<b>Outputs: CMD, DAT (referenced to CLK)</b>					
Output delay time - Data Transfer mode	t <sub>ODLY</sub>	0	-	14	ns
Output delay time - Identification mode	t <sub>ODLY</sub>	0	-	50	ns

a. Timing is based on CL ≤ 40pF load on CMD and Data.  
 b. min(V<sub>IH</sub>) = 0.7 × V<sub>DDIO</sub> and max(V<sub>IL</sub>) = 0.2 × V<sub>DDIO</sub>.

### 10.3 SDIO High Speed Mode Timing Diagram



Parameter	Symbol	Minimum	Typical	Maximum	Unit
<b>SDIO CLK (All values are referred to minimum VIH and maximum VIL<sup>b</sup>)</b>					
Frequency-Data Transfer mode	f <sub>PP</sub>	0	-	50	MHz
Frequency-Identification mode	f <sub>OD</sub>	0	-	400	kHz
Clock low time	t <sub>WL</sub>	7	-	-	ns
Clock high time	t <sub>WH</sub>	7	-	-	ns
Clock rise time	t <sub>TLH</sub>	-	-	3	ns
Clock low time	t <sub>TLH</sub>	-	-	3	ns
<b>Inputs: CMD, DAT (referenced to CLK)</b>					
Input setup time	t <sub>ISU</sub>	6	-	-	ns
Input hold time	t <sub>IH</sub>	2	-	-	ns
<b>Outputs: CMD, DAT (referenced to CLK)</b>					
Output delay time - Data Transfer mode	t <sub>ODLY</sub>	-	-	14	ns
Output hold time	t <sub>OH</sub>	2.5	-	-	ns
Total system capacitance (each line)	CL	-	-	40	pF

a. Timing is based on CL ≤ 40pF load on CMD and Data.

b. min(V<sub>Ih</sub>) = 0.7 x V<sub>DDIO</sub> and max(V<sub>Ih</sub>) = 0.2 x V<sub>DDIO</sub>.

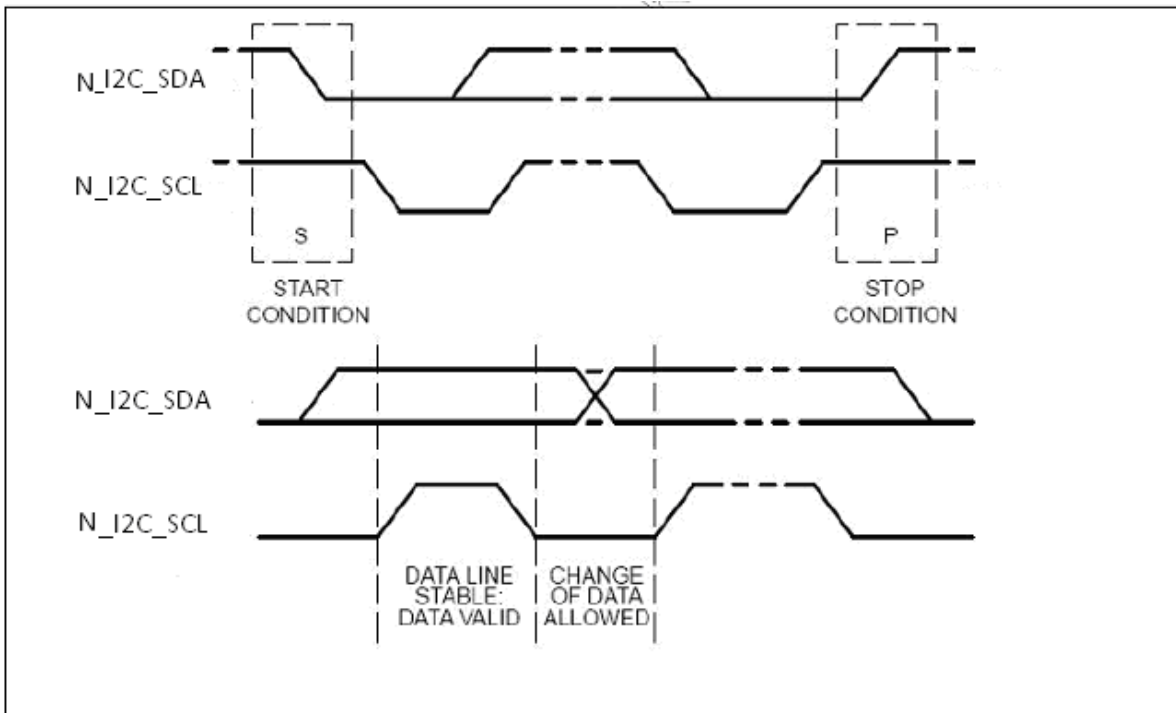
### 10.4 BSC (I2C-Compatible)

Following are the main features of the BSC host interface:

- Slave mode
- Low-speed mode (100 kbps), fast mode (400 kbps), and high-speed mode (3.4 Mbps) supported. Due to practical constraints imposed by parasitic capacitance and pull-up resistor values, especially in a multidrop system, recommend that this be limited to 1.7 Mbps.
- 7-bit or 10-bit addressing mode; default boot-up of fixed 10-bit address (0x1FA), thereafter configurable to 7-bit or 10-bit addresses

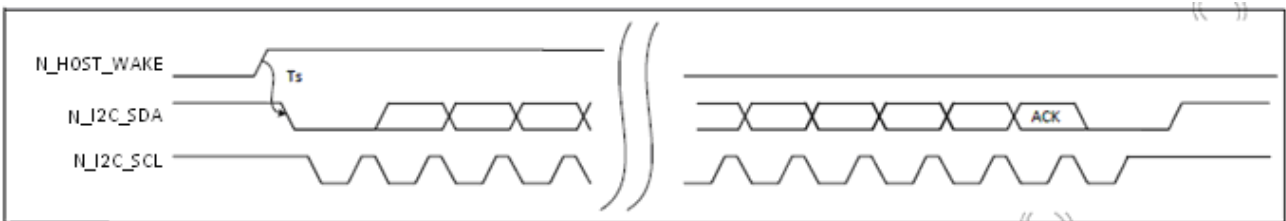
- Dedicated TX and RX FIFOs, 272 bytes each.
- Digital deglitching filter implemented. Uses simple majority of 3 and will filter spikes up to 42 ns.
- High-speed reference not required for operation. (Certain accesses in sleep mode will initiate the wakeup function.)

The BSC timing waveform is shown in



I2C Timing Waveform

NFC\_HOST\_WAKE is an output signal from the Module to the host that it wishes to communicate. The timing diagram shows NFC\_HOST\_WAKE as active high. The NFC\_HOST\_WAKE signal stays high until after the first byte has been read by the host.



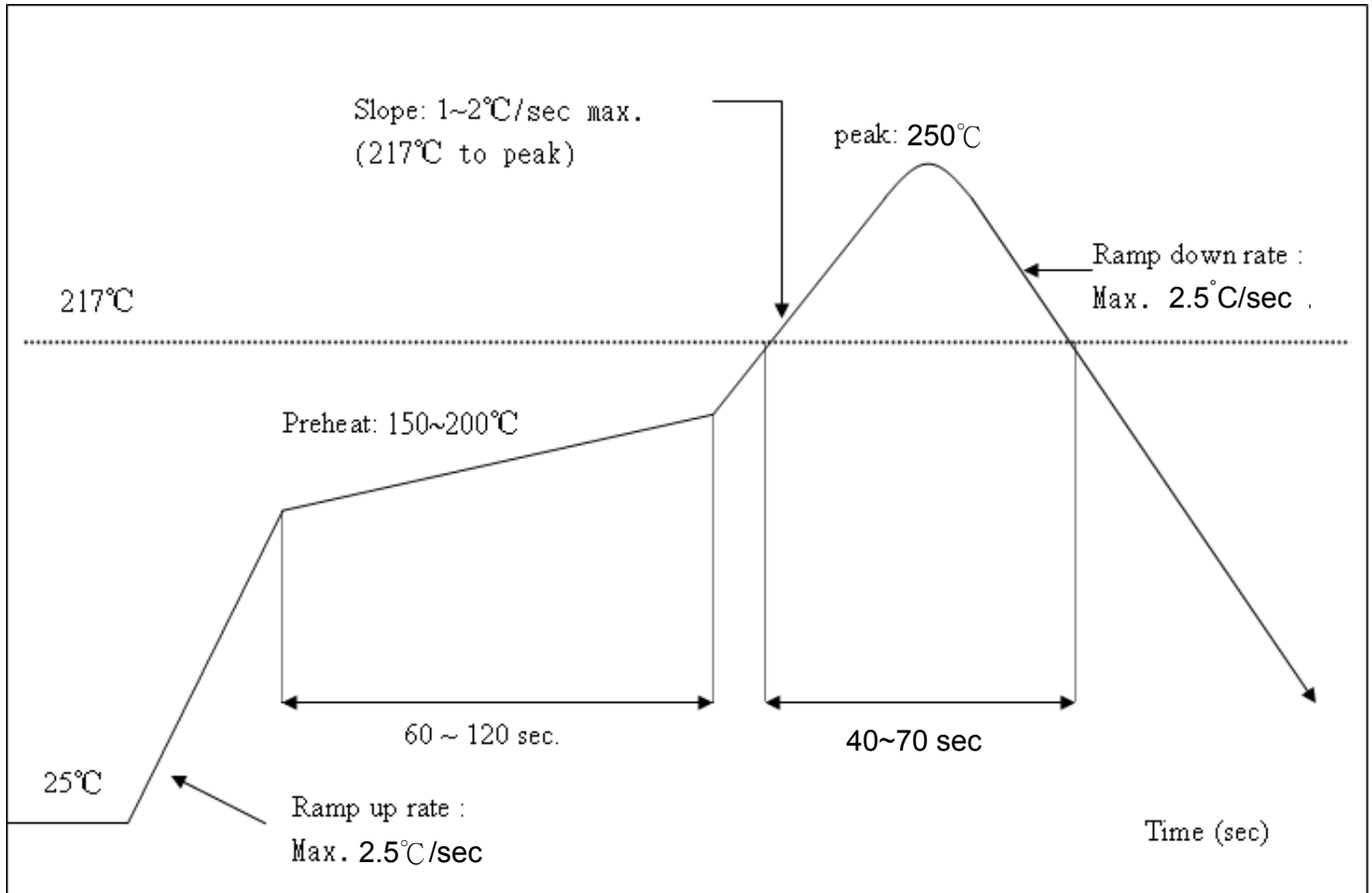
N\_HOST\_WAKE Timing Waveform

# 11. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <250°C

Number of Times : ≤2 times



# 12. Package Information

## 12.1 Label






Label A → Anti-static and humidity notice








Label B → MSL caution / Storage Condition

	<b>Caution</b> This bag contains MOISTURE-SENSITIVE DEVICES	LEVEL <input type="text"/>
	<small>If blank, see adjacent bar code label</small>	
<ol style="list-style-type: none"> <li>Calculated shelf life in sealed bag: 12 months at &lt;40°C and &lt;90% relative humidity (RH)</li> <li>Peak package body temperature: _____ °C <small>If blank, see adjacent bar code label</small></li> <li>After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be             <ol style="list-style-type: none"> <li>Mounted within: _____ hours of factory conditions <small>If blank, see adjacent bar code label</small> ≤30°C/60% RH, or</li> <li>Stored per J-STD-033</li> </ol> </li> <li>Devices require bake, before mounting, if:             <ol style="list-style-type: none"> <li>Humidity Indicator Card reads &gt;10% for level 2a - 5a devices or &gt;60% for level 2 devices when read at 23 ± 5°C</li> <li>3a or 3b are not met</li> </ol> </li> <li>If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure</li> </ol>		
Bag Seal Date: _____ <small>If blank, see adjacent bar code label</small>		
<small>Note: Level and body temperature defined by IPC/JEDEC J-STD-020</small>		

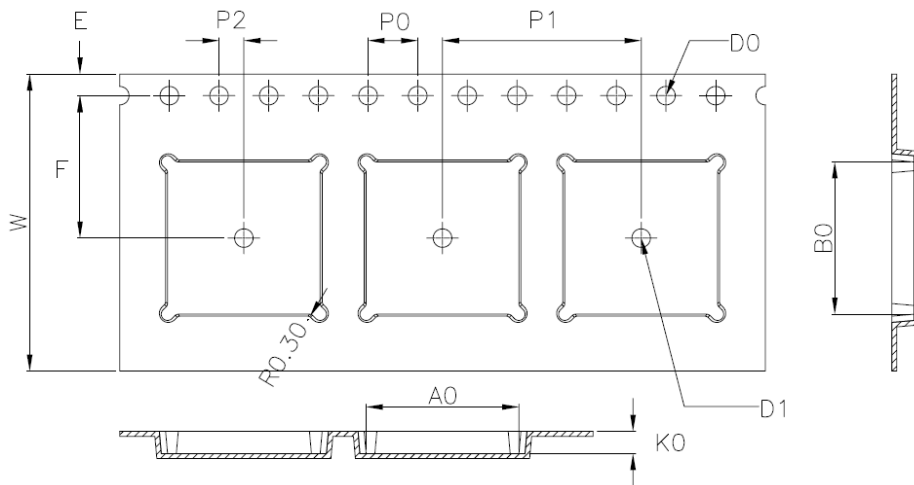
Label C → Inner box label .

<b>PKG S/N :</b>	 9PKG12013100001
<b>Model:</b>	 XXXXXXXXXXXX
<b>P/N :</b>	 99P-W01-0048R
<b>Qty :</b>	 1500
<b>Date Code :</b>	 1205
<b>Lot Code :</b>	 T0C102B

Label D → Carton box label .

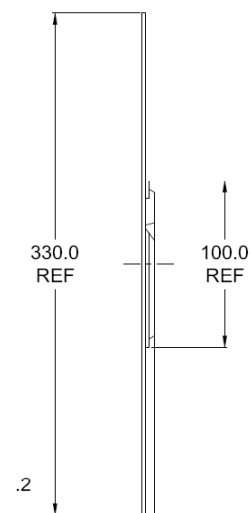
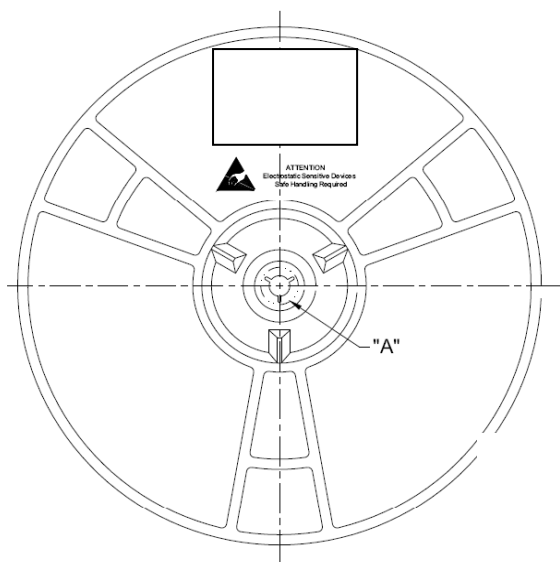
<b>AMPAK Technology</b>	
<b>Model Name :</b>	 XXXXXXXXXXXX
<b>Part No :</b>	 99P-W01-0048R
<b>Quantity :</b>	 7500 ea
<b>Lot D/C :</b>	 20081000033
<b>Manufacture :</b>	 2012/02/22

## 12.2 Dimension

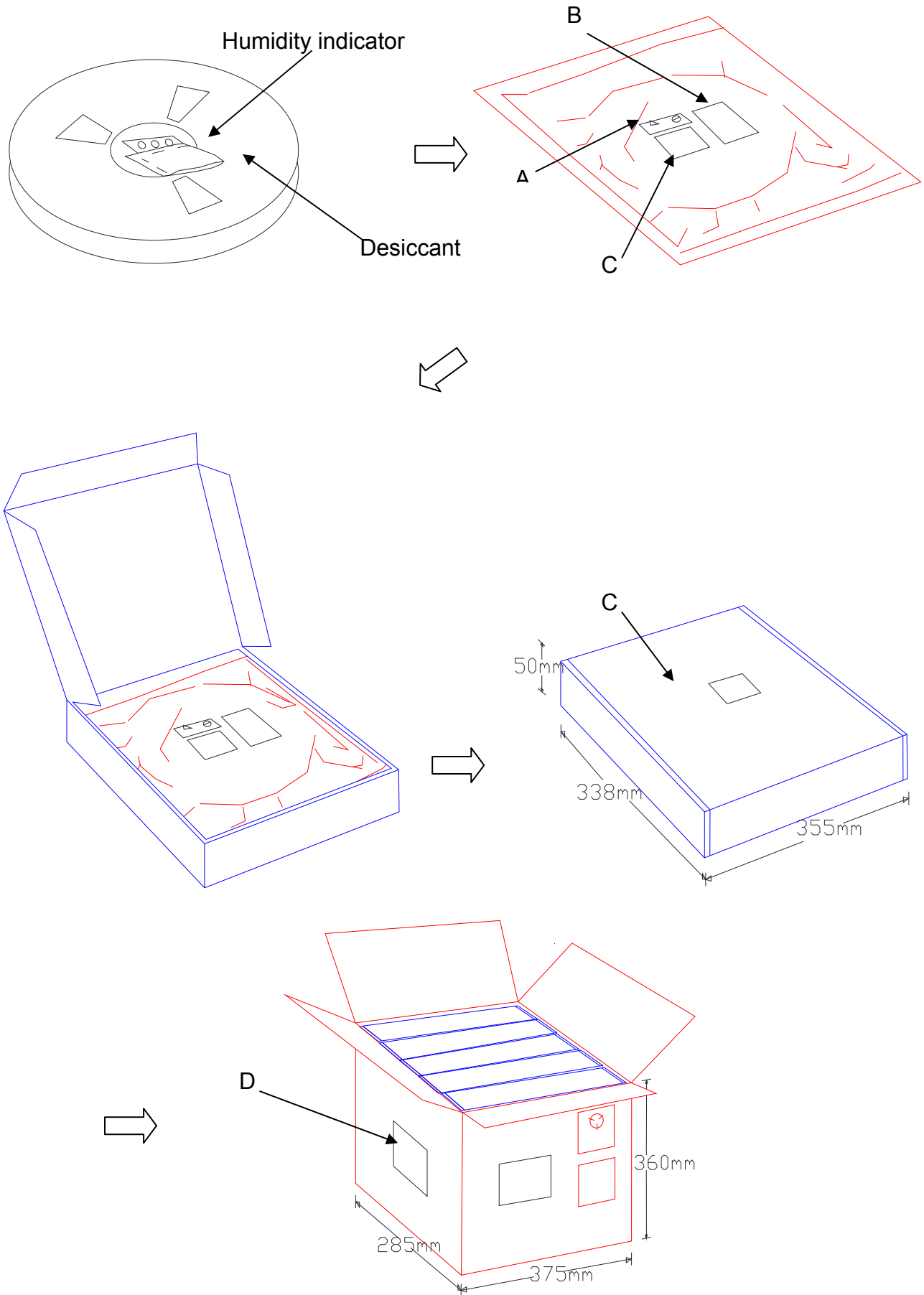


W	24.00±0.30
A0	12.30±0.10
B0	12.30±0.10
K0	1.80±0.10
E	1.75±0.10
F	11.50±0.10
P0	4.00±0.10
P1	16.00±0.10
P2	2.00±0.10
D0	1.50 $\begin{smallmatrix} +0.10 \\ -0.00 \end{smallmatrix}$
D1	∅1.50MIN


1. 10 sprocket hole pitch cumulative tolerance ±0.20.
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481-D requirements.
5. Thickness : 0.30±0.05mm.
6. Packing length per 22" reel : 98.5 Meters.(1:3)
7. Component load per 13" reel : 1500 pcs.







### 12.3 MSL Level / Storage Condition

	<p><b>Caution</b> This bag contains <b>MOISTURE-SENSITIVE DEVICES</b></p>	<table border="1" style="margin: auto;"> <tr><td style="padding: 2px;">LEVEL</td></tr> <tr><td style="text-align: center; font-size: 2em; padding: 10px;">4</td></tr> </table>	LEVEL	4
LEVEL				
4				
<p>Do not open except under controlled conditions</p>				
<p>1. Calculated shelf life in sealed bag: 12 months at &lt; 40°C and &lt; 90% relative humidity(RH)</p>				
<p>225°C   240°C   250°C   260°C</p>				
<p>2. Peak package body temperature:   <input type="checkbox"/>   <input type="checkbox"/>   <input checked="" type="checkbox"/>   <input type="checkbox"/></p>				
<p>3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must</p> <p style="margin-left: 20px;">a) Mounted within: 48 hours of factory conditions  <span style="margin-left: 40px;">&lt;30°C/60% RH, OR</span>            b) Stored at &lt;10% RH</p>				
<p>4. Devices require bake, before mounting, if:</p> <p style="margin-left: 20px;">a) Humidity Indicator Card is &gt;10% when read at 23±5°C            b) 3a or 3b not met</p>				
<p>5. If baking is required, devices may be baked for 24 hours at 125±5°C</p>				
<p>Note : If device containers cannot be subjected to high temperature or shorter bake times are desired, reference IPC/JEDEC J-STD-033 for bake procedure</p>				
<p>Bag Seal Date: <u>                    <b>See-SEAL DATE LABEL</b>                    </u></p>				
<p>Note: Level and body temperature defined by IPC/JEDEC J-STD-020</p>				

**※NOTE : Accumulated baking time should not exceed 96hrs**