5.5V TO 80V INPUT AUTOMOTIVE GRADE, 2.5A AND 3.5A NON-SYNCHRONOUS BUCK CONVERTER

Description

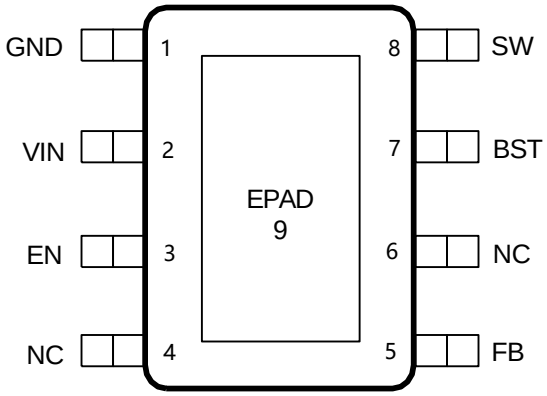
The AP68255Q/AP68355Q is an internally compensated, non-synchronous DC-DC buck converter with a default frequency of 300kHz. The device fully integrates a 500mΩ high-side power MOSFET power MOSFET to provide highly efficient step-down DC-DC conversion.

The AP68255Q/AP68355Q device is easily used by minimizing the external component count due to its adoption of Constant On-Time (COT) control to achieve fast transient response, easy loop stabilization, and low output voltage ripple.

The AP68255Q/AP68355Q design is optimized for Electromagnetic Interference (EMI) reduction. The device has a proprietary gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off times, which reduces high frequency radiated EMI noise caused by MOSFET switching.

The AP68255Q/AP68355Q is available in the standard Green SO-8EP package.

Pin Assignments



SO-8EP

Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results
  - Device Temperature Grade 1: -40°C to +125°C T_A
  - Device HBM ESD Classification Level 1C
  - Device CDM ESD Classification Level C5
- Functional Safety-Capable ISO26262 – Documentation Available to Aid Functional Safety System Design
- V_{IN} 5.5V to 80V
- 1.2V ±1.5% V_{REF}
- Continuous Output Current
  – AP68255Q: 2.5A
  – AP68355Q: 3.5A
- V_{OUT} Adjustable from 1.2V to 50V
- Overcurrent Protection (OCP)
- Thermal Protection
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **The AP68255Q/AP68355Q are suitable for automotive applications requiring specific change control; these parts are AEC-Q100 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.**
  https://www.diodes.com/quality/product-definitions/

Applications

- General-purpose point-of-load DC/DC power conversion
- Automotive infotainment
- Telecommunication systems
- Distributed power systems
- Home audio devices
- Consumer electronics
- Network systems
- FPGA, DSP, and ASIC supplies
- Green electronics

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit

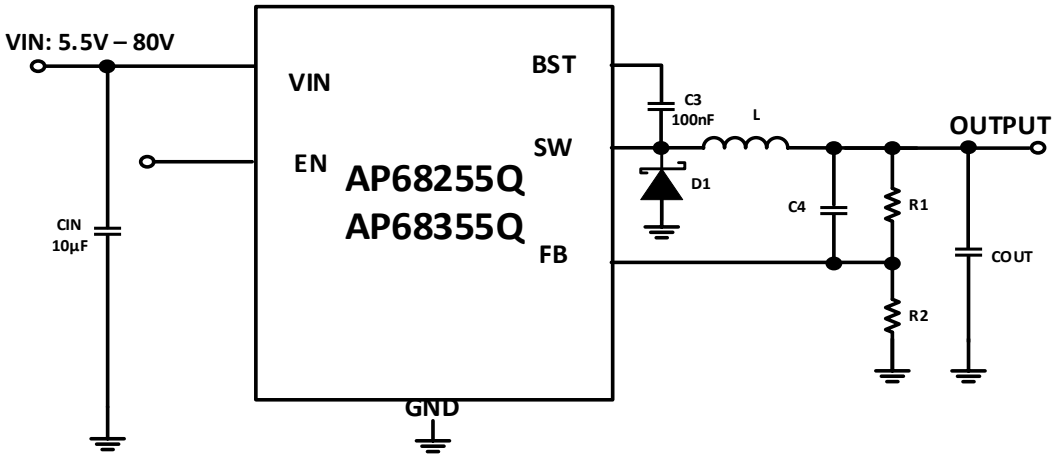


Figure 1. Typical Application Circuit

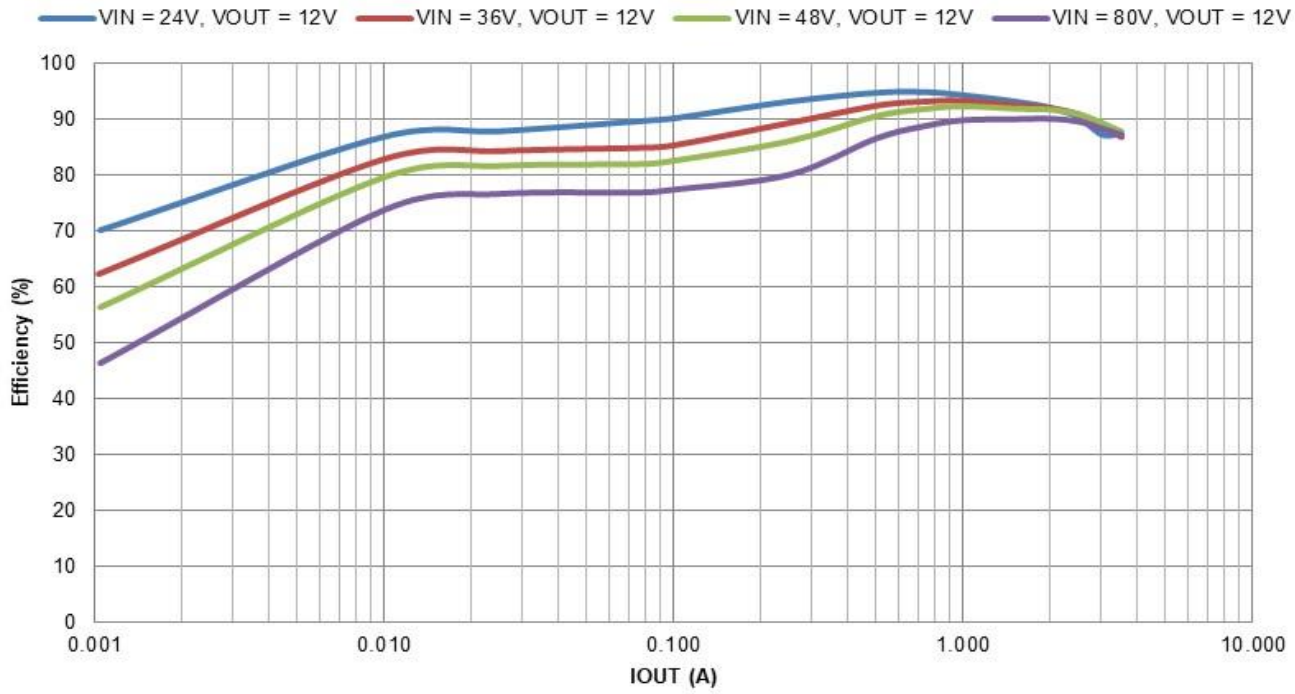


Figure 2. Efficiency vs. Output Current, V_{OUT} = 12V, f_{SW} = 300kHz, L = 68µH

Pin Descriptions

Pin Name	Pin Number	Function
GND	1	Analog ground is used for the control. Single point connection to the EPAD and the external Schottky diode power ground plane for proper electrical/thermal operations.
VIN	2	Power Input. VIN supplies the power to the IC, as well as the step-down converter switches. Drive VIN with a 5.5V to 80V power source. Bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC. See Input Capacitor.
EN	3	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator and low to turn it off. Leave floating for automatic startup. The EN has a precision threshold of 1.25V for programing the UVLO. See *Enable* section for more details.
NC	4, 6	Connect these NC pins to EPAD.
FB	5	Feedback Input. FB senses the output voltage and regulates it. Drive FB with a resistive divider connected to it from the output voltage to this pin. The feedback regulation voltage is 1.2V. See “Setting the Output Voltage”.
BST	7	High-Side Gate Drive Boost Input. BST supplies the drive for the high-side N-Channel MOSFET with a 0.1µF or greater capacitor from SW to BST to power the high-side switch.
SW	8	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BST to power the high-side switch.
EPAD	9	Heat dissipation path of die. Electrical connection to GND pin. Must be connected to ground plane on PCB for proper operation and optimized thermal performance.

Functional Block Diagram

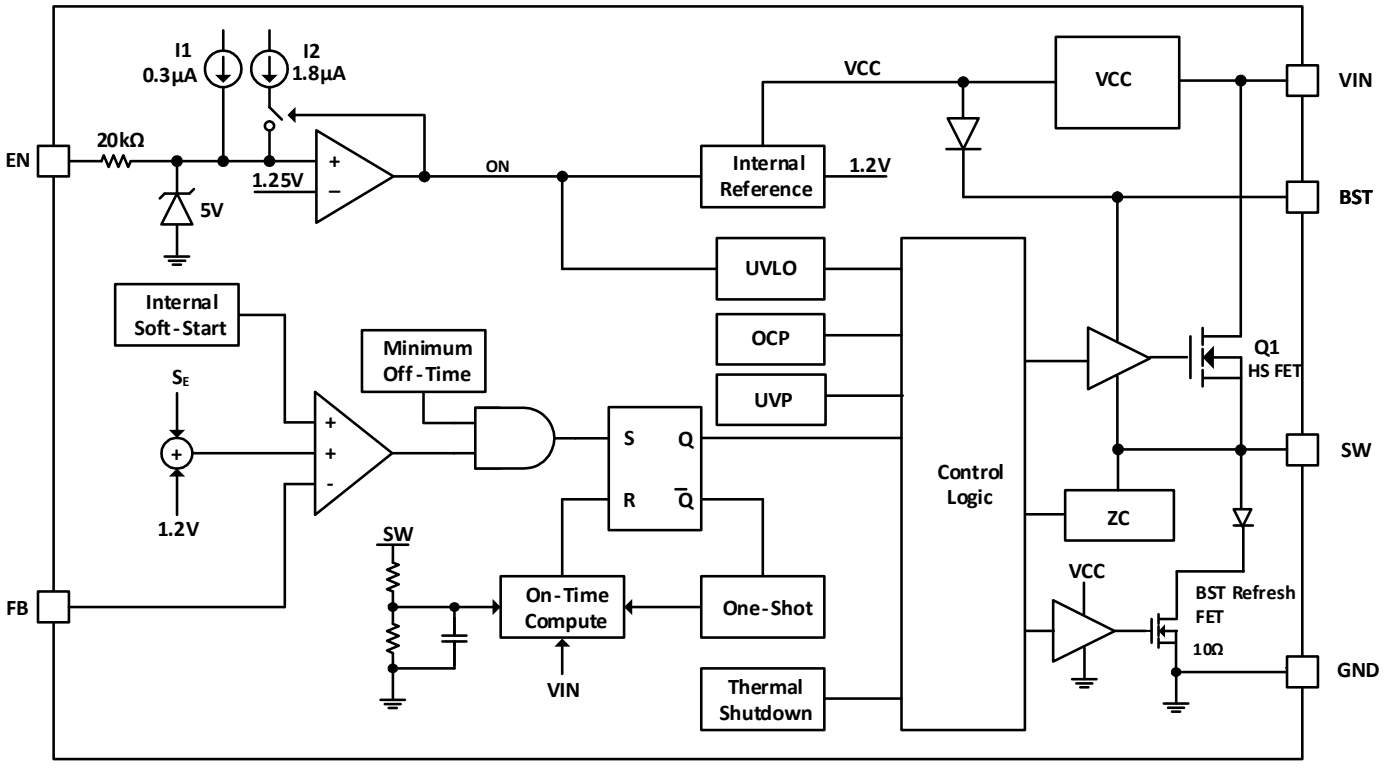


Figure 3. Functional Block Diagram

Absolute Maximum Ratings (@ T_A = +25°C, unless otherwise specified.) (Note 4)

Symbol	Parameter	Rating	Unit
V_{IN}	Supply Voltage	-0.3 to +110	V
V_{SW}	Switch Node Voltage	-1.0 to V_{IN} +0.3 (DC)	V
V_{SW}	Switch Node Voltage	-2.5 to V_{IN} +5 (ns)	V
V_{BST}	Bootstrap Voltage	V_{SW} -0.3 to V_{SW} +6.0	V
V_{EN}	Enable/UVLO Voltage	-0.3V to +6.0	V
V_{FB}	Feedback Voltage	-0.3V to +6.0	V
T_{ST}	Storage Temperature	-65 to +150	°C
T_J	Junction Temperature	+150	°C
T_L	Lead Temperature	+300	°C
ESD Susceptibility (Note 5)			
HBM	Human Body Model	±1000	V
CDM	Charged Device Model	±1500	V

Notes: 4. Stresses greater than the *'Absolute Maximum Ratings'* specified above can cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability can be affected by exposure to absolute maximum rating conditions for extended periods of time.
5. Semiconductor devices are ESD sensitive and can be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

Package Thermal Information (Note 6)

Symbol	Parameter	Rating		Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance	SO-8EP	39	°C/W
$R_{\theta JC(top)}$	Junction-to-Case (Top) Thermal Resistance	SO-8EP	13	°C/W
$R_{\theta JB}$	Junction-to-Board Thermal Resistance	SO-8EP	13	°C/W
ψ_{JT}	Junction-to-Top Characterization Parameter	SO-8EP	4.5	°C/W
ψ_{JB}	Junction-to-Board Characterization Parameter	SO-8EP	12.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-Case (Bottom) Thermal Resistance	SO-8EP	3.5	°C/W

Note: 6. Device mounted on FR-4 substrate, 1" sq. PC board, 2oz copper, with minimum recommended pad layout.

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.) (Note 7)

Symbol	Parameter	Min	Max	Unit
V_{IN}	Supply Voltage	5.5	80	V
T_J	Operating Junction Temperature Range	-40	+150	°C

Note: 7. The device function is not guaranteed outside of the recommended operating conditions.

Electrical Characteristics (T_A = +25°C, V_{IN} = 48V, unless otherwise specified. Min/Max limits apply across the recommended junction temperature range, -40°C to +150°C, and input range from 5.5V to 80V, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
UVLO	VIN Power On Reset Threshold	—	4.7	5.0	5.3	V
	Hysteresis	—	—	440	—	mV
I_{SHDN}	Shutdown Supply Current	V_{EN} = 0V, V_{EN_LDO} = 0V	—	5.6	20	μA
I_Q	Supply Current (Quiescent)	V_{EN} = Open, V_{EN_LDO} = 0V, V_{BIAS} = 0V, V_{BST} - V_{SW} = 5V, Non-Switching	—	140	240	μA
$R_{DS(ON)1}$	High-Side Switch On-Resistance	—	—	500	950	mΩ
I_{LIMIT}	HS Peak Current Limit	VIN > 9V, AP68255Q	3.0	4.0	5.5	A
		VIN > 9V, AP68355Q	4.0	5.0	6.5	A
I_{SW_LKG}	Switch Leakage Current	V_{EN} = 0V, V_{SW} = 0V, V_{IN} = 80V	—	—	5	μA
f_{SW}	Oscillator Frequency	—	260	300	340	kHz
t_{OFF}	Minimum Off-Time	—	—	200	260	ns
D_{MAX}	Maximum Duty Cycle (Note 8)	—	—	93	—	%
V_{FB}	Feedback Voltage	—	1.182	1.200	1.218	V
t_{SS}	Soft-Start Period	—	—	4	—	ms
V_{EN_TH}	EN Rising Threshold	—	—	1.25	—	V
	Hysteresis	—	—	10	—	mV
I_{EN_L}	EN Pull-Up Current	V_{EN} = 0V	—	0.3	—	μA
I_{EN_H}	EN Pull-Up Current	V_{EN} = 1.5V	—	2.1	—	μA
V_{OVP}	% of VFB	Rising Edge	—	120	—	%
		—	—	115	—	%
T_{SHDN}	Thermal Shutdown (Note 8)	—	—	+160	—	°C
T_{HYS}	Thermal Hysteresis (Note 8)	—	—	+20	—	°C

Note: 8. Compliance to the datasheet limits is assured by one or more methods: production test, characterization, and/or design.

Typical Performance Characteristics (AP68255Q/AP68355Q @ T_A = +25°C, VIN = 48V, VOUT = 12V, f_{SW} = 300kHz, BOM = Table 1, unless otherwise specified.)

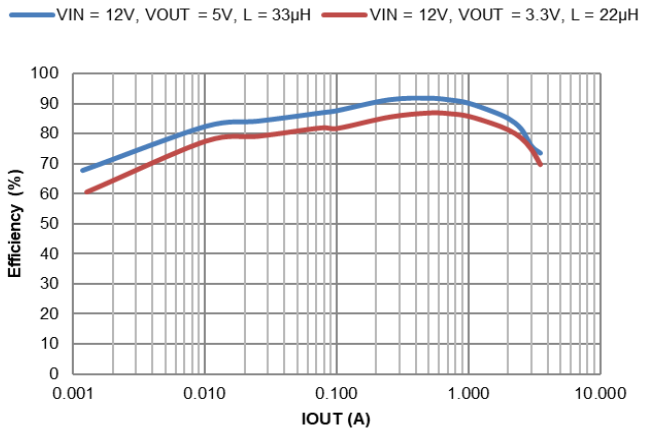


Figure 4. Efficiency vs. Output Current, VIN = 12V

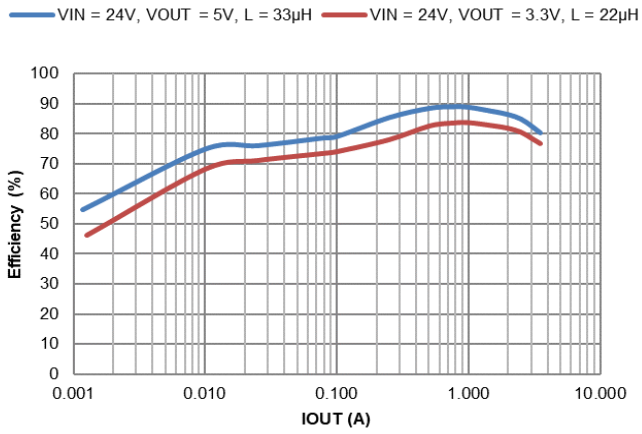


Figure 5. Efficiency vs. Output Current, VIN = 24V

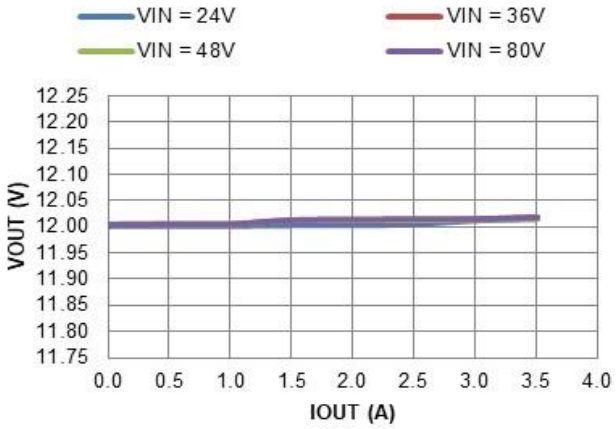


Figure 6. Load Regulation

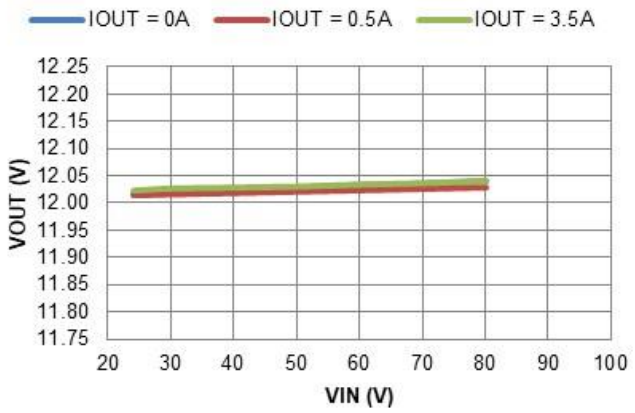


Figure 7. Line Regulation

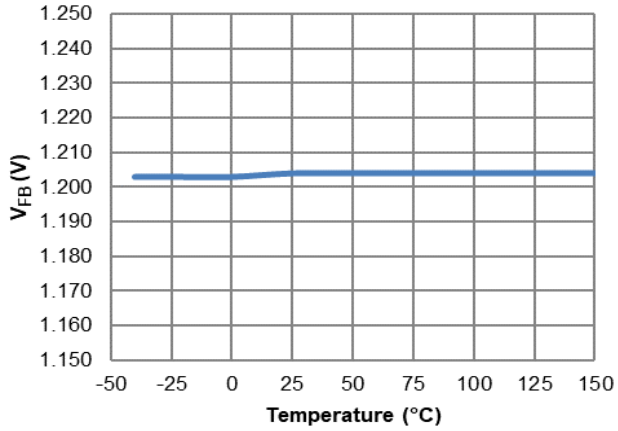


Figure 8. Feedback Voltage vs. Temperature, IOUT = 0A

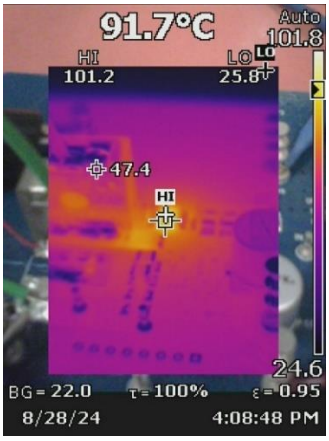


Figure 9. Case Temperature, VIN = 80V, VOUT = 12V, IOUT = 3.5A

Typical Performance Characteristics (AP68255Q/AP68355Q @ T_A = +25°C, VIN = 48V, VOUT = 12V, f_{SW} = 300kHz, BOM = Table 1, unless otherwise specified. continued)

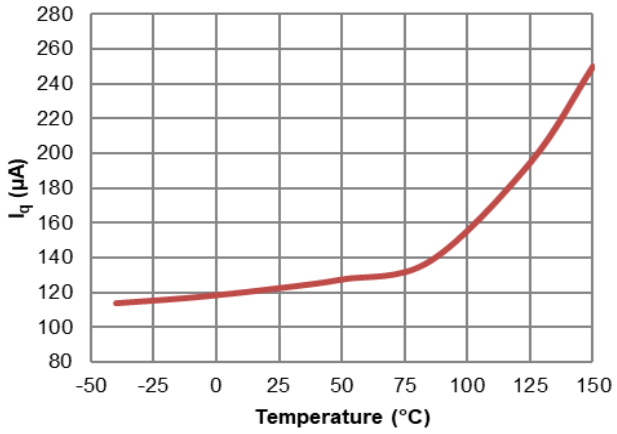


Figure 10. I_Q vs. Temperature, V_{EN} = Float, V_{BST-SW} = 5V

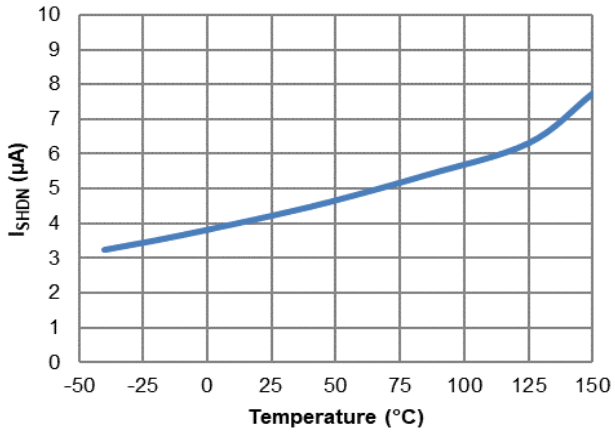


Figure 11. I_{SHDN} vs. Temperature, V_{EN} = 0V, IOUT = 0A

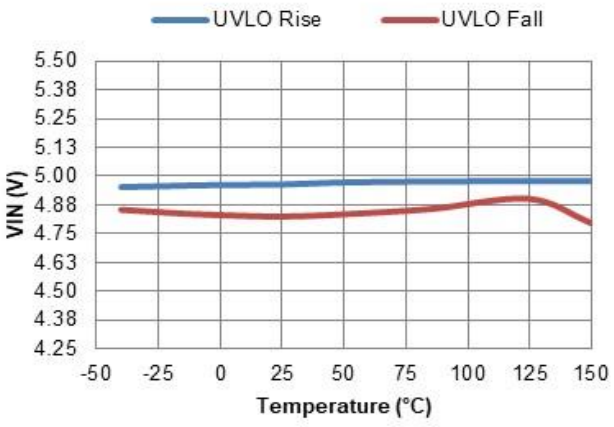


Figure 12. VIN POR and UVLO vs. Temperature

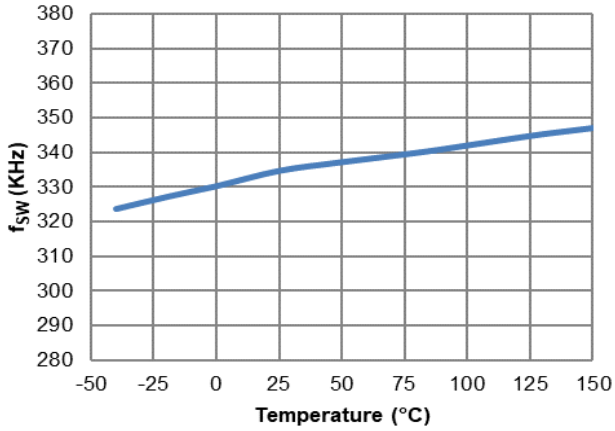


Figure 13. f_{SW} vs. Temperature, IOUT = 3A

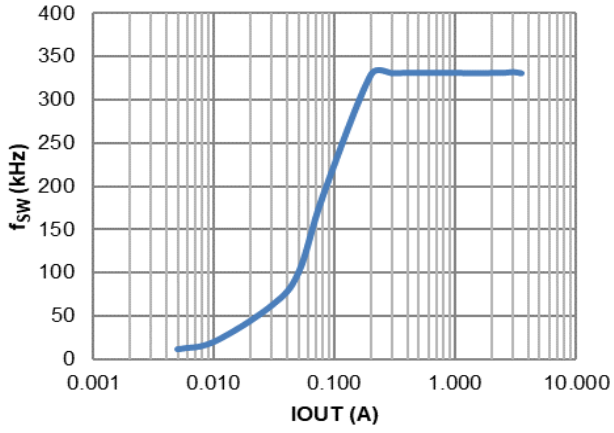


Figure 14. f_{SW} vs. Load

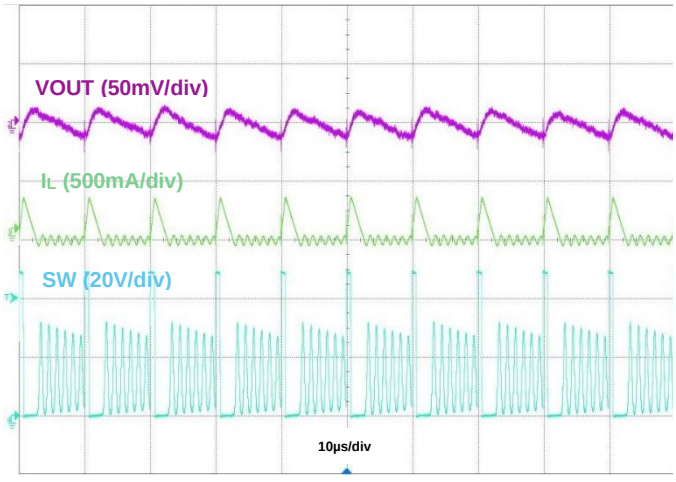


Figure 15. Output Voltage Ripple, IOUT = 50mA

Typical Performance Characteristics (AP68255Q/AP68355Q at T_A = +25°C, VIN = 48V, VOUT = 5V, unless otherwise specified.)

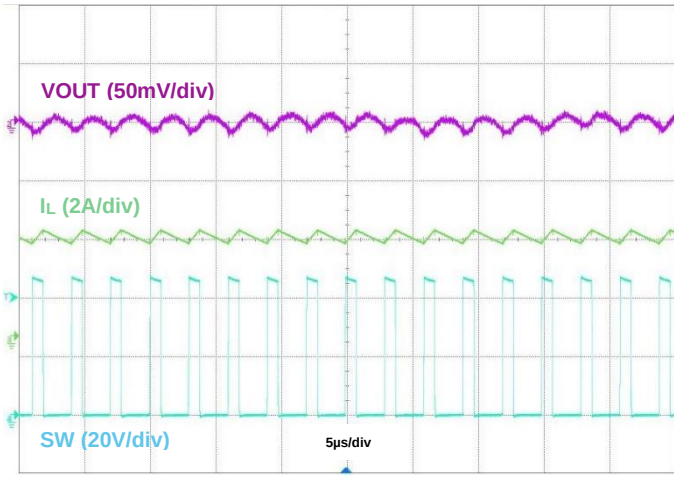


Figure 16. Output Voltage Ripple, IOUT = 3.5A

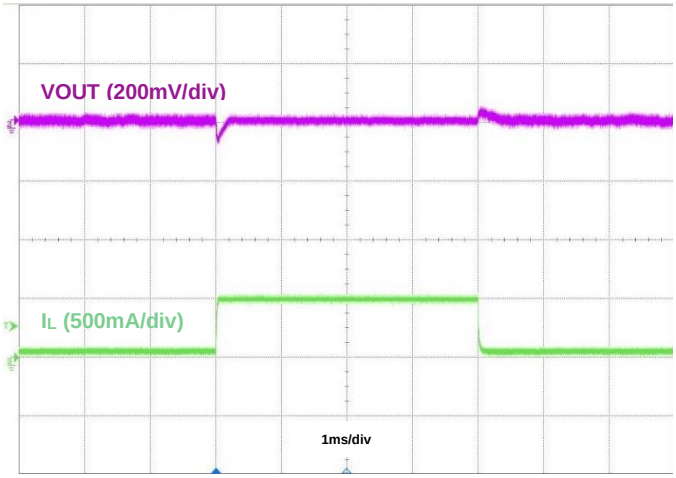


Figure 17. Load Transient, IOUT = 50mA to 500mA to 50mA

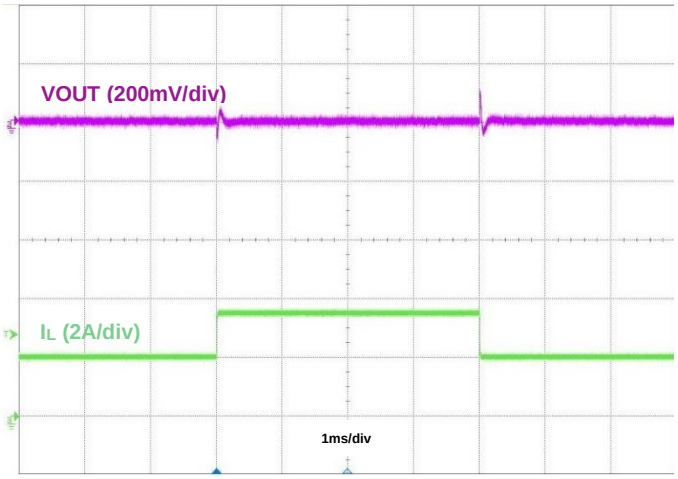


Figure 18. Load Transient, IOUT = 2A to 3.5A to 2A

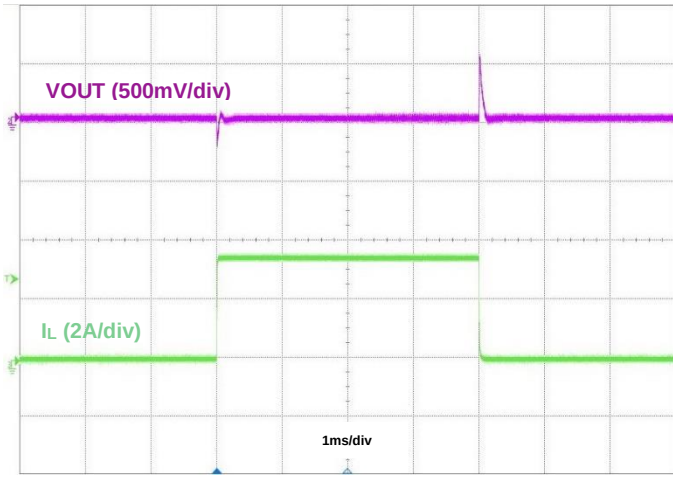


Figure 19. Load Transient, IOUT = 50mA to 3.5A to 50mA

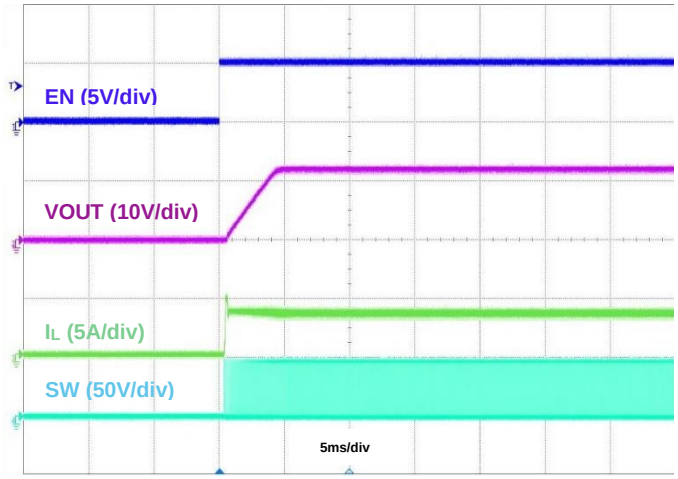


Figure 20. Startup Using EN, IOUT = 3.5A

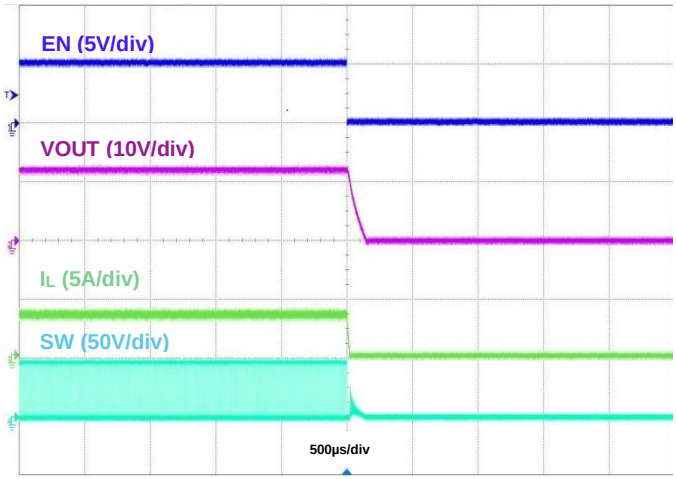


Figure 21. Shutdown Using EN, IOUT = 3.5A

Typical Performance Characteristics (AP68255Q/AP68355Q at T_A = +25°C, VIN = 48V, VOUT = 5V, unless otherwise specified. continued)

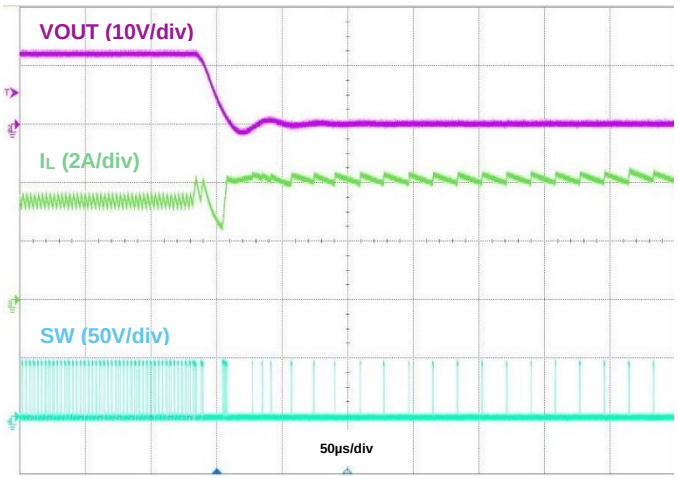


Figure 22. Output Short Protection, IOUT = 3.5A

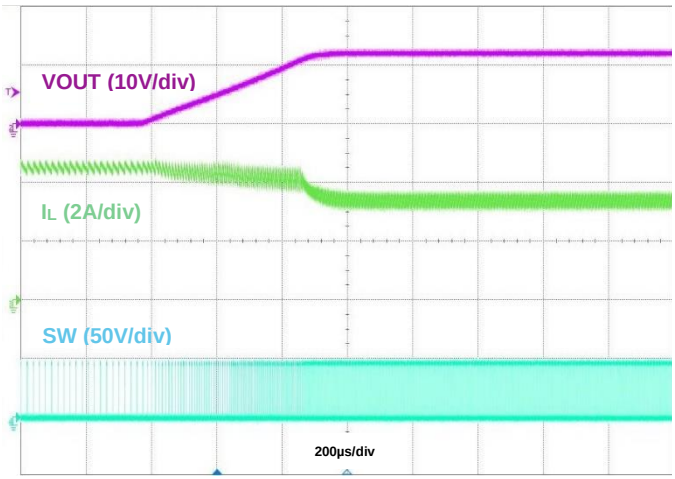


Figure 23. Output Short Recovery, IOUT = 3.5A

Application Information

Pulse Width Modulation (PWM) Operation

The AP68255Q/AP68355Q device is a 5.5V-to-80V input, 2.5A/3.5A output, EMI friendly, fully integrated non-synchronous buck converter. Refer to the block diagram in Figure 3. The device employs constant on-time control to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the one-shot pulse turns on the high-side power MOSFET, Q1, for a fixed on-time, t_{ON}. This one-shot on-pulse timing is calculated by the converter's input voltage and output voltage to maintain a pseudo-fixed frequency over the input voltage range. When Q1 is on, the inductor current rises linearly and the device charges the output capacitor. Q1 turns off after the fixed on-time expires, and the free-wheeling power Diode, D1, conducts. Once the output voltage drops below the output regulation, the one-shot timer is then reset and Q1 turns on again. The on-time is inversely proportional to the input voltage and directly proportional to the output voltage. It is calculated by the following equation:

$$t_{ON} = \frac{VOUT}{VIN \cdot f_{SW}} \quad \text{Eq. 1}$$

Where:

- VIN is the input voltage
- VOUT is the output voltage
- f_{SW} is the switching frequency

The off-time duration is t_{OFF} and starts after the on-time expires. The off-time expires when the feedback voltage decreases below the reference voltage, which then triggers the on-time duration to start again. The minimum off-time is 200ns typically.

Power Diode Selection

The AP68255Q/AP68355Q requires an external free-wheeling diode between SW and GND. The diode must have a reverse voltage rating equal to or greater than VIN maximum, preferably +25% higher. The peak current rating of the diode must be greater than the maximum peak inductor current. Schottky diodes are good choice for the power diode due to their low-forward voltage property, but careful consideration of its reverse leakage current.

Enable and Disable

When disabled, the device shutdown supply current is only 5.6μA. When applying a voltage greater than the EN logic high threshold (typical 1.22V, rising), the AP68255Q/AP68355Q enables all functions, and the device initiates the soft-start phase. An internal 0.3μA pullup current source connected from the internal LDO-regulated VCC to the EN pin guarantees that if EN is left floating, the device is still automatically enabled once the voltage reaches the EN logic high threshold. The AP68255Q/AP68355Q has a built-in 4ms soft-start time to prevent output voltage overshot and inrush current. When the EN voltage falls below its logic low threshold (typical 1.24V, falling), the internal SS voltage discharges to ground and device operation is disabled.

The EN pin can also be used to program the undervoltage lockout thresholds. Undervoltage lockout is implemented to prevent the IC from insufficient input voltages. The AP68255Q/AP68355Q device has a UVLO comparator that monitors the input voltage and the internal bandgap reference. The AP68255Q/AP68355Q is disabled if the input voltage falls below 3.6V. In this UVLO event, both the high-side and low-side power MOSFETs turn off.

Some applications may desire higher VIN UVLO threshold voltages than is provided by the default setup. A 1.8μA hysteresis pullup current source on the EN pin along with an external resistive divider (R3 and R4) configures the VIN UVLO threshold voltages as shown in Figure 24.

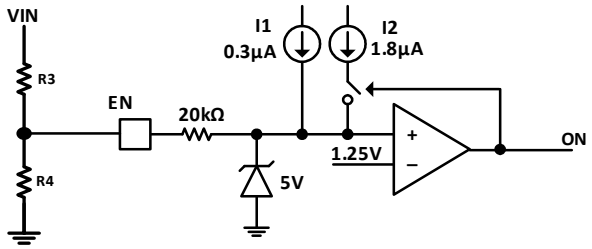


Figure 24. Programming UVLO

Application Information (continued)

The resistive divider resistor values are calculated by:

$$\mathbf{R3} = \frac{\boldsymbol{V_{ON}} - \boldsymbol{V_{OFF}}}{\mathbf{2.1\mu A}} \quad \textbf{Eq. 3}$$

$$\mathbf{R4} = \frac{\mathbf{R3}}{\mathbf{0.8} \cdot \boldsymbol{V_{ON}} - \mathbf{1}} \quad \textbf{Eq. 4}$$

Where:

- V_{ON} is the rising edge VIN voltage to enable the regulator and is greater than 5.3V
- V_{OFF} is the falling edge VIN voltage to disable the regulator and is greater than 4.9V

Current Limit Protection

To reduce the total power dissipation and to protect the application, the AP68255Q/AP68355Q has cycle-by-cycle current limiting implementation. The voltage drops across the internal high-side MOSFET is sense and compared with the internally set current limit threshold. This voltage drop is sensed at about 200ns after the HS turns on. When the peak inductor current exceeds the current limit threshold, current limit protection activates. The device enters frequency foldback to help maintain output overcurrent threshold. This protection mode greatly reduces the power dissipated on the IC and reduces thermal stress to help protect the device. The AP68255Q/AP68355Q will reinitiate soft-start when the overcurrent situation is resolved.

Thermal Shutdown

If the junction temperature of the device reaches the thermal shutdown limit of +160°C, the AP68255Q/AP68355Q shuts down both its high-side and low-side power MOSFETs. When the junction temperature reduces to the required level (+137°C typical), the device initiates a normal power-up cycle with soft-start.

Power Derating Characteristics

To prevent the regulator from exceeding the maximum recommended operating junction temperature, some thermal analysis is required. The regulator's temperature rise is given by:

$$\mathbf{T_{RISE}} = \mathbf{PD} \cdot (\boldsymbol{\theta_{JA}}) \quad \textbf{Eq. 4}$$

Where:

- PD is the power dissipated by the regulator
- θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature

The junction temperature, T_J, is given by:

$$\mathbf{T_J} = \mathbf{T_A} + \mathbf{T_{RISE}} \quad \textbf{Eq. 5}$$

Where:

- T_A is the ambient temperature of the environment

Application Information (continued)

For the SO-8EP package, the θ_{JA} is 39°C/W. The actual junction temperature should not exceed the maximum recommended operating junction temperature of +150°C when considering the thermal design. Figure 25 shows a typical derating curve versus ambient temperature.

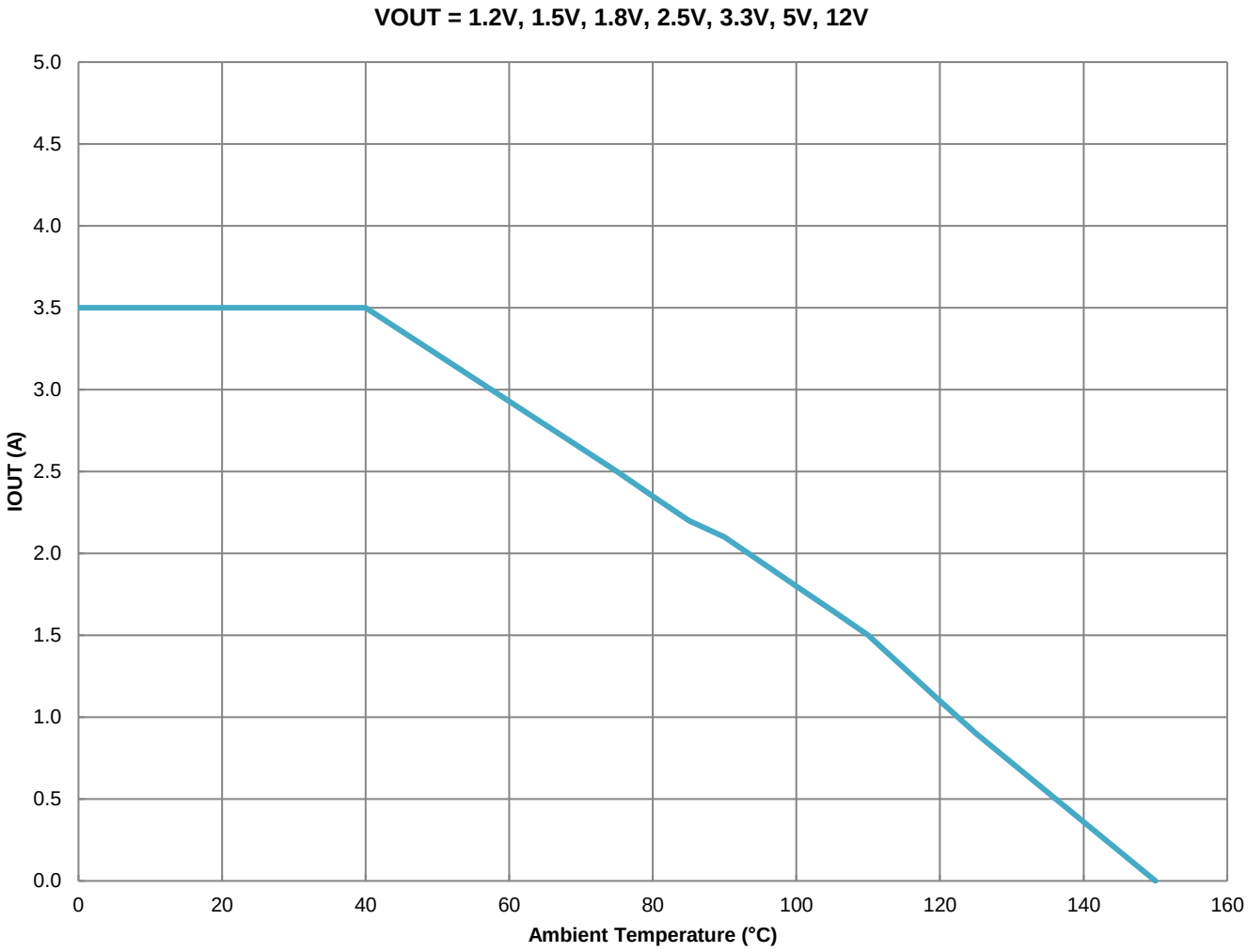


Figure 25. Output Current Derating Curve vs. Ambient Temperature, VIN = 48V

Application Information (continued)

Setting the Output Voltage

The output voltage can be adjusted from 1.2V using an external resistor divider. Table 1 shows a list of resistor selection for common output voltages. An optional C4 of 10pF to 470pF can be used to boost the phase margin and improve stability as well as the transient performance. R2 in Figure 26 can be determined by the following equation:

$$R_2 = \frac{1.2V \cdot R_1}{Vout - 1.2V}$$

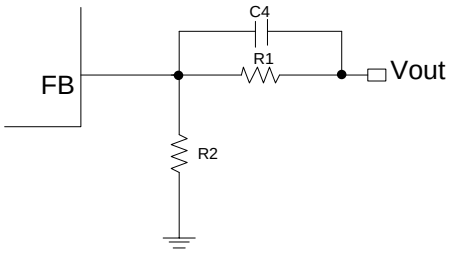


Figure 26. Feedback Divider Network

VOUT (V)	R1 (kΩ)	R2 (kΩ)	C1 (µF)	C2 (µF)	C4 (pF)	L1 (µH)	
						AP68255Q	AP68355Q
1.2	32.4	OPEN	10	2x22	47	5.6	3.3
2.5	32.4	30	10	2x22	47	10	8.2
3.3	52.3	30	10	2x22	47	15	10
5	95.3	30	10	2x22	68	33	15
12	270	30	10	2x22	150	68	33
24	191	10	10	2x22	150	82	47

Table 1. Recommended Component Selection

Additional Ripple Network

The A ripple generation network uses an RC filter consisting of R5 and C5 across SW and VOUT to produce a triangular ramp that is in phase with the inductor current. This triangular ramp is then AC-coupled into the FB node using C4 as shown in Figure 27. This configuration is suited for applications where low output voltage ripple is crucial.

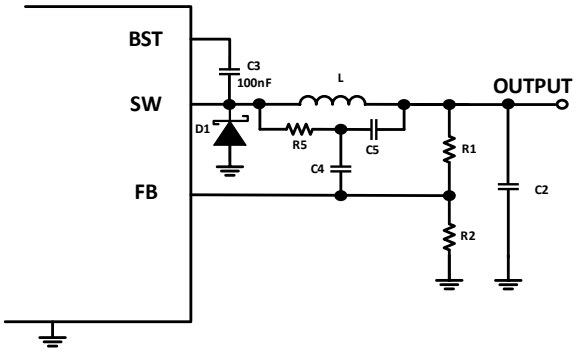


Figure 27. Added Ripple Network

Select C5 between 47nF to 100nF. Then set R5 to match the time constant of the inductor L by the following equation:

$$R_5 = \frac{L}{C_5 \cdot R_{DCR}}$$

Where L is the inductance of the output inductor and the R_{DCR} is the equivalent series resistance of the inductor. R_{DCR} can be found in the typical specification of the inductor. Then set C4 about tenth of C5 or less.

Input Capacitor

The input capacitor reduces the surge current drawn from the input supply and the switching noise from the device. The input capacitor must sustain the ripple current produced during the on time on the upper MOSFET. It must hence have a low ESR to minimize the losses.

The RMS current rating of the input capacitor is a critical parameter that must be higher than the RMS input current. As a rule of thumb, select an input capacitor which has RMs rating that is greater than half of the maximum load current.

Due to large di/dt through the input capacitors, electrolytic or ceramics should be used. If a tantalum must be used, it must be surge protected. Otherwise, capacitor failure could occur. For most applications, a 10µF ceramic capacitor is sufficient and 0.1µF parallel capacitor is also recommended for improving the stability. Higher C1 capacitance is recommended for applications where input line is noisy or got wide transient such as during “hot plug” event.

Application Information (continued)

Inductor

Calculating the inductor value is a critical factor in designing a buck converter. For most designs, the following equation can be used to calculate the inductor value:

$$L = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{V_{IN} \cdot \Delta I_L \cdot f_{SW}}$$

Where ΔI_L is the inductor ripple current and f_{SW} is the buck converter switching frequency.
Choose the inductor ripple current to be 30% to 40% of the maximum load current. The maximum inductor peak current is calculated from:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Peak current determines the required saturation current rating, which influences the size of the inductor. Saturating the inductor decreases the converter efficiency while increasing the temperatures of the inductor and the internal MOSFETs. Hence choosing an inductor with appropriate saturation current rating is important.

An inductor with a DC current rating of at least 25% higher than the maximum load current is recommended for most applications.

For highest efficiency, the inductor's DC resistance should be as low as possible. Use a larger inductance for improved efficiency under light load conditions.

Output Capacitor

The output capacitor keeps the output voltage ripple small, ensures feedback loop stability and reduces the overshoot of the output voltage. The output capacitor is a basic component for the fast response of the power supply. In fact, during load transient, for the first few microseconds it supplies the current to the load. The converter recognizes the load transient and sets the duty cycle to maximum, but the current slope is limited by the inductor value.

ESR of the output capacitor dominates the output voltage ripple. The amount of ripple can be approximate from the equation below:

$$\mathrm{Vout_{capacitor}} = \Delta I_L * (ESR + \frac{1}{8 f_{SW} C_O})$$

An output capacitor with ample capacitance and low ESR is the best option. For most applications, a 22µF ceramic capacitor will be sufficient.

$$C_o = \frac{L(I_{out} + \frac{\Delta I_L}{2})^2}{(\Delta V + V_{out})^2 - {V_{out}}^2}$$

Where ΔV is the maximum output voltage overshoot.

Diode Selection

The AP68255Q/AP68355Q is a non-synchronous buck regulator which means it requires an external diode across SW to GND. The diode must have a reverse voltage rating equal to or greater than VIN. The current rating of the diode should be higher than the peak current of the inductor. The PDS5100Q, SDT5A100P5, and SDT8A120P5 Schottky diodes are good choices.

Bootstrap

The internal driver of the HS FET is equipped with a BST undervoltage detection (UV) circuit. If the voltage difference between BST and SW falls below 2V, the UV detection circuit allows a small 10Ω LS FET on for 400ns to recharge the bootstrap capacitor.

Layout

PCB Layout

1. The AP68255Q/AP68355Q is a high switching frequency converter. Hence, attention must be paid to the switching currents interference in the layout. Switching current from one power device to another can generate voltage transients across the impedances of the interconnecting bond wires and circuit traces. These interconnecting impedances should be minimized by using wide, short, printed circuit traces. The AP68255Q/AP68355Q works at 3.5A load current so heat dissipation is a major concern in the layout of the PCB. 2oz copper for both the top and bottom layers is recommended.
2. Place the input capacitors as closely across VIN and GND as possible.
3. Place the inductor as close to SW as possible.
4. Place the output capacitors as close to GND as possible.
5. Place the feedback components as close to FB as possible.
6. If using four or more layers, use at least the 2nd and 3rd layers as GND to maximize thermal performance.
7. Add as many vias as possible around both the GND pin and under the GND plane for heat dissipation to all the GND layers.
8. Add as many vias as possible around both the VIN pin and under the VIN plane for heat dissipation to all the VIN layers.
9. See Figure 28 for more details.

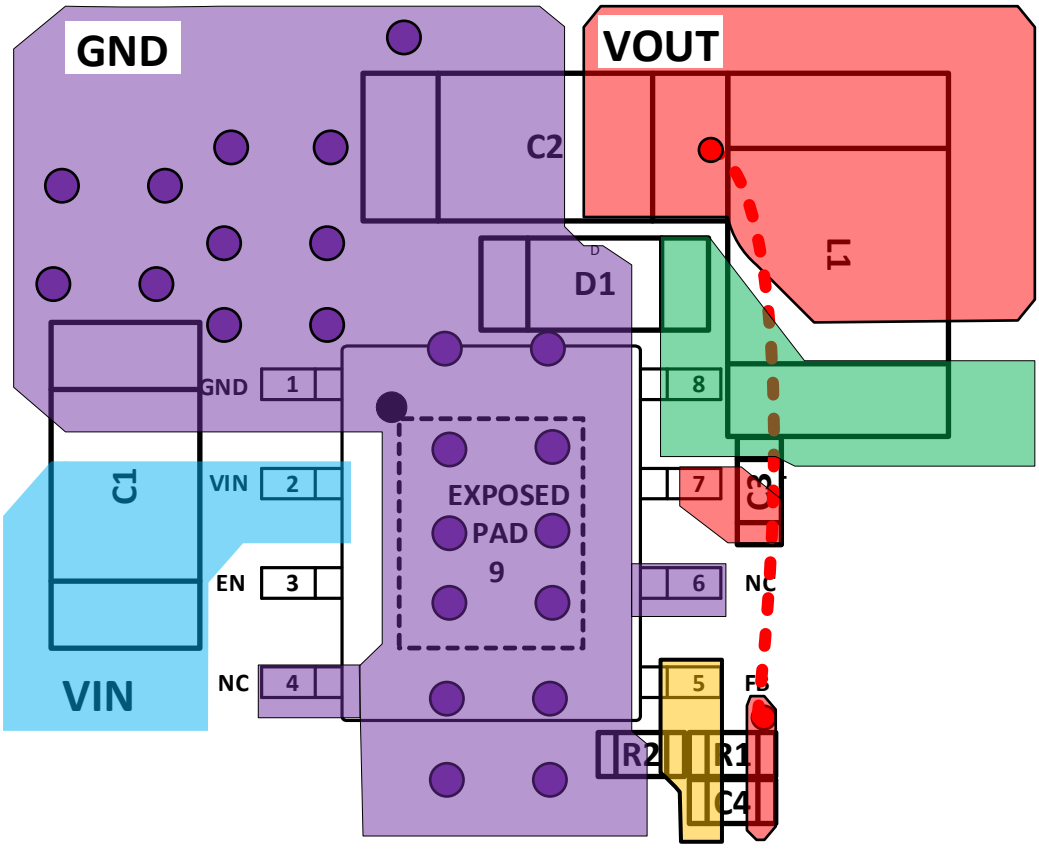
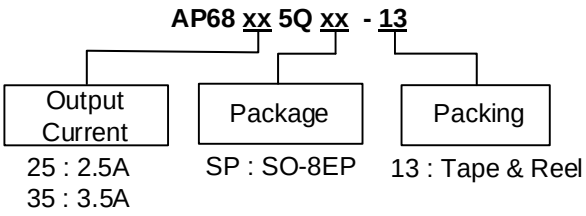


Figure 28. PC Board Layout

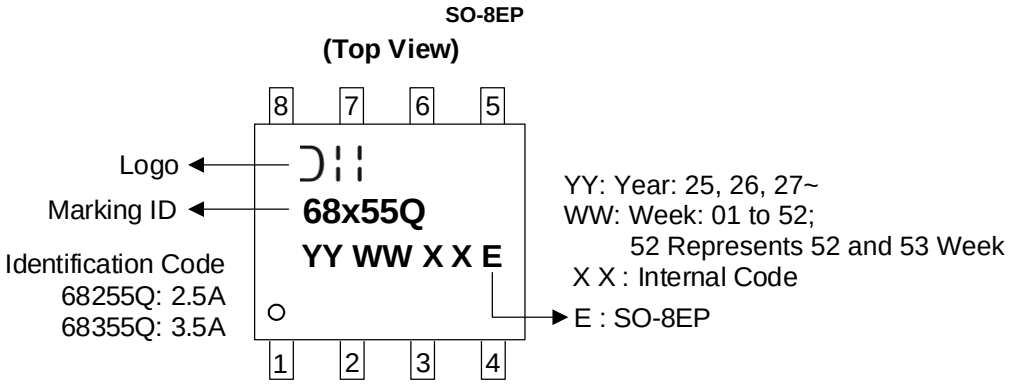
Ordering Information (Note 9)



Orderable Part Number	Output Current	Package Code	Package	Identification Code	Packing	
					Qty.	Carrier
AP68255QSP-13	2.5A	SP	SO-8EP	68255Q	4000	13” Tape and Reel
AP68355QSP-13	3.5A	SP	SO-8EP	68355Q	4000	13” Tape and Reel

Note: 9. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

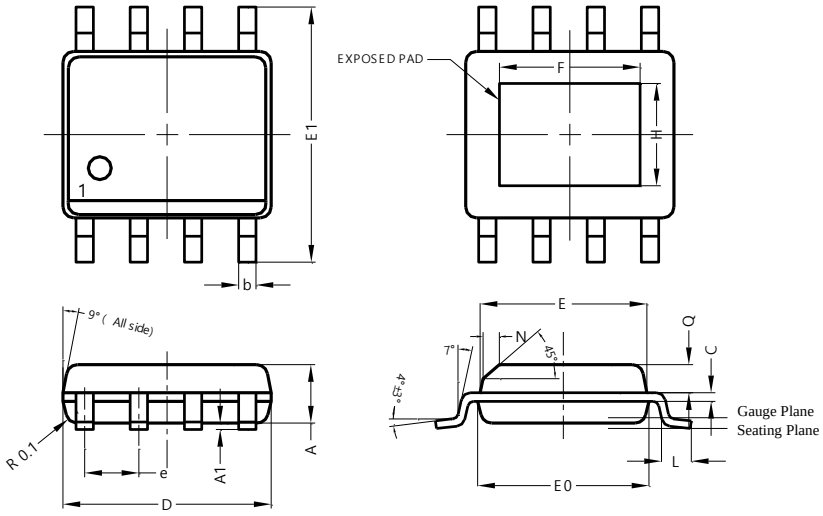
Marking Information



Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

SO-8EP

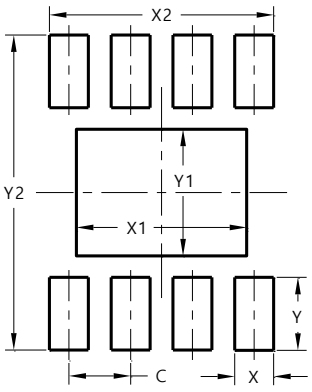


SO-8EP			
Dim	**Min**	**Max**	**Typ**
A	1.40	1.50	1.45
A1	0.00	0.13	-
b	0.30	0.50	0.40
C	0.15	0.25	0.20
D	4.85	4.95	4.90
E	3.80	3.90	3.85
E0	3.85	3.95	3.90
E1	5.90	6.10	6.00
e	-	-	1.27
F	2.75	3.35	3.05
H	2.11	2.71	2.41
L	0.62	0.82	0.72
N	-	-	0.35
Q	0.60	0.70	0.65
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

SO-8EP



Dimensions	Value (in mm)
C	1.270
X	0.802
X1	3.502
X2	4.612
Y	1.505
Y1	2.613
Y2	6.500

Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.081 grams (Approximate)

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