



**Advanced Power
Electronics Corp.**

AP6923GMT-HF

Halogen-Free Product

*DUAL N-CHANNEL MOSFET WITH
SCHOTTKY DIODE*

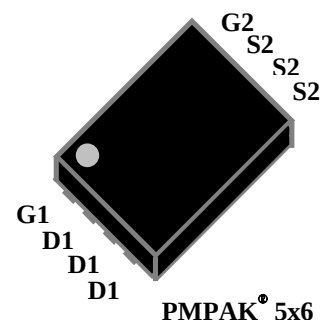
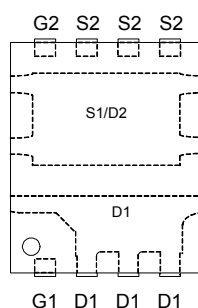
- ▼ Simple Drive Requirement
- ▼ Easy for Synchronous Buck
Converter Application
- ▼ RoHS Compliant & Halogen-Free

Description

Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The control MOSFET (CH-1) and synchronous MOSFET (CH-2) co-package for synchronous buck converters.

	CH-1	BV_{DSS}	30V
		$R_{DS(ON)}$	11m Ω
		I_D	32A
	CH-2	BV_{DSS}	30V
		$R_{DS(ON)}$	7m Ω
		I_D	47A



Absolute Maximum Ratings@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Rating		Units
		CH-1	CH-2	
V_{DS}	Drain-Source Voltage	30	30	V
V_{GS}	Gate-Source Voltage	± 20	± 12	V
$I_D@T_C=25^\circ\text{C}$	Drain Current (Chip Limited) , $V_{GS} @ 10\text{V}$	32	47	A
$I_D@T_A=25^\circ\text{C}$	Drain Current ³ , $V_{GS} @ 10\text{V}$	12.8	18.5	A
$I_D@T_A=70^\circ\text{C}$	Drain Current ³ , $V_{GS} @ 10\text{V}$	10.2	14.8	A
I_{DM}	Pulsed Drain Current ¹	40	60	A
$P_D@T_A=25^\circ\text{C}$	Total Power Dissipation	3.13	3.9	W
T_{STG}	Storage Temperature Range	-55 to 150		$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150		$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Rating		Units
		CH-1	CH-2	
Rthj-c	Maximum Thermal Resistance, Junction-case	6.5	5	$^\circ\text{C}/\text{W}$
Rthj-a	Maximum Thermal Resistance, Junction-ambient ³	40	32	$^\circ\text{C}/\text{W}$
Rthj-a	Maximum Thermal Resistance, Junction-ambient ⁴	70	60	$^\circ\text{C}/\text{W}$



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CH-1 Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	30	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =10A	-	8.7	11	mΩ
		V _{GS} =4.5V, I _D =6A	-	14.3	18.5	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	1	1.6	3	V
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =10A	-	20	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =24V, V _{GS} =0V	-	-	10	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Q _g	Total Gate Charge	I _D =10A	-	10	16	nC
Q _{gs}	Gate-Source Charge	V _{DS} =15V	-	3	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =4.5V	-	4	-	nC
t _{d(on)}	Turn-on Delay Time	V _{DS} =15V	-	8	-	ns
t _r	Rise Time	I _D =1A	-	4.5	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =3.3Ω	-	21	-	ns
t _f	Fall Time	V _{GS} =10V	-	4	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	1150	1840	pF
C _{oss}	Output Capacitance	V _{DS} =15V	-	135	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	100	-	pF
R _g	Gate Resistance	f=1.0MHz	-	1.2	2.4	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ²	I _S =10A, V _{GS} =0V	-	-	1.2	V
t _{rr}	Reverse Recovery Time	I _S =10A, V _{GS} =0V,	-	21	-	ns
Q _{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	14	-	nC

**CH-2 Electrical Characteristics@T_j=25°C(unless otherwise specified)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	30	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =15A	-	5.6	7	mΩ
		V _{GS} =4.5V, I _D =10A	-	8.7	11.5	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	1	1.4	3	V
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =15A	-	28	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =24V, V _{GS} =0V	-	-	500	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±12V, V _{DS} =0V	-	-	±100	nA
Q _g	Total Gate Charge	I _D =15A	-	17	27.2	nC
Q _{gs}	Gate-Source Charge	V _{DS} =15V	-	4	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =4.5V	-	8	-	nC
t _{d(on)}	Turn-on Delay Time	V _{DS} =15V	-	10	-	ns
t _r	Rise Time	I _D =1A	-	6	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =3.3Ω	-	32	-	ns
t _f	Fall Time	V _{GS} =10V	-	8	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	2000	3200	pF
C _{oss}	Output Capacitance	V _{DS} =15V	-	250	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	180	-	pF
R _g	Gate Resistance	f=1.0MHz	-	1	2	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Diode+Schottky Forward On Voltage ²	I _S =1A, V _{GS} =0V	-	0.48	0.5	V
t _{rr}	Body Diode+Schottky Reverse Recovery Time	I _S =10A, V _{GS} =0V, dI/dt=100A/μs	-	25	-	ns
Q _{rr}	Body Diode+Schottky Reverse Recovery Charge		-	15	-	nC

Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test
- 3.Surface mounted on 1 in² copper pad of FR4 board, t ≤10sec.
- 4.Surface mounted on 1 in² copper pad of FR4 board, on steady-state.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

APEC RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.



Channel-1

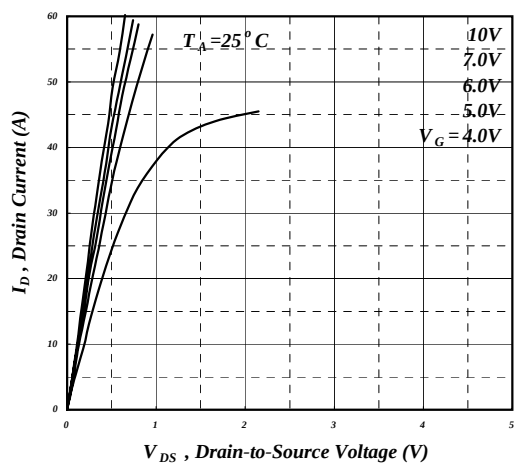


Fig 1. Typical Output Characteristics

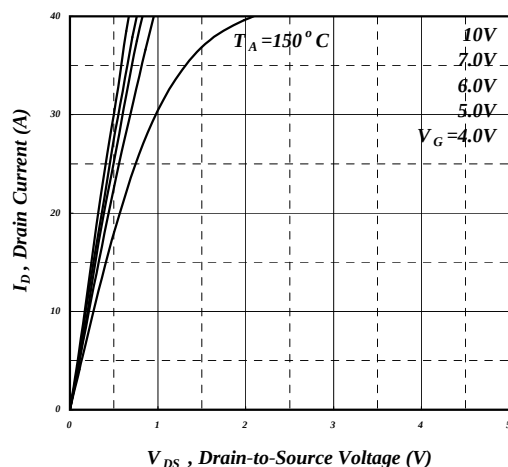


Fig 2. Typical Output Characteristics

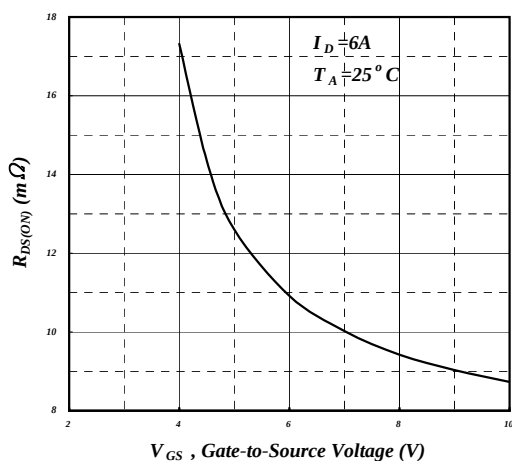


Fig 3. On-Resistance v.s. Gate Voltage

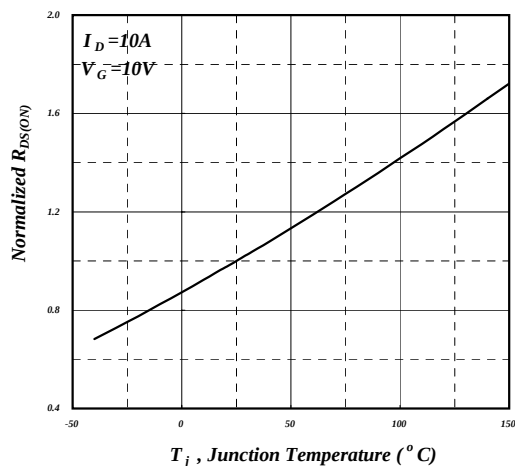


Fig 4. Normalized On-Resistance
v.s. Junction Temperature

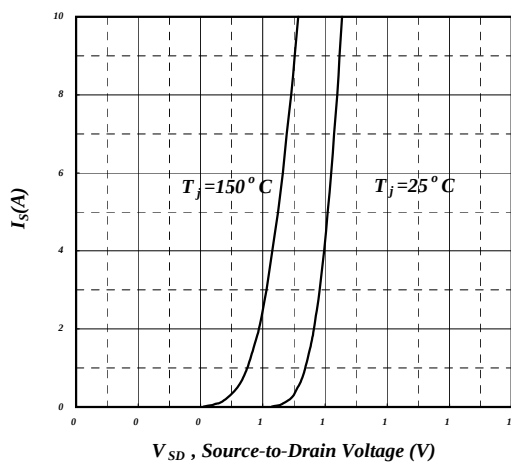


Fig 5. Forward Characteristic of
Reverse Diode

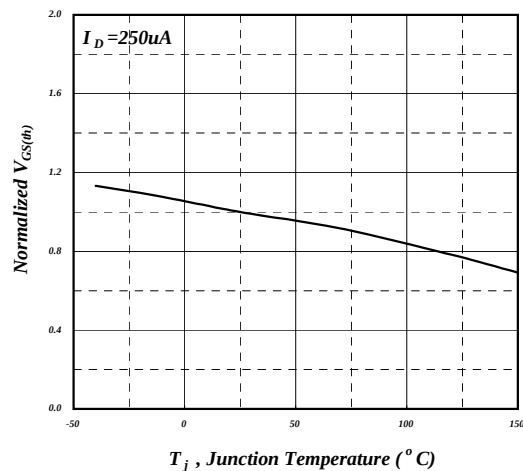


Fig 6. Gate Threshold Voltage v.s.
Junction Temperature



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Channel-1

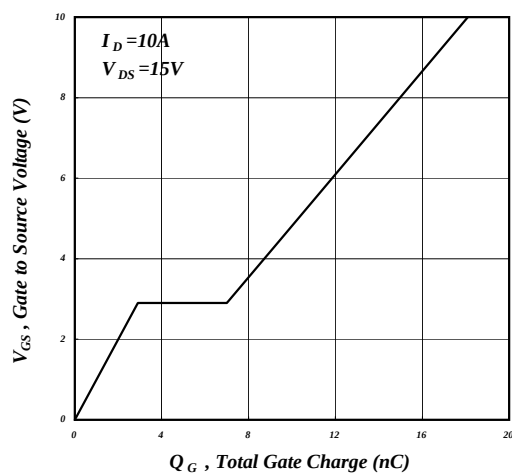


Fig 7. Gate Charge Characteristics

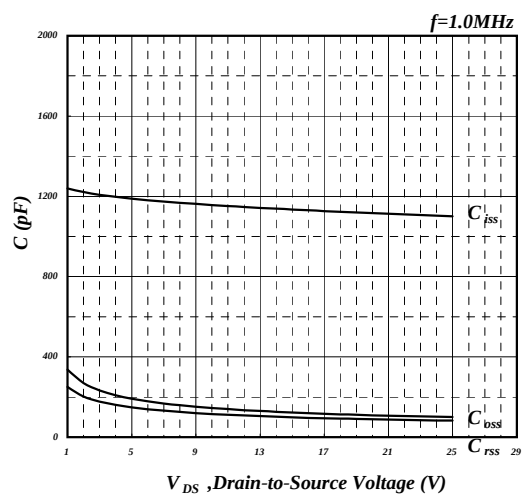


Fig 8. Typical Capacitance Characteristics

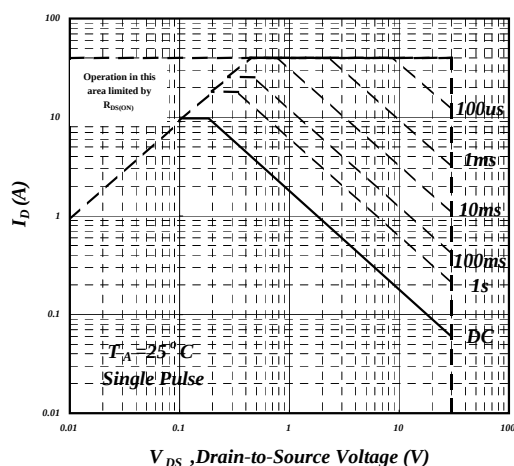


Fig 9. Maximum Safe Operating Area

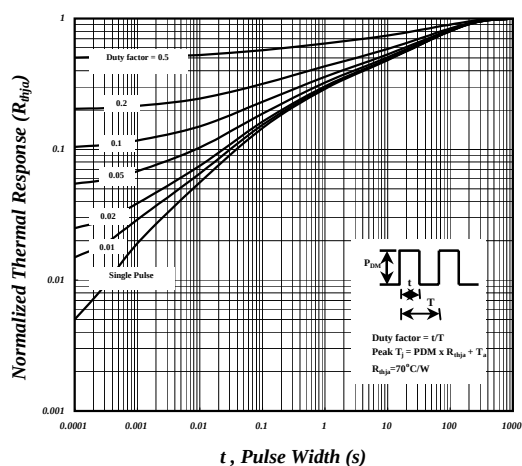


Fig 10. Effective Transient Thermal Impedance

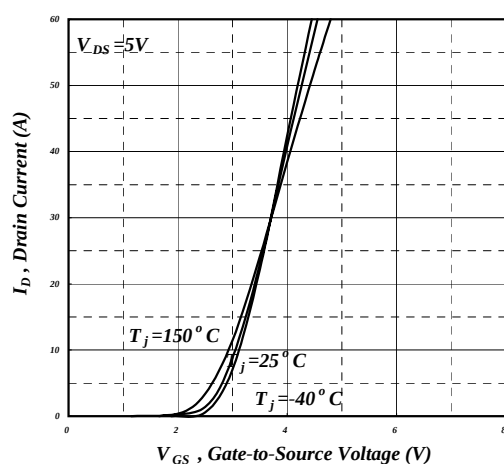


Fig 11. Transfer Characteristics

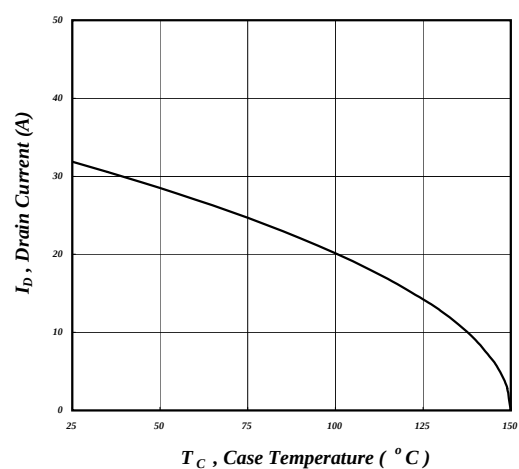


Fig 12. Drain Current v.s. Case Temperature



Channel-2

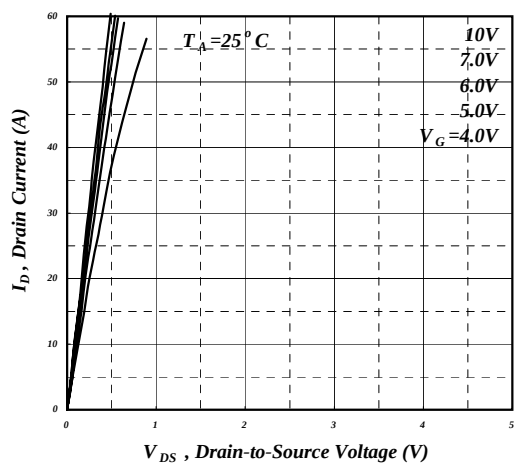


Fig 1. Typical Output Characteristics

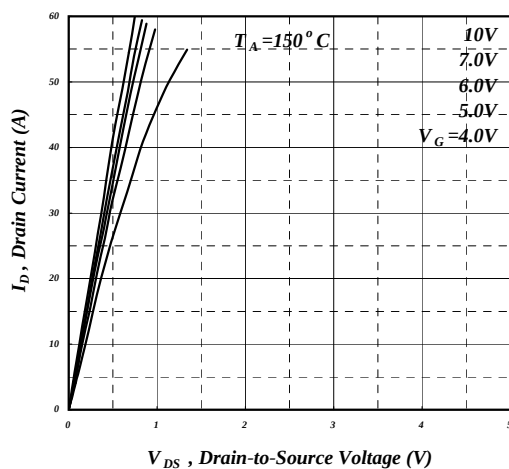


Fig 2. Typical Output Characteristics

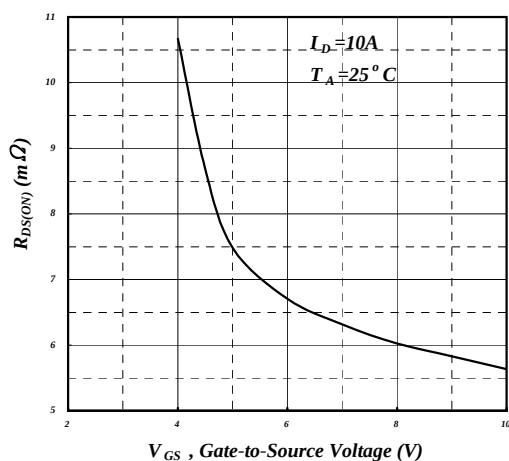


Fig 3. On-Resistance v.s. Gate Voltage

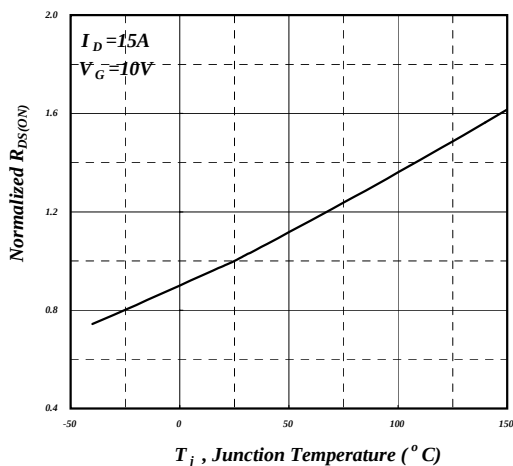


Fig 4. Normalized On-Resistance
v.s. Junction Temperature

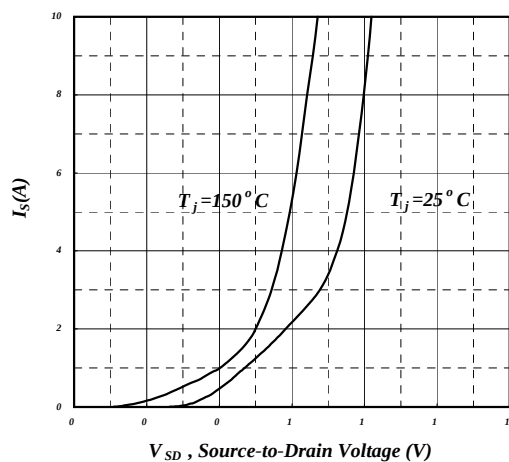


Fig 5. Forward Characteristic of
Reverse Diode

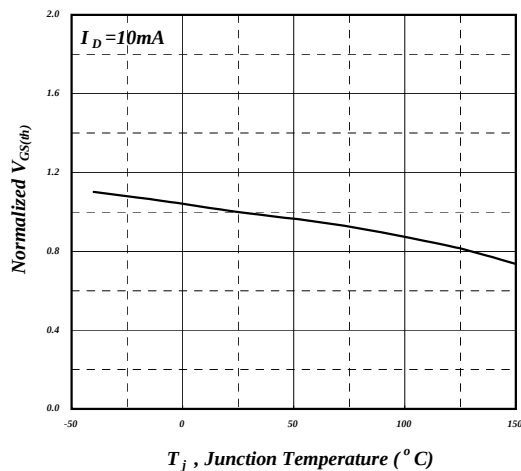


Fig 6. Gate Threshold Voltage v.s.
Junction Temperature



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Channel-2

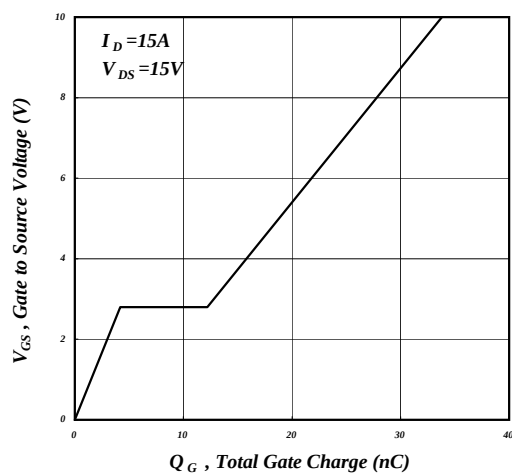


Fig 7. Gate Charge Characteristics

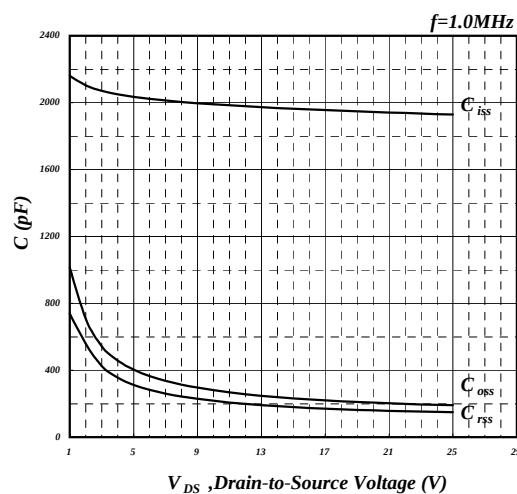


Fig 8. Typical Capacitance Characteristics

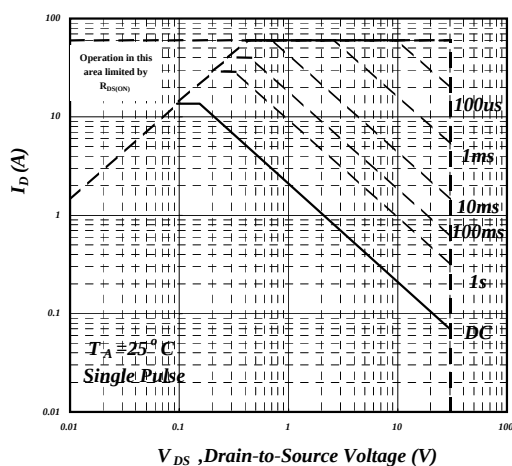


Fig 9. Maximum Safe Operating Area

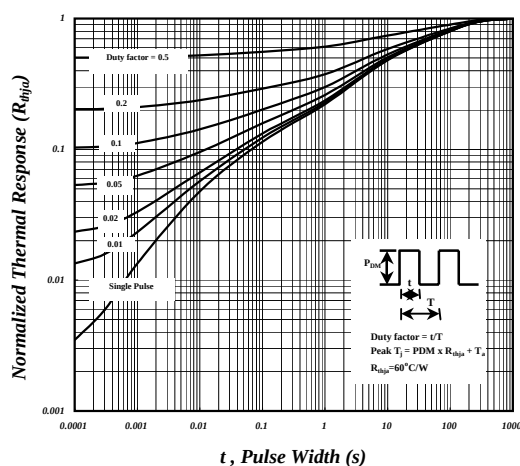


Fig 10. Effective Transient Thermal Impedance

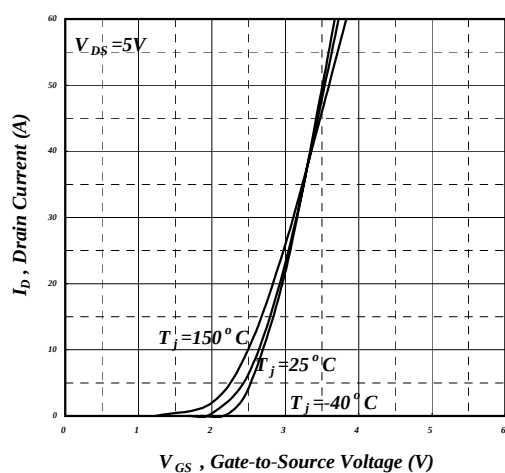


Fig 11. Transfer Characteristics

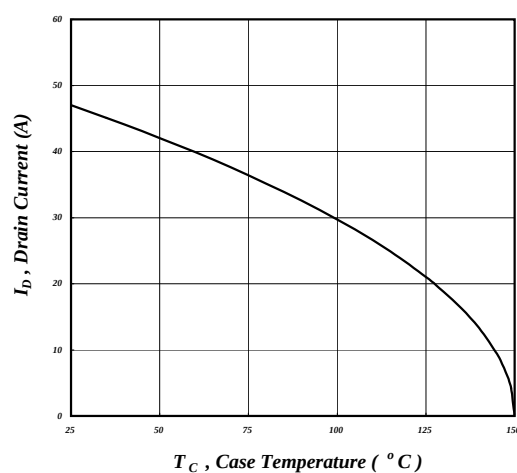


Fig 12. Drain Current v.s. Case Temperature



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MARKING INFORMATION

