

60V N+P-Channel Enhancement Mode MOSFET

Description

The AP6G06S uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = 60V$ $I_D = 6.5A$

$R_{DS(ON)} < 55m\Omega$ @ $V_{GS}=10V$ (Type: 40m Ω)

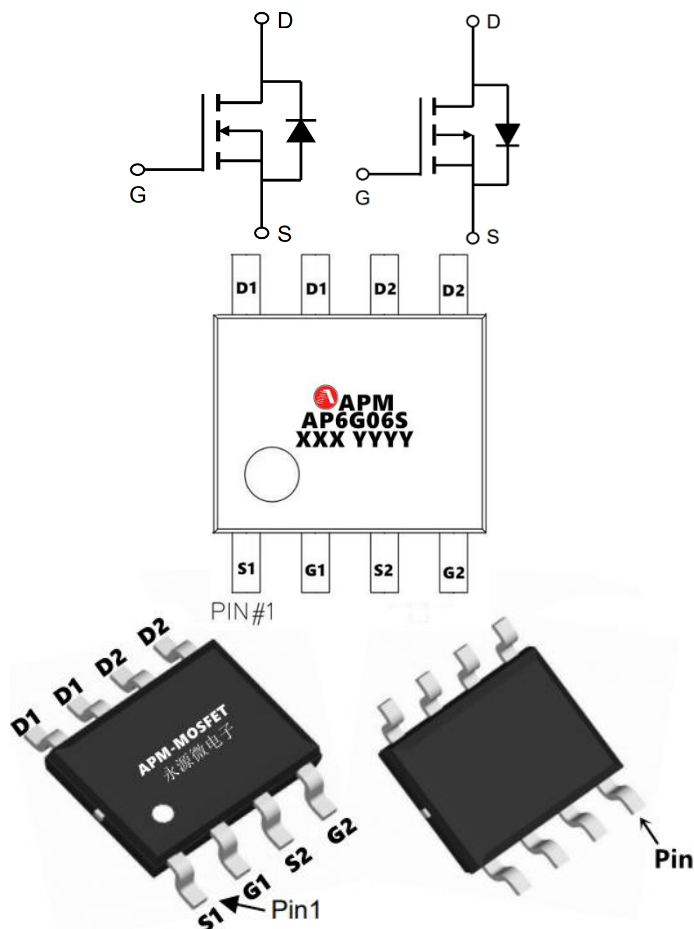
$V_{DS} = -60V$ $I_D = -6.2A$

$R_{DS(ON)} < 90m\Omega$ @ $V_{GS}=-10V$ (Type: 70m Ω)

Application

Boost driver

Brushless motor



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP6G06S	SOP-8L	AP6G06S XXX YYYY	3000

Absolute Maximum Ratings ($T_C=25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Rating		Units
		N-Channel	P-Channel	
V_{DS}	Drain-Source Voltage	60	-60	V
V_{GS}	Gate-Source Voltage	± 20	± 20	V
$I_{D@T_A=25^{\circ}C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	6.5	-6.2	A
$I_{D@T_A=70^{\circ}C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	3.1	-2.8	A
IDM	Pulsed Drain Current ²	27	25.5	A
EAS	Single Pulse Avalanche Energy ³	21	21.8	mJ
$P_{D@T_A=25^{\circ}C}$	Total Power Dissipation ⁴	1.5	1.3	W
TSTG	Storage Temperature Range	-55 to 150		$^{\circ}C$
T_J	Operating Junction Temperature Range	-55 to 150		$^{\circ}C$

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N-Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V(BR)DSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	60	65	-	V
IDSS	Zero Gate Voltage Drain Current	V _{DS} =60V, V _{GS} =0V,	-	-	1.0	μA
IGSS	Gate to Body Leakage Current	V _{DS} =0V, V _{GS} =±20V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.2	1.6	2.5	V
RDS(on)	Static Drain-Source on-Resistance	V _{GS} =10V, I _D =15A	-	40	50	mΩ
		V _{GS} =4.5V, I _D =10A	-	45	55	mΩ
Ciss	Input Capacitance	V _{DS} =25V, V _{GS} =0V, f=1.0MHz	-	825	-	pF
Coss	Output Capacitance		-	49	-	pF
Crss	Reverse Transfer Capacitance		-	41	-	pF
Q _g	Total Gate Charge	V _{DS} =30V, I _D =4.5A, V _{GS} =10V	-	14	-	nC
Q _{gs}	Gate-Source Charge		-	2.9	-	nC
Q _{gd}	Gate-Drain("Miller") Charge		-	5.2	-	nC
td(on)	Turn-on Delay Time	V _{DS} =30V, I _D =2A, R _L =6.7Ω, R _G =3Ω, V _{GS} =10V	-	5	-	ns
tr	Turn-on Rise Time		-	2.6	-	ns
td(off)	Turn-off Delay Time		-	16.1	-	ns
tf	Turn-off Fall Time		-	2.3	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	6.5	A
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	20	A
VSD	Drain to Source Diode Forward Voltage	V _{GS} =0V, I _S =15A	-	-	1.2	V

Note :

- 1、The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
- 2、The data tested by pulsed , pulse width .The EAS data shows Max. rating .
- 3、The test cond ≅ 300us duty cycle ≅ 2%, duty cycle ition is T_J =25°C, VDD =48V, VG =10V, RG =25Ω, L=0.1mH, IAS =9.8A
- 4、The power dissipation is limited by 175°C junction temperature
- 5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

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P-Electrical Characteristics (T_J =25 °C, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDSS	Drain-Source Breakdown Voltage	VGS=0V, ID=-250μA	-60	-	-	V
IGSS	Gate-body Leakage current	VDS=0V, VGS=±20V	-	-	±100	nA
IDSS	Zero Gate Voltage Drain Current T _J = 25°C	VDS=-60V, VGS=0V	-	-	-1	μA
	Zero Gate Voltage Drain Current T _J = 25°C		-	-	-100	
VGS(th)	Gate-Threshold Voltage	VDS=VGS, ID=-250μA	-1	-1.6	-2.5	V
RDS(on)	Drain-Source On-Resistance ⁴	VGS=-10V, ID=-10A	-	70	85	mΩ
		VGS=-4.5V, ID=-5A	-	81	95	
gfs	Forward Transconductance ⁴	VDS=-10V, ID=-10A	-	30	-	S
Ciss	Input Capacitance	VDS=-30V, VGS=0V, f = 1MHz	-	1022	-	pF
Coss	Output Capacitance		-	47	-	
Crss	Reverse Transfer Capacitance		-	39	-	
Rg	Gate Resistance	f=1MHz	-	11	-	Ω
Qg	Total Gate Charge	VGS=-10V, VDS=-30V, ID=-10A	-	17	-	nC
Qgs	Gate-Source Charge		-	2.9	-	
Qgd	Gate-Drain Charge		-	7.4	-	
td(on)	Turn-On Delay Time	VGS=-10V, VDD=-30V, RG=3Ω, ID=-10A	-	8.5	-	ns
tr	Rise Time		-	19.9	-	
td(off)	Turn-Off Delay Time		-	44	-	
tf	Fall Time		-	12.2	-	
VSD	Diode Forward Voltage ⁴	IS=-1A, VGS=0V	-	-	-1.2	V
IS	Continuous Source Current TC= 25°C	-	-	-	-6.2	A

Note :

- 1、The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.
- 2、The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3、The power dissipation is limited by 150°C junction temperature
- 4、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

N-Typical Characteristics

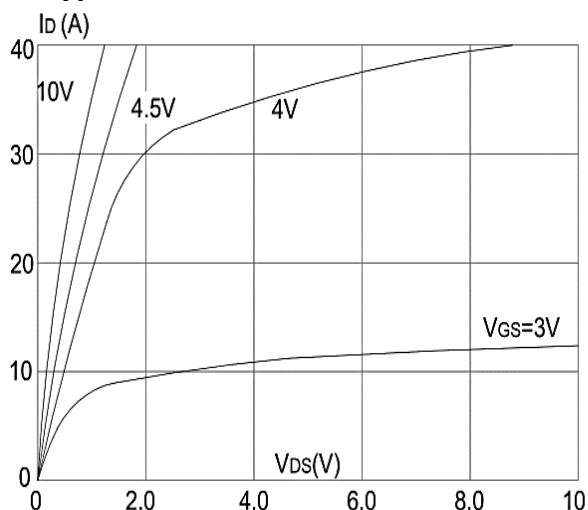


Figure1: Output Characteristics

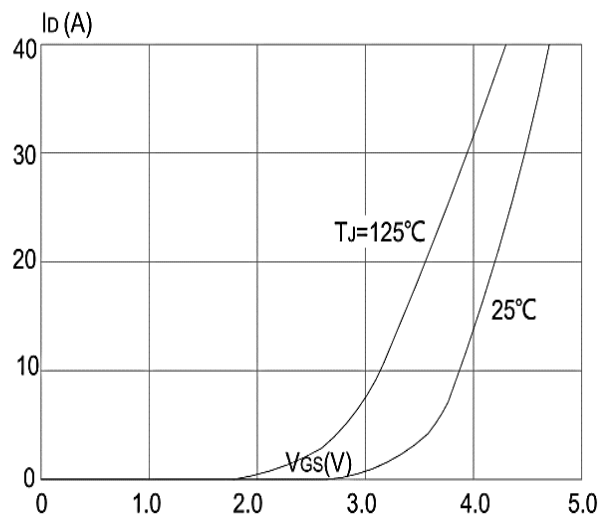


Figure 2: Typical Transfer Characteristics

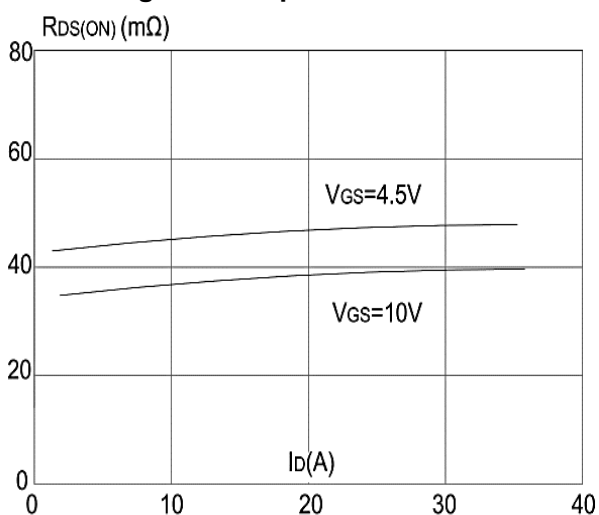


Figure 3: On-resistance vs. Drain Current

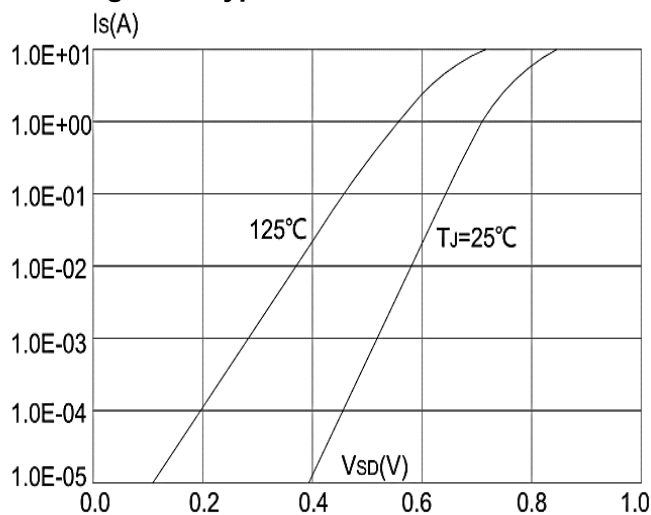


Figure 4: Body Diode Characteristics

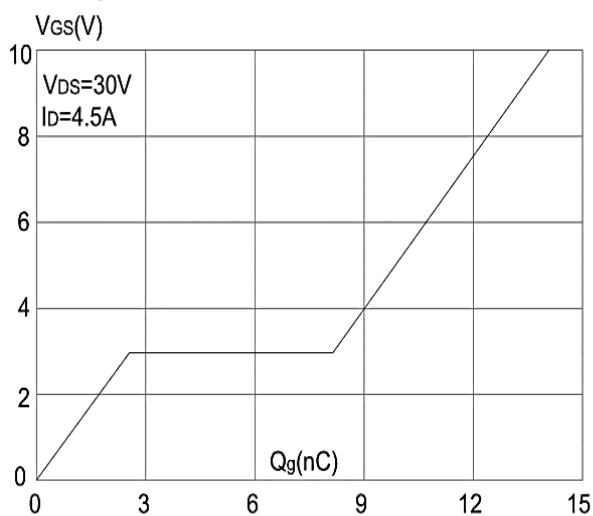


Figure 5: Gate Charge Characteristics

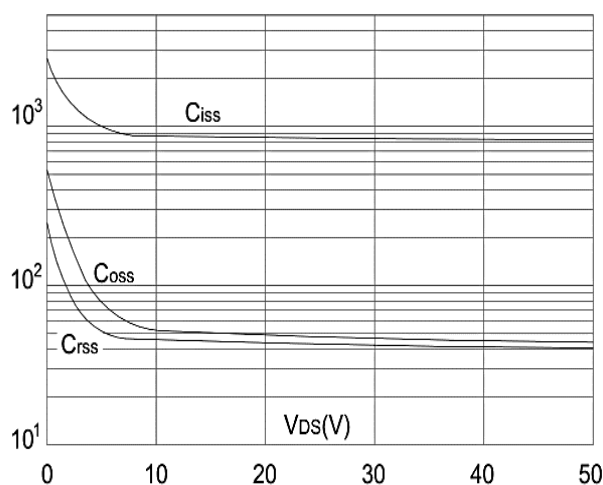


Figure 6: Capacitance Characteristics

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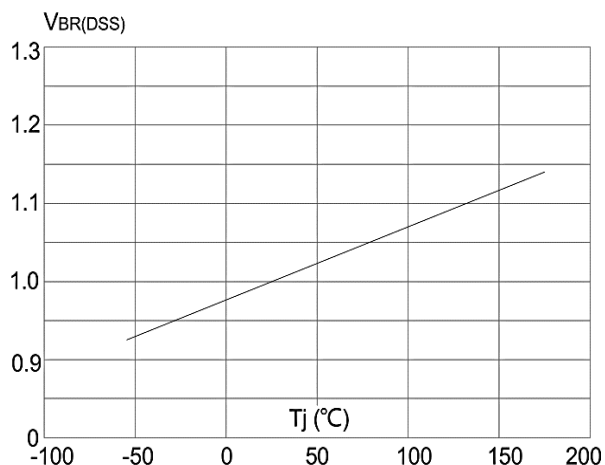


Figure 7: Normalized Breakdown Voltage vs Junction Temperature

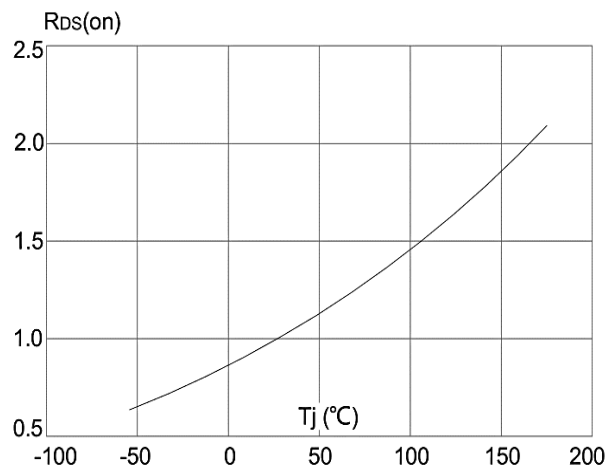


Figure 8: Normalized on Resistance vs. Junction Temperature

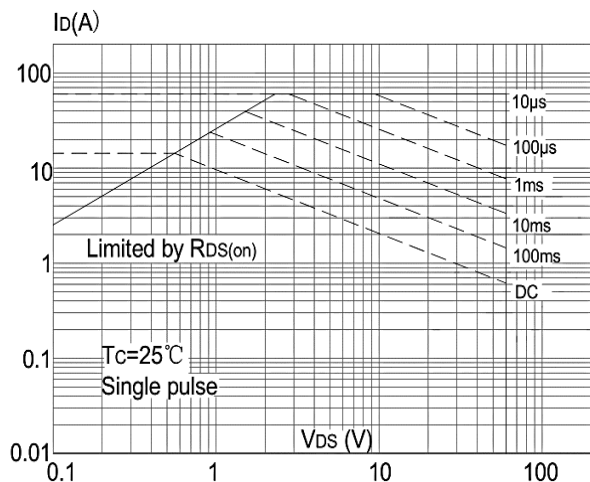


Figure 9: Maximum Safe Operating Area vs. Ambient Temperature

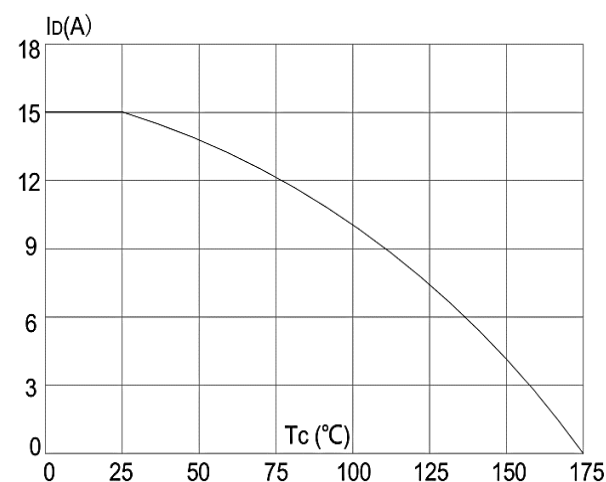


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

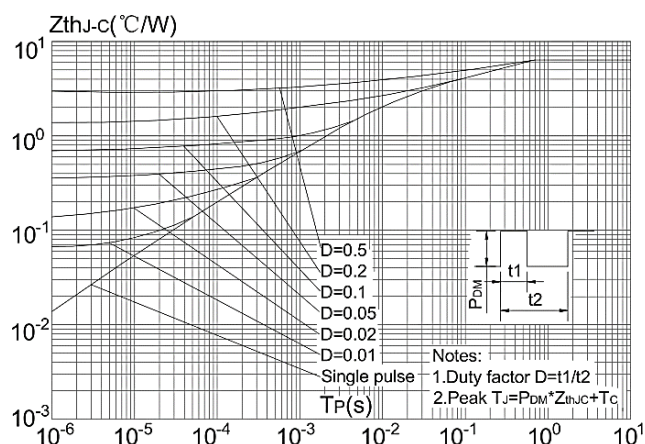


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambien

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P-Channel Typical Characteristic

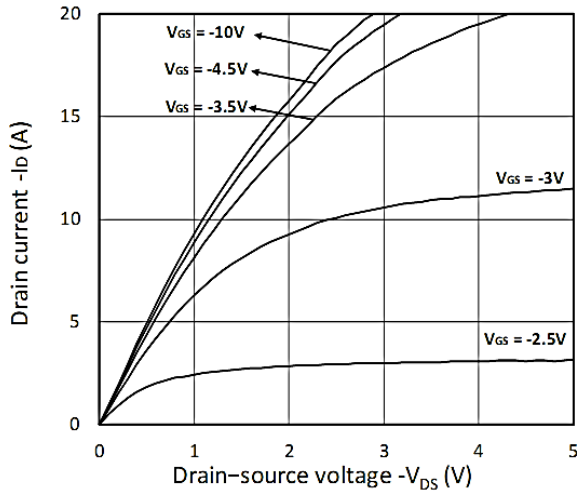


Figure 1. Output Characteristics

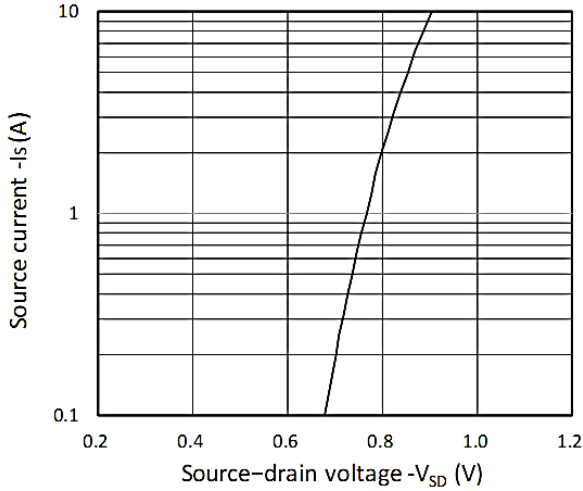


Figure 3. Forward Characteristics of Reverse

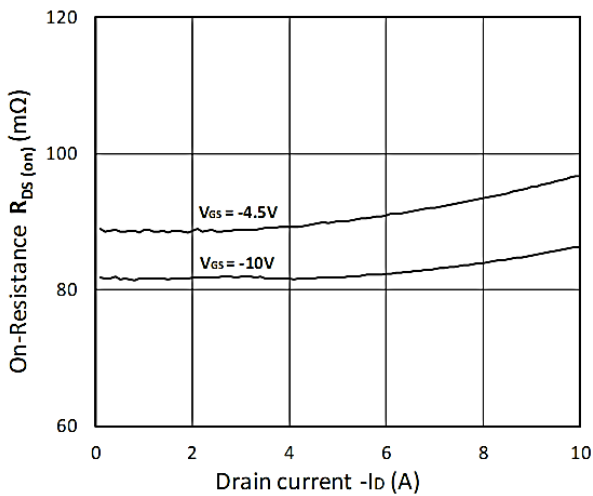


Figure 5. $R_{DS(ON)}$ vs. I_D

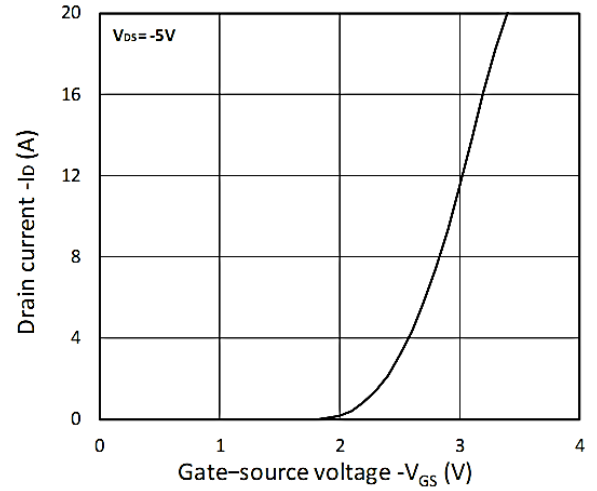


Figure 2. Transfer Characteristics

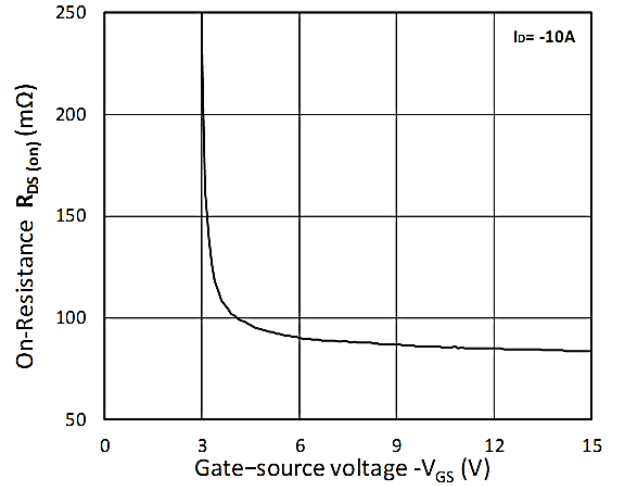


Figure 4. $R_{DS(ON)}$ vs. V_{GS}

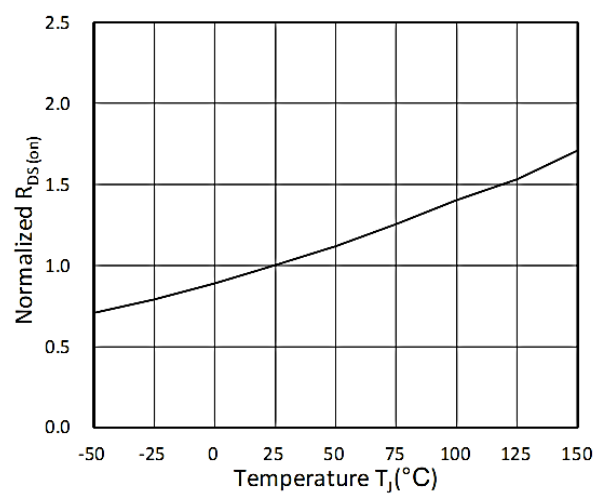


Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

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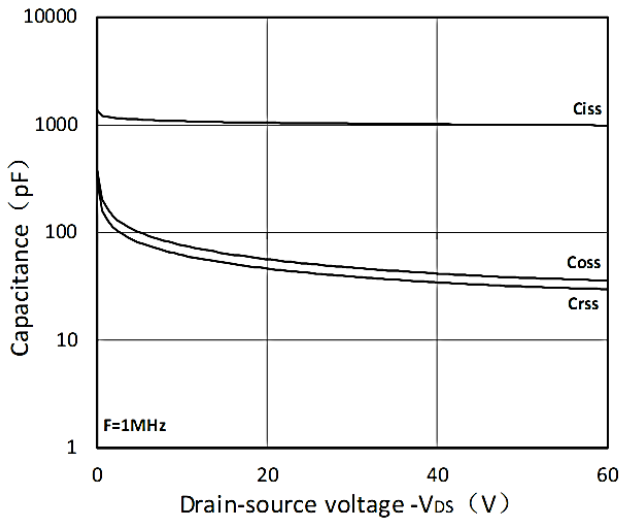


Figure 7. Capacitance Characteristics

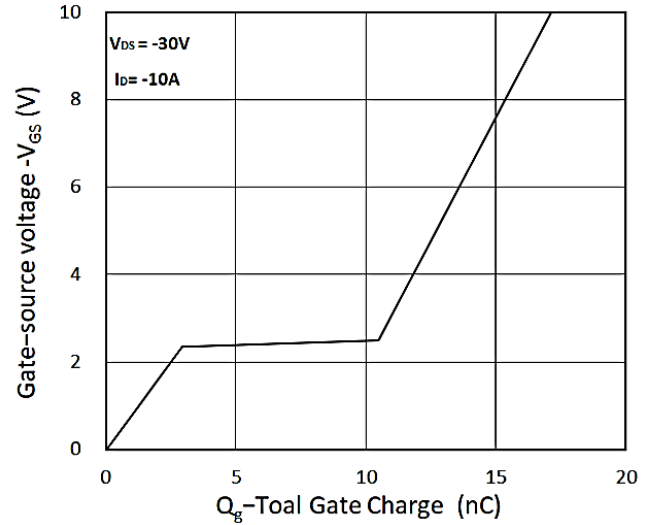


Figure 8. Gate Charge Characteristics

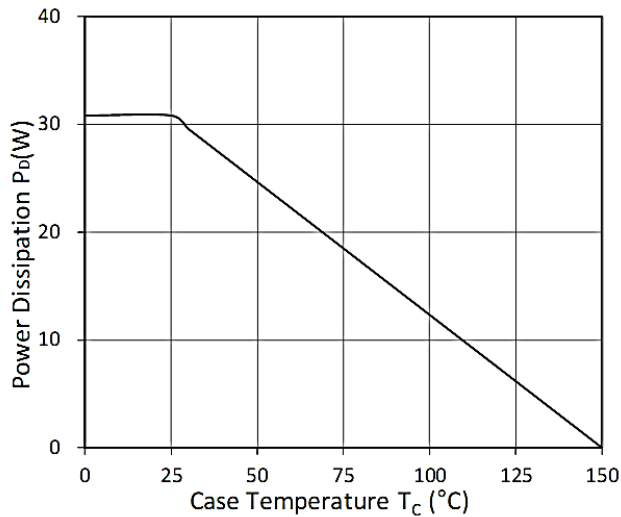


Figure 9. Power Dissipation

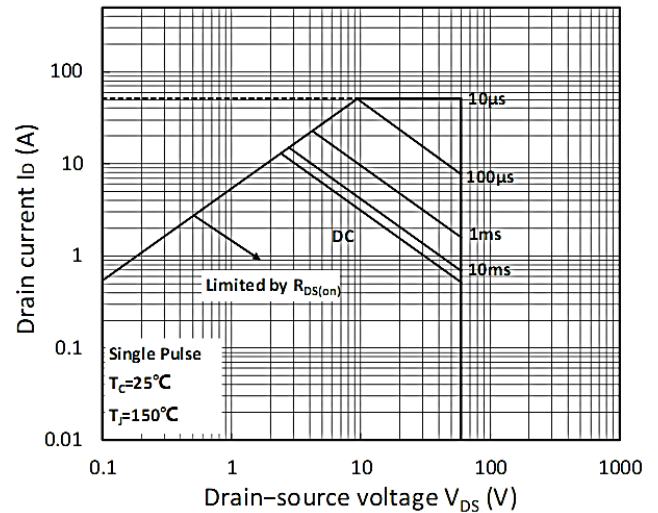


Figure 10. Safe Operating Area

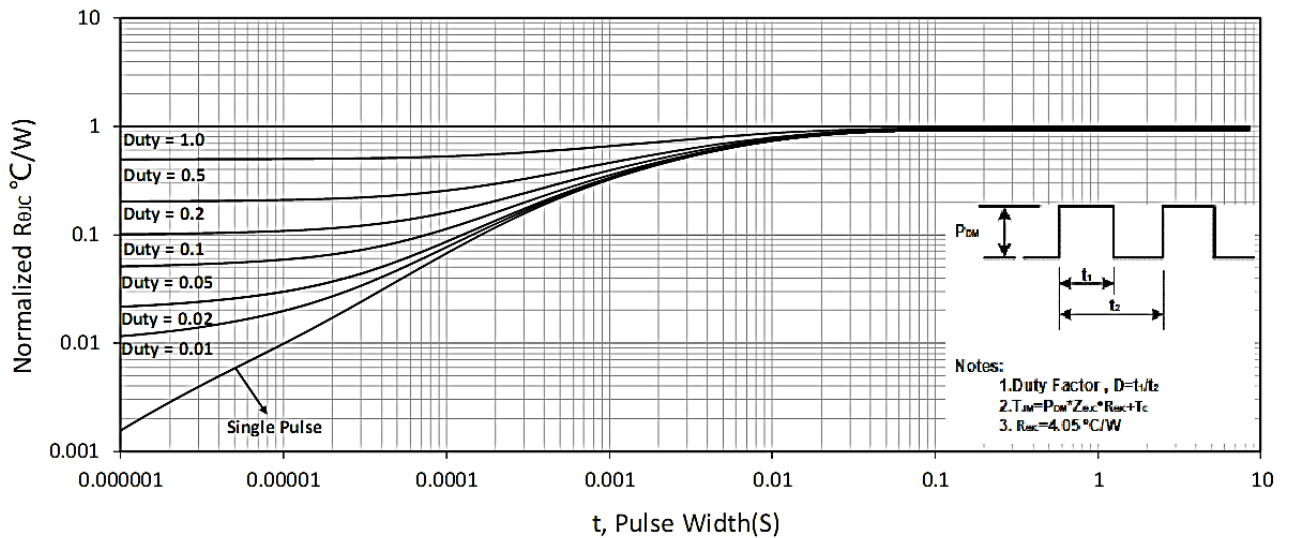
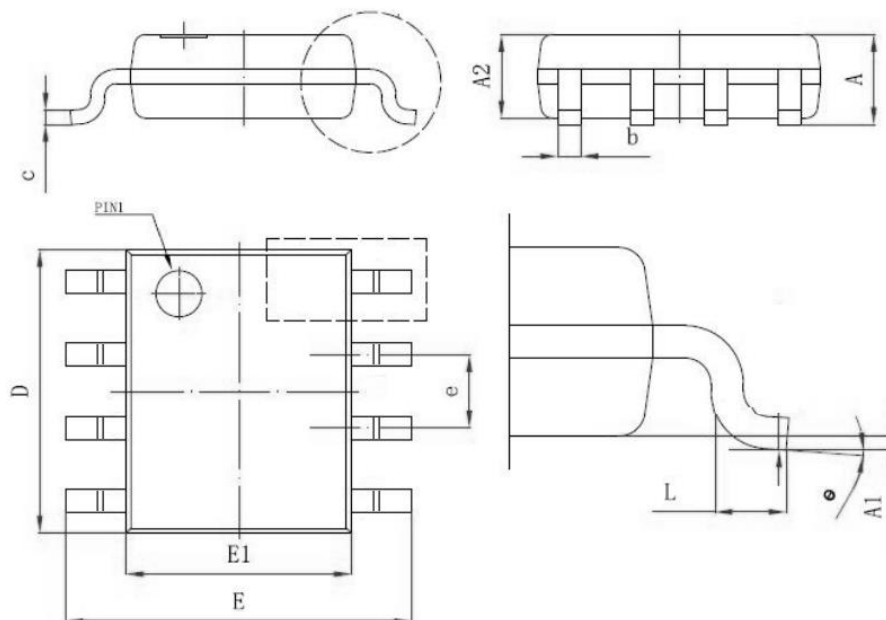


Figure 11 Normalized Maximum Transient Thermal Impedance

Package Mechanical Data-SOP-8L



Symbol	Dim in mm		
	Min	Typ	Max
A	1.35	1.55	1.75
A1	0.02	0.15	0.25
A2	1.425	1.45	1.475
b	0.3	0.4	0.5
c	0.15	0.2	0.25
D	4.8	5	5.2
E	5.8	6	6.2
E1	3.8	4	4.2
e	1.27BSC		
L	0.4		1.27
θ	0°		8°

60V N+P-Channel Enhancement Mode MOSFET**Attention**

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Edition	Date	Change
REV1.0	2023/5/31	Initial release

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