Low Standby-Power Off-line PWM converters

General Description

The AP8022 consists of an integrated Pulse Width Modulator (PWM) controller and power MOSFET, specifically designed for a high performance off-line converter with minimal external components. AP8022 offers complete protection coverage with automatic self-recovery feature including Cycle-by-Cycle current limiting (OCP), over voltage protection (OVP), over temperature protection (OTP) and soft-start. Burst mode operation and device very low consumption helps to meet the standby energy saving regulations. Excellent EMI performance is achieved with frequency modulation. The device consists of the high voltage start-up circuit. The device provides an advanced platform well suited for low standby-power and cost-effective flyback converters.

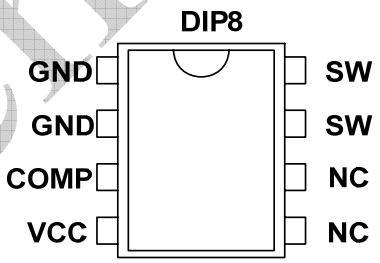
Features

- ■ 85v to 265v wide range AC voltage input
- ■Internal 700V avalanche-rugged power MOSFET
- ■Operating Frequency(60kHz)
- ■9.5v to 27v wide range VCC voltage
- ■ Frequency modulation for low EMI
- ■ Burst-mode Operation
- ■ Built-in Soft Start
- ■ Internal HV Start-up Circuit
- ■ Excellent Protection :
  - ✧ Over Current Protection (OCP)
  - ✧ Over Temperature Protection (OTP)
  - ✧ Over Voltage Protection (OVP)

Applications

- ■Small Household Application auxiliary power
- ■ LED Driver

Package/Order Information



Order codes	Package	Package
		85~265 V_{AC}
AP8022FNEC-T1	DIP8	10W
Note: the maximum output power should be tested in open frame with heat sink at 50℃.		

Typical Application

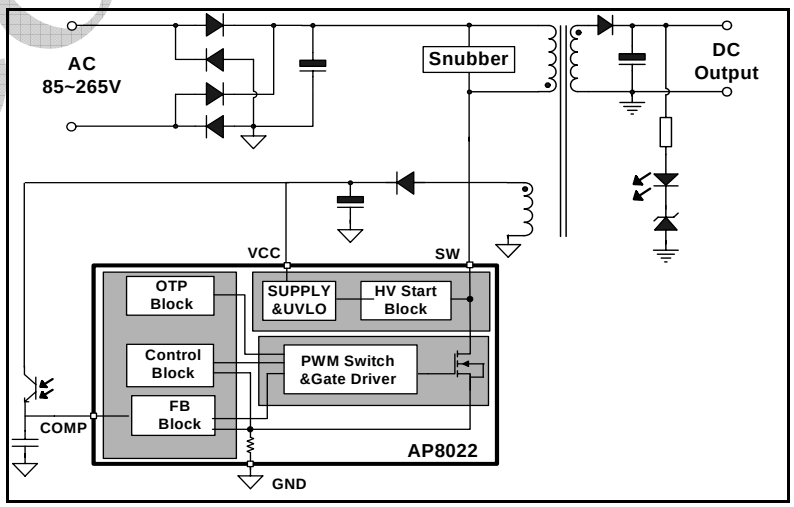


Figure 1. Typical Block Diagram

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Pin Definitions

Table 1. Pin Definitions

Pin Number	Pin Name	Pin Function Description
1,2	GND	Ground
3	COMP	Voltage feedback. By connecting a opto-coupler to close the control loop and achieve the regulation.
4	VCC	Positive Supply voltage Input.
5,6	NC	No connection
7,8	SW	The SW pin is designed to connect directly to the primary lead of the transformer and is capable of switching a maximum of 650V.

Note: NC Pin can be connected to SW

Typical power

Table 2. Typical power

Part number	85~265 V_{AC}	230 V_{AC} ±15%
AP8022	**12W**	**20W**

Note:

Maximum practical continuous power in an open frame design at 50 °C ambient, with adequate heat sinking.

Absolute Maximum Ratings

Supply voltage Pin VCC……..…-0.3~27V

High-Voltage Pin, SW…… 670V

Start-up Voltage ,SW to GND Voltage……670V

Pin COMP Feedback Current……3mA

Continuous VDMOS Drain Current…… Internally limited

Electrostatic Discharge Machine Mode……200V

Junction Operating Temperature…… Internally limited

Case Operating Temperature……-40~150℃

Storage Temperature Range…… -55~150℃

Lead Temperature (Soldering, 10secs) ……260℃

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Electrical Characteristics

(T_A=25°C, V_{CC} = 18 V; unless otherwise specified)

Table 3. Thermal section

SYMBOL	PARAMETER	DIP8	UNIT
R_{THJC_MAX}	Thermal resistance junction package	40	℃/W
R_{THJA_MAX}	Thermal resistance junction ambient	80	℃/W

Note: Drain Pin Connect 100mm^2 PCB copper clad.

Table 4. Power section

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	DMOS Breakdown Voltage	I_D=250uA;V_{COMP}=2V	670			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{SW}=500V;V_{COMP}=2V;			100	μA
R_{DSON}	Static Drain-Source on Resistance	I_D=0.4A;		15	17	Ω
T_r	Rise Time	I_D=0.1A;V_{SW}=300V		50		ns
T_f	Fall Time	I_D=0.2A;V_{SW}=300V		100		
Coss	DMOS Drain Capacitance	V_{SW}=25V		20		pF

Table 5. Control section

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
UVLO SECTION						
V_{START}	VCC Start Threshold Voltage	V_{COMP}=0V	13	14.5	16	V
V_{STOP}	VCC Stop Threshold Voltage	V_{COMP}=0V	7.5	8.5	9.5	V
V_{HYS}	VCC Threshold Hysteresis	V_{START} -V_{STOP}		6		V
OSCILLATOR SECTION						
F_{OSC}	Initial Accuracy	V_{STOP}≤VCC≤Vovp; 0≤T_j≤ 100°C	54	60	66	kHz
ΔF/ΔT	Frequency Change With Temperature	-25°C ≤ T_j ≤ +125°C		±2	±5	%
FD	Frequency Variation			±5		kHz
FM	Modulation frequency			125		Hz
D_{MAX}	Maximum duty cycle		60	75	90	%
FEEDBACK SECTION						

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I_{COMP}	Feedback Shutdown Current			1		mA
R_{COMP}	COMP Pin Input Impedance			1.1		kΩ
CURRENT LIMIT(SELF-PROTECTION)SECTION						
I_{LIM}	Peak Current Limit	T_j = 25°C	0.6	0.7	0.8	A
T_{ONMIN}	Minimum Turn On Time			400		ns
t_{SS}	Soft-start time			8		ms
PROTECTION SECTION						
T_{SD}	Thermal Shutdown Temperature		120	160	-	°C
T_{HYST}	Thermal Shutdown Hysteresis			40		°C
V_{OVP}	Over Voltage Protection		27	30	33	V
Vclamp	VCC Clamp Voltage	V_{COMP}=0 I_{VCC}>3mA	30	33	36	V
SUPPLY CURRENT SECTION						
V_{SW_START}	Drain-source start voltage				105	V
I_{CH}	Startup Charging Current (SW pin)	V_{SW}=120V, V_{CC}=0V		-1		mA
I_{OP0}	Operating Supply Current (Control Part Only) Switching	V_{COMP} = 0V		0.6		mA
I_{OP1}	Operating Supply Current (Control Part Only) Not Switching	V_{COMP} = 2V		0.3		mA

Typical circuit

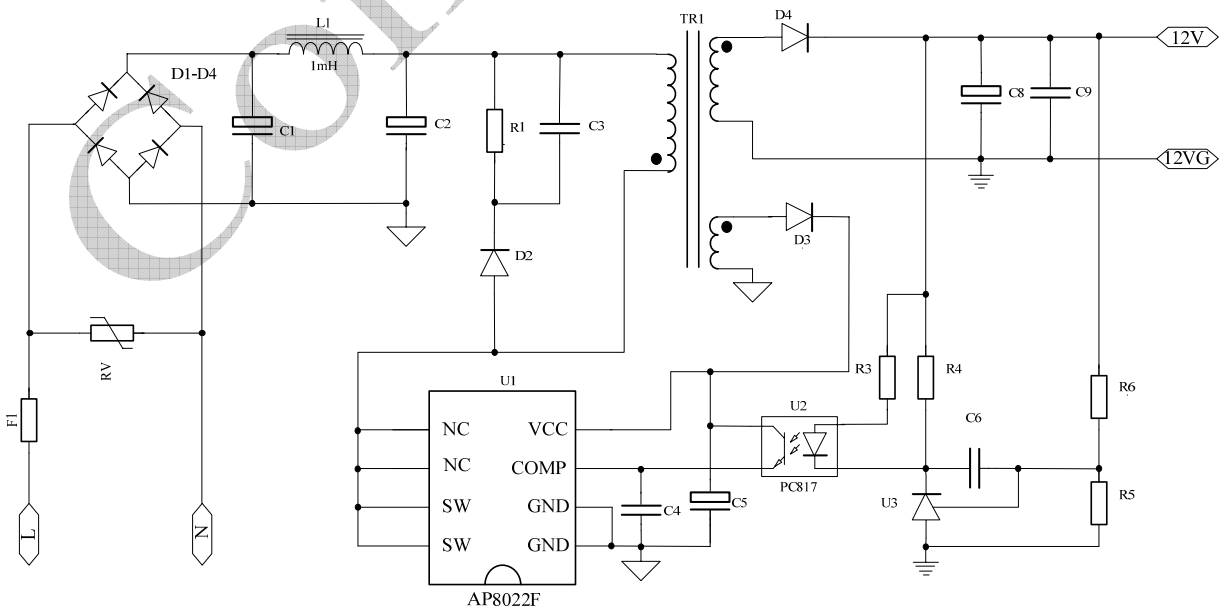

Figure 2. Flyback application (basic)

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Functional Description

1. Startup

This device includes a high voltage start up current source connected on the SW of the device. As soon as a voltage is applied on the input of the converter, this start up current source is activated and to charge the VCC capacitor as long as VCC is lower than VSTART. When reaching VSTART, the start up current source is cut off by UVLO&TSD and the device begins to operate by turning on and off its main power MOSFET. As the COMP pin does not receive any current from the opto-coupler, the device operates at full current capacity and the output voltage rises until reaching the regulation point where the secondary loop begins to send a current in the opto-coupler. At this point, the converter enters a regulated operation where the COMP pin receives the amount of current needed to deliver the right power on secondary side.

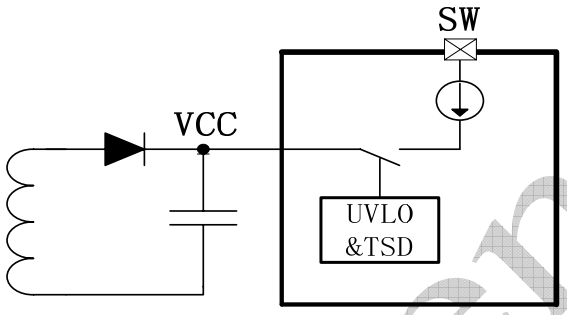

Figure9. Startup circuit

2. Soft-start up

In the process of start up, the current of drain increases to maximum limitation step by step. As a result, it can reduce the stress of secondary diode greatly and is propity to prevent the transformer turning into the saturation states. Typically, the duration of soft-start is 8ms.

3. Gate driver

The internal power MOSFET in AP8022 is driven by a dedicated gate driver for power switch control. Too weak the gate driver strength results in higher conduction and switch loss of MOSFET while too strong gate drive results in worse EMI.

A good tradeoff is achieved through the built-in totem pole gate design with proper output strength and dead time. The good EMI system design and low idle loss is easier to achieve with this dedicated control scheme.

4. Oscillator

The switching frequency of AP8022 is internally fixed at 60 kHz. No external frequency setting components are required for PCB design.

The frequency modulation is implemented in AP8022. So that, it minimizes the conduction band EMI and therefore eases the system design because the tone energy could be spread out.

5. Feed-back

A feedback pin controls the operation of the device. Unlike conventional PWM control circuits which use a voltage input, the COMP pin is sensitive to current. Figure 10 presents the internal current mode structure. The Power MOSFET delivers a sense current which is proportional to the main current. R2 receives this current and the current coming from the COMP pin. The voltage across R2(VR2) is then compared to a fixed reference voltage. The

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MOSFET is switched off when VR2 equals the reference voltage.

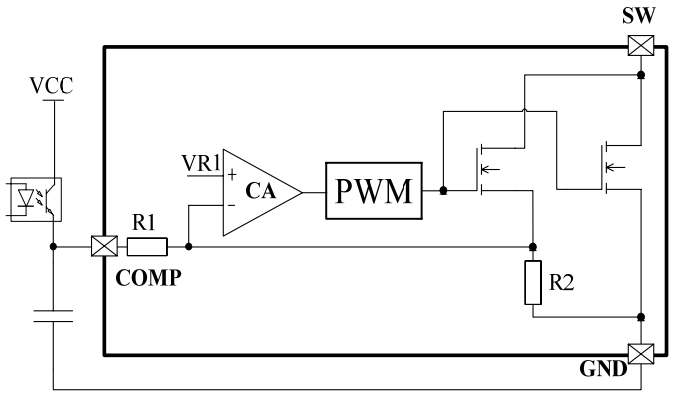

Figure10. Feedback circuit

6. Leading Edge Blanking (LEB)

At the instant the internal Sense FET is turned on, there usually exists a high current spike through the Sense FET, caused by the primary side capacitance and secondary side rectifier diode reverse recovery. Excessive voltage across the sense resistor would lead to false feedback operation in the current mode PWM control. To counter this effect, the device employs a leading edge blanking (LEB) circuit. This circuit inhibits the PWM comparator for a short time (typically 300ns) after the Sense FET is turned on.

7. Under Voltage Lock Out

Once fault condition occurs, switching is terminated and the Sense FET remains off. This causes VCC to fall. When VCC reaches the UVLO stop voltage, 9V, the protection is reset and the internal high voltage current source charges the VCC capacitor. When VCC reaches the UVLO start voltage, 13V, the device resumes its normal operation. In this manner, the auto-restart can alternately enable and disable the switching of the power Sense FET until the fault condition is eliminated.

8. Thermal Shutdown (TSD)

The Sense FET and the control IC are integrated in the same chip, making it easier for the control IC to detect the temperature of the Sense FET. When the temperature exceeds approximately 160°C, thermal shutdown is activated, the device turn off the Sense FET and the high voltage current source to charge VCC. The device will go back to work when the lower threshold temperature about 120°C is reached.

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Package Dimensions（DIP8）

Table 6. DIP8 mechanical data

尺寸 / 符号	最小(mm)	最大(mm)	尺寸 / 符号	最小(mm)	最大(mm)
A	9.30	9.50	C2	0.50	
A1	1.524		C3	3.3	
A2	0.39	0.53	C4	1.57TYP	
A3	2.54		D	8.2	8.8
A4	0.66TYP		D1	0.2	0.35
A5	0.99TYP		D2	7.62	7.87
B	6.3	6.5	Θ1	8°TYP	
C	7.2		Θ2	8°TYP	
C1	3.3	3.5	Θ3	5°TYP	

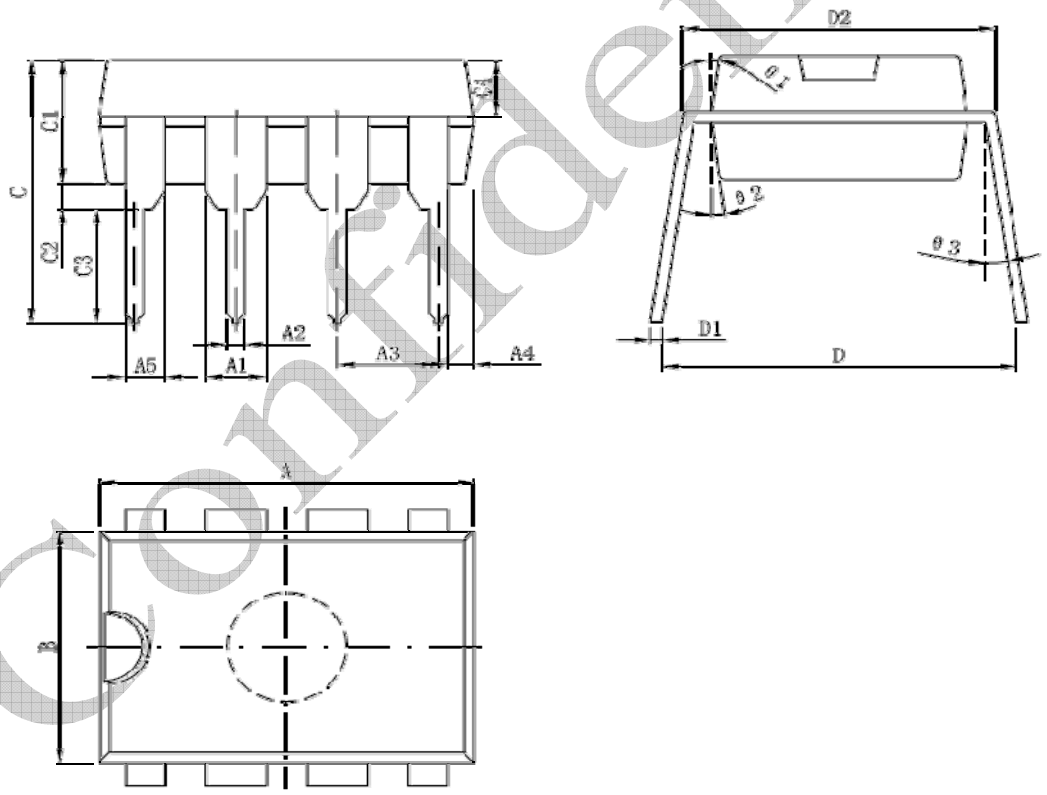

Figure 11. Package dimensions

TOP MARK	Package
AP8022 YWWXXXXX	DIP8

Note: Y: Year Code; W: Week Code; XXXXX: Internal Code

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