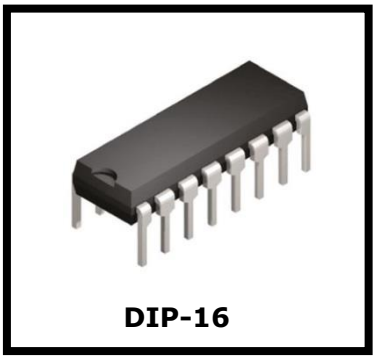
Bipolar Stepping Motor Driver IC

Description

The AP8100 is 2 phase stepping motor driver IC.
It consists of TTL compatible input circuits, dual bridge driver outputs with flyback diodes, changing circuit of motor coil drive voltage (Power saving circuit) and stand-by circuit



DIP-16

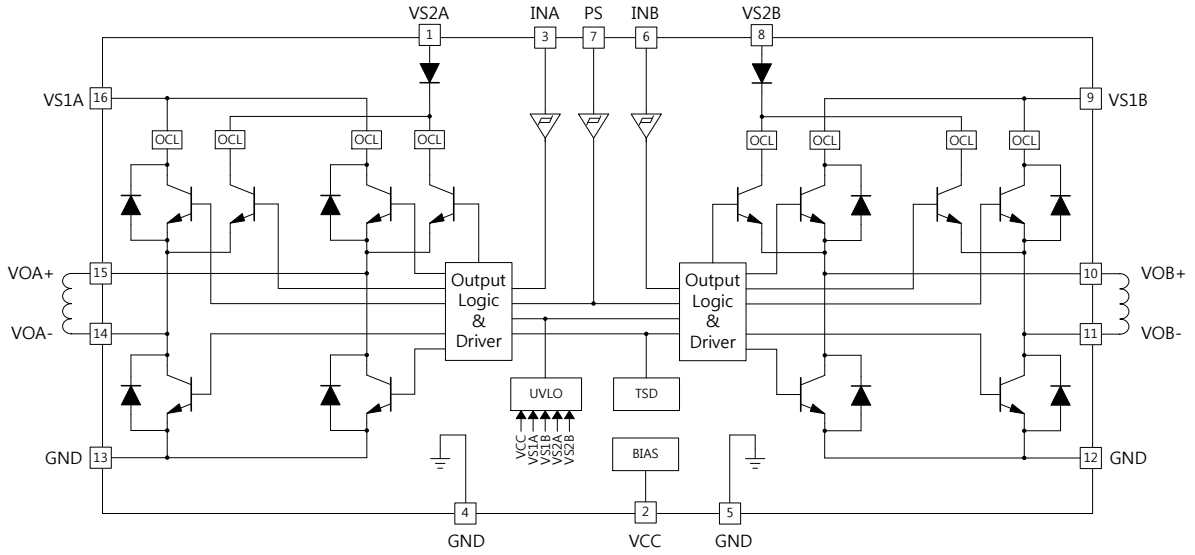
Features

- One Chip 2 Phase Stepping Motor Driver including two bridge drivers
- Power Saving and Stand-by Operation
- Short-Through Current Restriction Circuit
- TTL Compatible Inputs
- Output Current up to 400mA(Peak)
- Over Current Shutdown Circuit
- Thermal Shutdown Circuit
- Under Voltage Lockout Circuit
- Pull-down Resistance for Input

Application

- FDD, Refrigerator Actuator

Block Diagram



Note : Pin 4, 5, 12 and 13 are internally connected.

Pin Description

Pin No	Symbol	Functional Description
1	V_{S2A}	Low-voltage power supply terminal
2	V_{CC}	Power voltage supply terminal for control
3	INA	A-ch forward rotation / reverse rotation signal input terminal, Truth Table 1
6	INB	B-ch forward rotation / reverse rotation signal input terminal, Truth Table 1
7	PS	Power saving signal input terminal
8	V_{S2B}	Standby signal input terminal, Truth Table 2
9	V_{S1B}	High-voltage power supply terminal
10	VOB+	Output B+
11	VOB-	Output B-
14	VOA-	Output A-
15	VOA+	Output A+
16	VS1A	High-voltage power supply terminal
4, 5, 12, 13	GND	GND terminal (Logic and Power GND)

Truth Table 1.

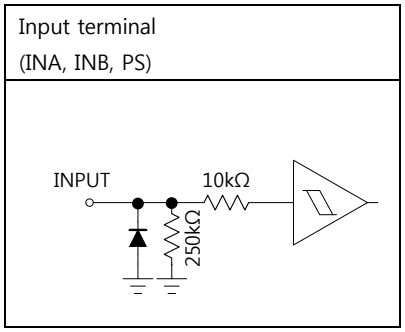
Input		Output (x : A, B)		
PS	IN	VOx+	VOx-	Mode
L	L	L	H	ENABLE V_{S1}
L	H	H	L	ENABLE V_{S1}
H	L	L	H	ENABLE V_{S2}(Power saving)
H	H	H	L	ENABLE V_{S2}(Power saving)

Truth Table 2.

VS2B	Mode
L	POWER OFF (Standby mode)
H	OPERATION

Note : Apply 5V to VS2A as a supply terminal.

Terminal Circuit



The diagram is partly-provided and omitted or simplified for explanatory purposes.

Maximum Ratings Characteristics

(T_A = 25℃ unless otherwise specified)

Characteristics	Symbol	Value	Unit
Supply voltage	V_{CC}	7.0	V
	V_{S1}	17.0	
	V_{S2}	VCC	
Output current	I_O (PEAK)	±400	mA
	I_O (START)	±350	
	I_O (HOLD)	±100	
Input voltage	V_{IN}	VCC	V
Power dissipation	P_D	1.4	W
Operating temperature	T_{opr}	-30 ~ 75	℃
Storage temperature	T_{stg}	-55 ~ 150	℃

Recommended Operating Conditions

(T_A = 25℃ unless otherwise specified)

Characteristics	Symbol	Min	Typ.	Max	Unit
Supply voltage	V_{CC}	4.5	-	5.5	V
	V_{S1}	-	12	-	
	V_{S2}	2.7	-	5.5	
	V_{IN}	-	-	VCC	

* Operating Voltage Restriction : $V_{S1} \geq V_{S2A}$

Electrical Characteristics

(T_A = 25℃, V_{CC} = 5V, V_{S1} = 12V, V_{S2A} = 5V unless otherwise specified)

Characteristics	Symbol	Test Circuit	Condition	Min	Typ.	Max	Unit
UNDER VOLTAGE LOCKOUT SECTION							
Start Threshold Voltage	V_{ST}	-	V_{CC} Increasing	3.7	4.21	4.5	V
UVLO Hysteresis	V_{HYS}	-	-	-	0.1	-	V
SUPPLY CURRENT SECTION							
V_{CC} Supply Current	I_{CC1}	1	PS : H, V_{S2} : H	-	3.1	4.5	mA
	I_{CC2}		PS : L, V_{S2} : H	-	3.1	4.5	
	I_{CC3}		PS : L, V_{S2} : L	-	65	100	μA
V_{S1} Supply Current	I_{VS1}	1	PS : L	-	1.6	3	mA
V_{S2} Supply Current	I_{VS2}	1	PS : L	-	1.6	2.4	
	I_{VS2_ON}	1	PS : H	-	2.5	3.75	
INPUT VOLTAGE SECTION							
Input Logic High Level	$V_{IN}H$	-	V_{S2} : H	2.0	-	V_{CC}	V
Input Logic Low Level	$V_{IN}L$	-		0	-	0.8	
PS Input High Level	$V_{PS}H$	-		2.0	-	V_{CC}	
PS Input Low Level	$V_{PS}L$	-		0	-	0.8	
INPUT CURRENT SECTION							
Logic Input Current	I_{IN}	-	$V_{IN/PS}$ = 5V	-	20	30	μA
PS Input Current	I_{PS}	-					
OUTPUT VOLTAGE SECTION							
Output Saturation Voltage	$V_{SAT}1H1$	3	PS : L, V_{S2} : H, I_{OUT} = 100mA	-	1.14	-	V
	$V_{SAT}1H2$	3	PS : L, V_{S2} : H, I_{OUT} = 400mA	-	1.39	-	
	$V_{SAT}2H1$	3	PS : H, V_{S2} : H, I_{OUT} = 30mA	-	1.94	-	
	$V_{SAT}2H2$	3	PS : H, V_{S2} : H, I_{OUT} = 100mA	-	2.19	-	
	$V_{SAT}L1$	3	V_{S2} : H, I_{OUT} = 30mA	-	0.14	-	
	$V_{SAT}L2$	3	V_{S2} : H, I_{OUT} = 100mA	-	0.24	-	
	$V_{SAT}L3$	3	V_{S2} : H, I_{OUT} = 400mA	-	0.59	-	
DIODE SECTION							
Diode Forward Voltage	$V_F U1$	2	I_F = 30mA	-	0.91	-	V
	$V_F D1$	2		-	0.76	-	
	$V_F U2$	2	I_F = 100mA	-	1.02	-	
	$V_F D2$	2		-	0.89	-	
	$V_F U3$	2	I_F = 350mA	-	1.30	-	
	$V_F D3$	2		-	1.21	-	
OUTPUT DELAY SECTION							
Delay Time	t_{pLH}	-	Output Rising	-	6.3	-	us
	t_{pHL}	-	Output Falling	-	0.6	-	

Characteristics	Symbol	Test Circuit	Condition	Min	Typ.	Max	Unit
PROTECTION SECTION*							
Thermal Shutdown	TSD	-	-	-	170	-	℃
TSD Hysteresis	TSDhys	-	-	-	25	-	
Output Limit Current	I_{limit}	-	-	0.4	0.8	-	A

*: These parameters, although guaranteed, are not 100% tested in production.

Under voltage Lockout Circuit (UVLO)

An under voltage lockout circuit is included.

Outputs are turned off under the conditions as follows;

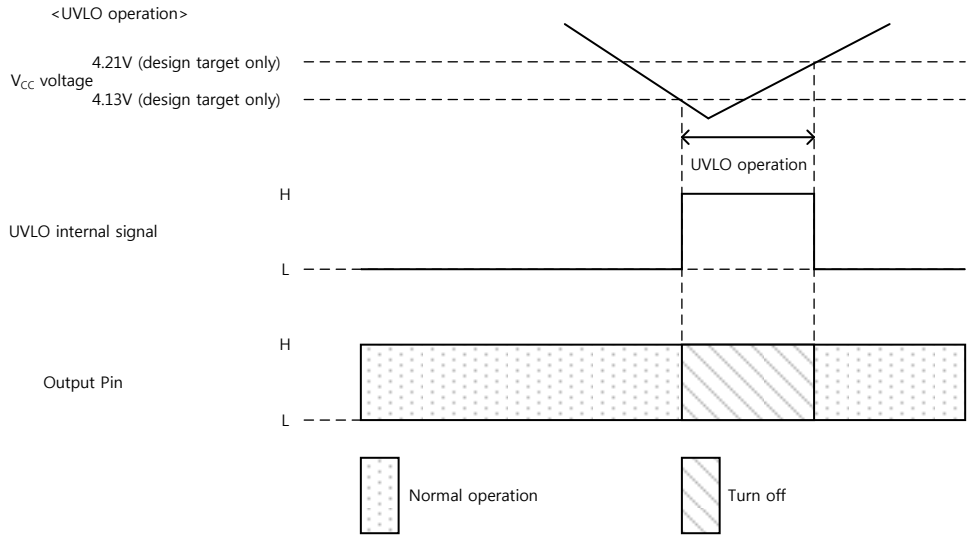
V_{CC} ≤ 4.21V (Design target) or

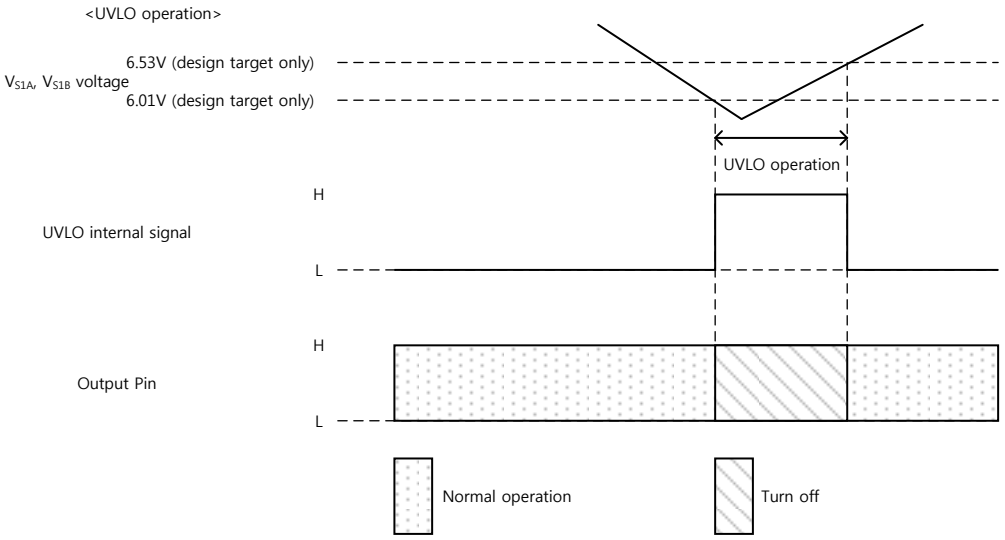
V_{S1A} ≤ 6.53V (Design target) and V_{S1B} ≤ 6.53V (Design target) or

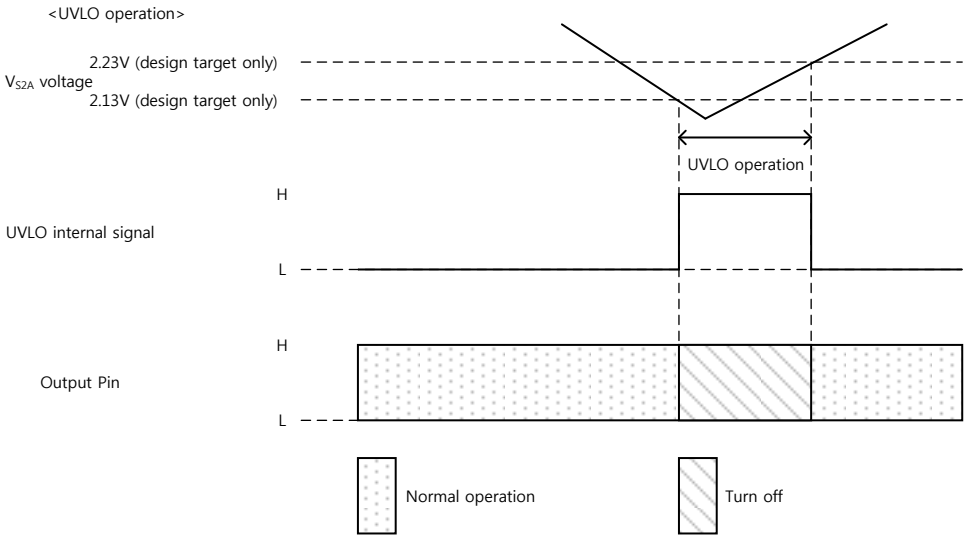
V_{S2A} ≤ 2.23V (Design target)

The UVLO circuit has a hysteresis and the function recovers under the conditions as follows;

V_{CC} = 4.21V (Design target), V_{S1A}/V_{S1B} = 6.53V (Design target), V_{S2A} = 2.23V (Design target)





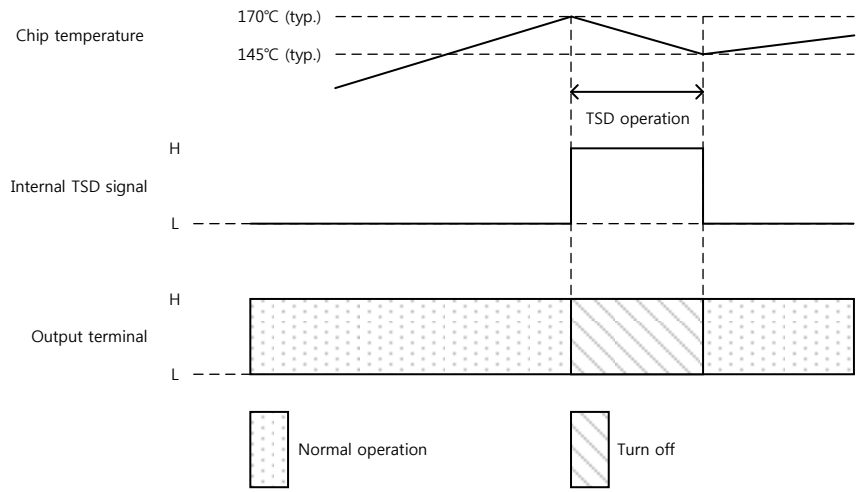

<UVLO operation>
2.23V (design target only)
V_{S2A} voltage
2.13V (design target only)
UVLO operation
H
UVLO internal signal
L
H
Output Pin
L
Normal operation
Turn off

Thermal Shutdown Circuit (TSD)

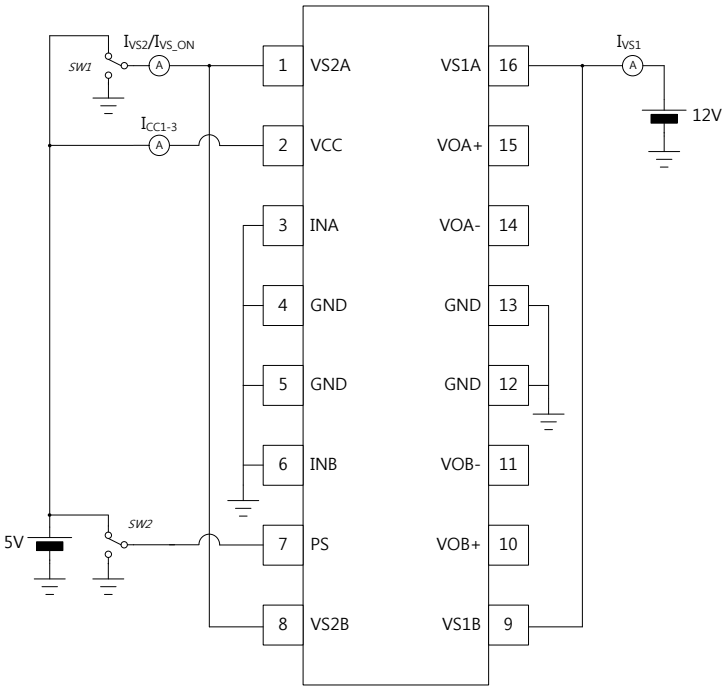
The AP8100 has a thermal shutdown circuit. If the junction temperature (T_j) exceeds 170℃ (design target only), all the outputs are turned off.
It recovers automatically at 145℃, It has a hysteresis width of 25℃.

TSD = 170℃ (design target only)

<TSD operation>



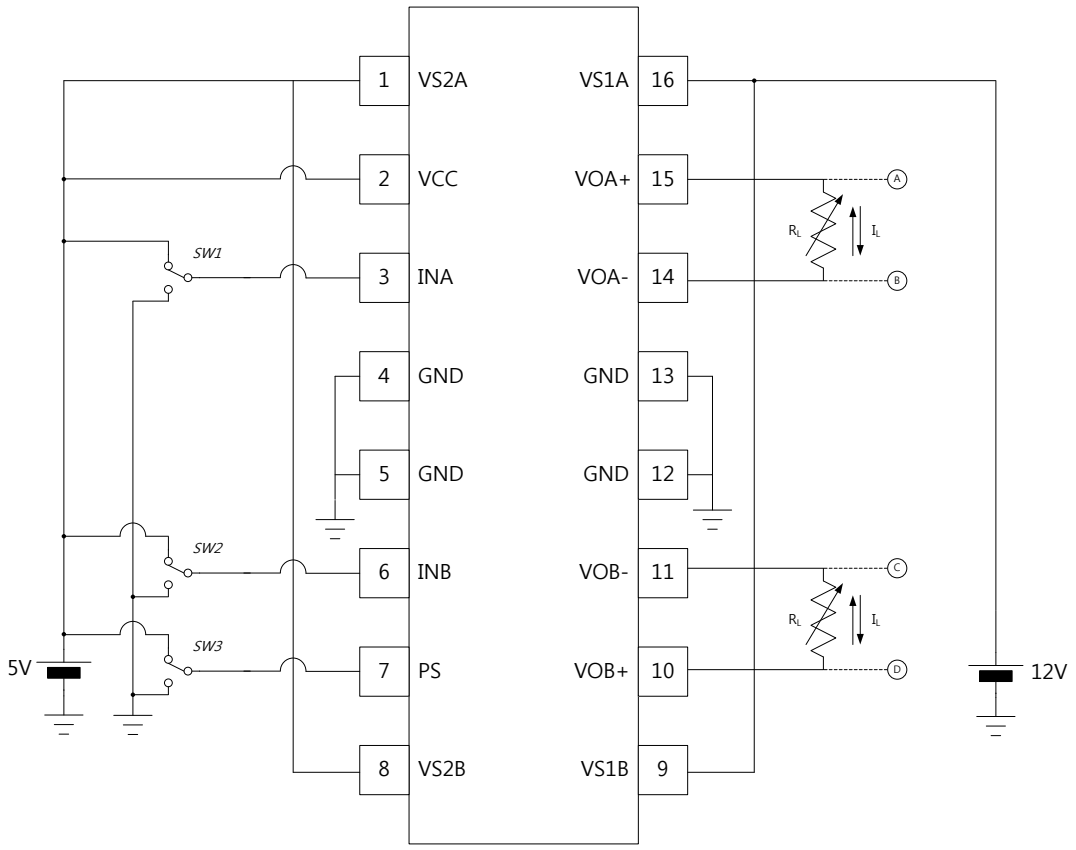
Test Circuit 1. I_{CC1}, I_{CC2}, I_{CC3}, I_{VS1}, I_{VS2}, I_{VS2_ON}



Item	SW1	SW2
ICC1	H	H
ICC2	H	L
ICC3	L	L
IVS1	H	L
IVS2	H	L
IVS2_ON	H	H

External capacitors are removed for simplified test circuit; Further information is described on "Application Circuit" below.

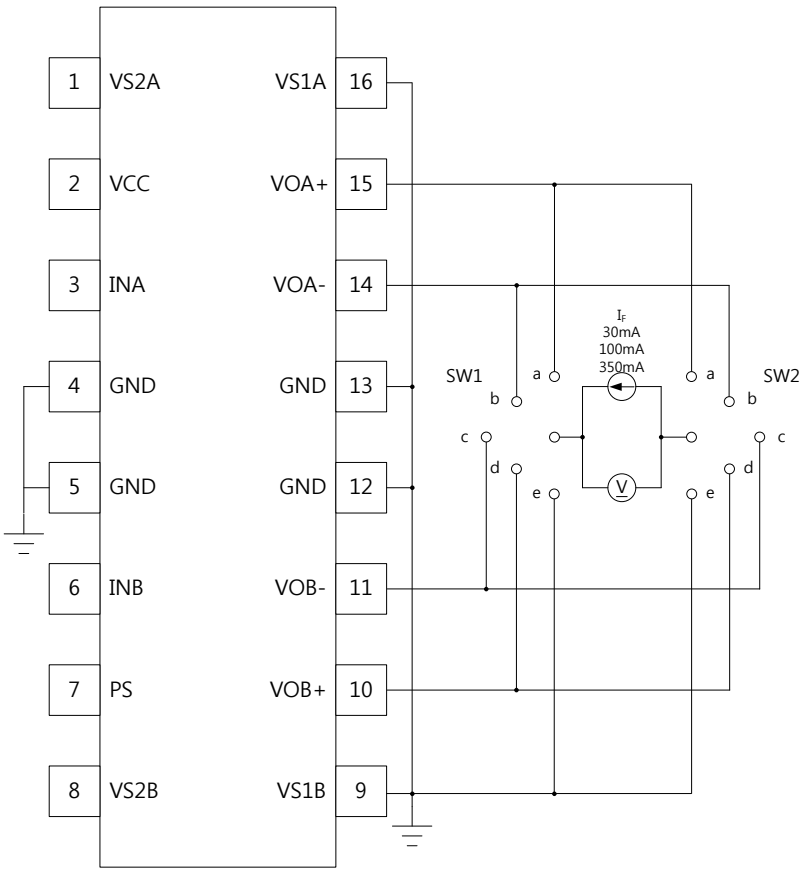
Test Circuit 2. $V_{SAT}1H1$, $V_{SAT}1H2$, $V_{SAT}2H1$, $V_{SAT}2H2$, $V_{SAT}L1$, $V_{SAT}L2$, $V_{SAT}L3$



Item	IL (mA)	Output (x=A,B)	SW1	SW2	SW3	Measurement Point (A, B, C, D : node)
$V_{SAT}1H1$	100	VOx+	H	H	L	12V-V_A, 12V-V_D
		VOx-	L	L	L	12V-V_B, 12V-V_C
$V_{SAT}1H2$	400	VOx+	H	H	L	12V-V_A, 12V-V_D
		VOx-	L	L	L	12V-V_B, 12V-V_C
$V_{SAT}2H1$	30	VOx+	H	H	H	5V-V_A,5V-V_D
		VOx-	L	L	H	5V-V_B, 5V-V_C
$V_{SAT}2H2$	100	VOx+	H	H	H	5V-V_A, 5V-V_D
		VOx-	L	L	H	5V-V_B, 5V-V_C
$V_{SAT}L1$	30	VOx+	H	H	—	Node B, node C
		VOx-	L	L	—	Node A, node D
$V_{SAT}L2$	100	VOx+	H	H	—	Node B, node C
		VOx-	L	L	—	Node A, node D
$V_{SAT}L3$	400	VOx+	H	H	—	B, C
		VOx-	L	L	—	A, D

External capacitors are removed for simplified test circuit; Further information is described on "Application Circuit" below.

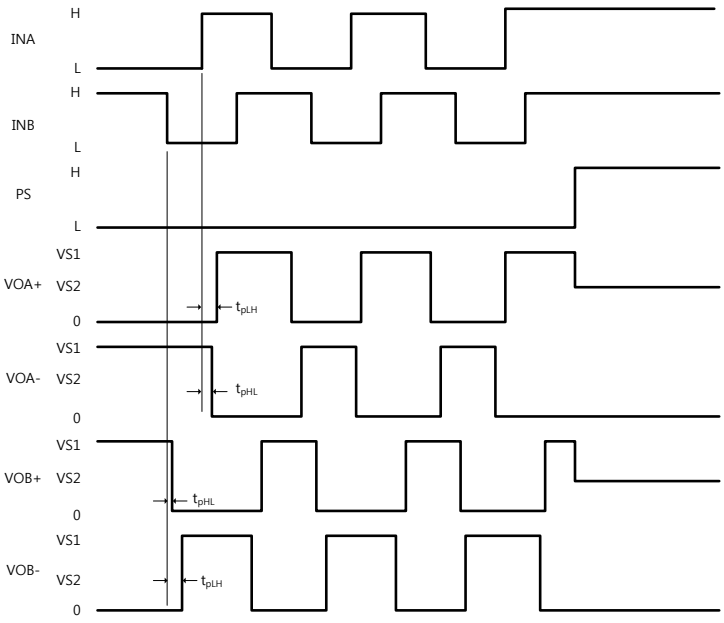
Test Circuit 3. V_FU, V_FD



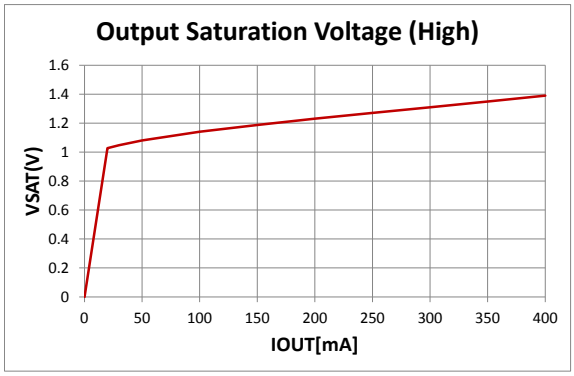
Item	SW1	SW2
VFU	a	e
	b	
	c	
	d	
VFL	e	a
		b
		c
		d

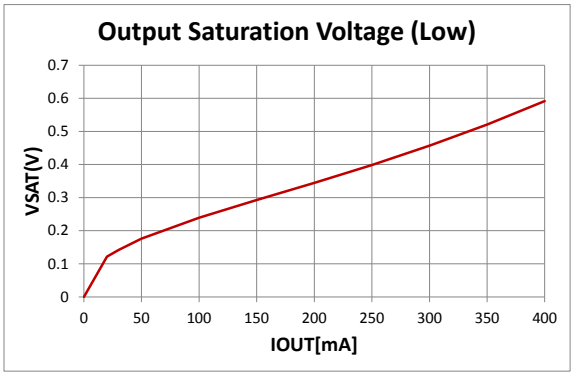
External capacitors are removed for simplified test circuit; Further information is described on "Application Circuit" below.

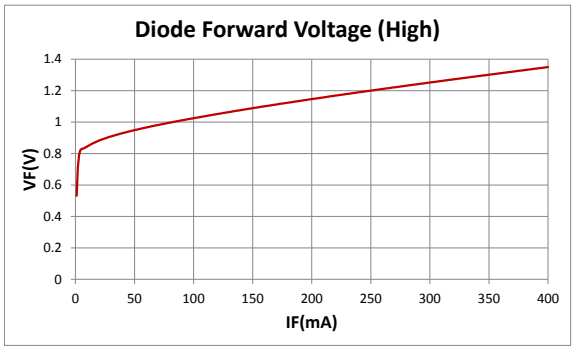
Timing Chart

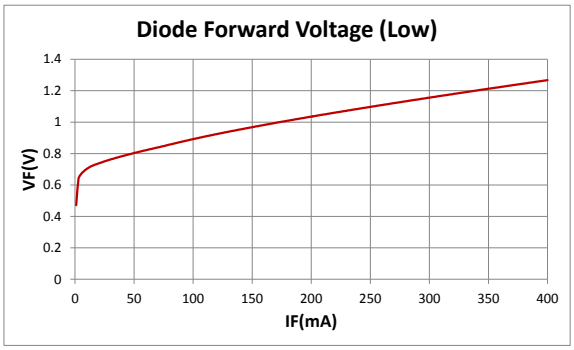


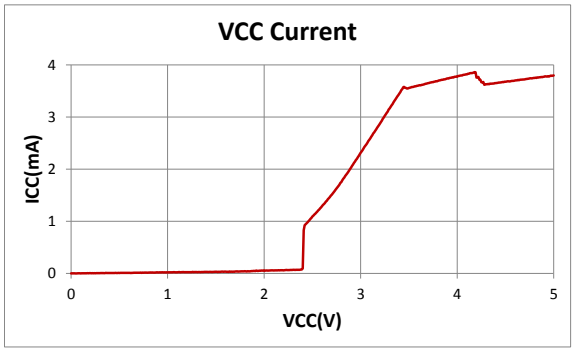
Typical Performance Characteristics



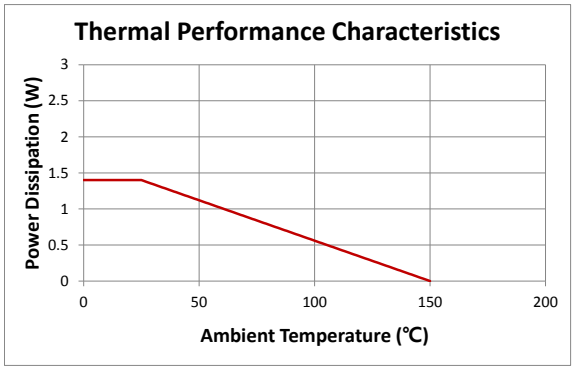




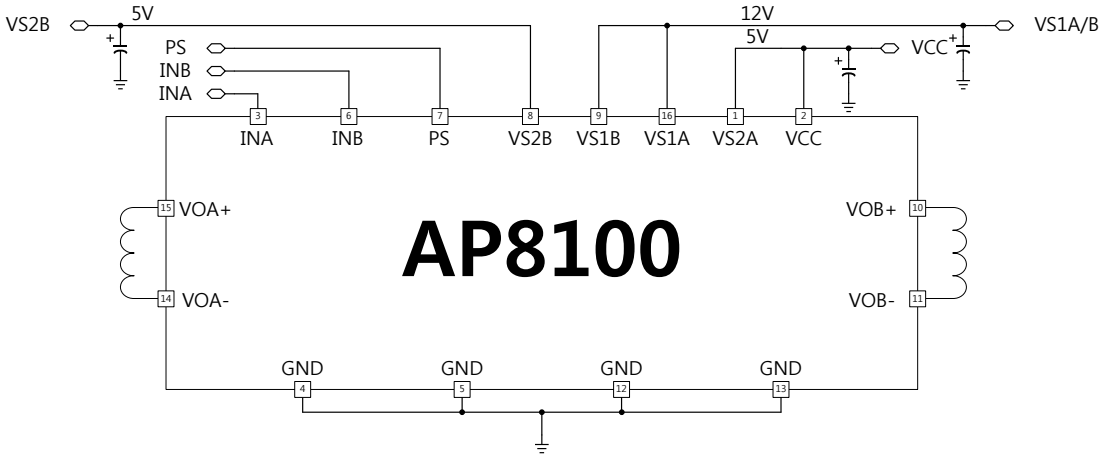




Thermal Performance Characteristics



Application Circuit



Ordering Information

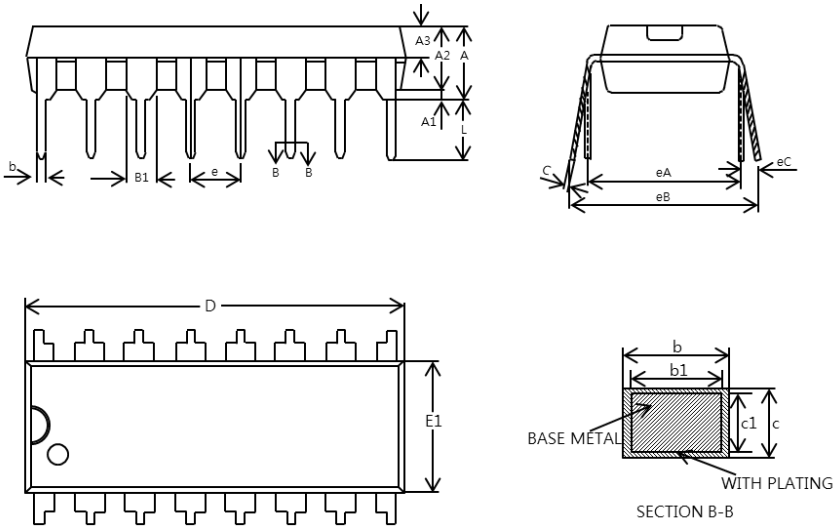
Part No	Package	Packing	Finish	Halogen	Packing Unit
AP8100	DIP-16	Tube : 25pcs	Sn	Free	5,000pcs

Marking Layout

1ST Line : Company logo

2nd Line : Device name : AP8100D
-D : DIP-16 PKG code
3rd Line : Date code
- YY : Last two digit of calendar year
- WW : Work week calendar
- Z : ASSEMBLY SITE

Package Dimensions



SYMBOL	MLLIMETER		
	MIN	NOM	MAX
A	3.60	3.80	4.00
A1	0.51	—	—
A2	3.20	3.30	3.40
A3	1.47	1.52	1.57
b	0.44	—	0.52
b1	0.43	0.46	0.49
B1	1.52RFE		
c	0.25	—	0.29
c1	0.24	0.25	0.26
D	19.00	19.10	19.20
E1	6.25	6.35	6.45
e	2.54BSC		
eA	7.62REF		
eB	7.62	—	9.30
eC	0	—	0.84
L	3.00	—	—

Revision History

No	Date	Contents
REV00	2017-03-28	Initial Brief Datasheet Release
REV01	2018-03-20	Start Threshold Voltage Revised

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