NEW PRODUCT

Description

AP9060 is designed to protect the latest generation of PMICs for portable applications such as Smartphones, UMPCs and others that utilize battery power.

The device, with its integrated low resistance p-channel MOSFET, operates as a switch and passes the input voltage through to the output till the input reaches a clamp voltage limit. Once V_{IN} goes above the clamp limit, which is set to 11.15V, the output voltage gets clamped and the feedback loop maintains the clamped V_{OUT} by reducing the drive to the p-channel FET.

The output voltage is clamped at 11.15V to ensure that a following PMIC can detect a faulty charger and ensure safe and proper communication to the system.

AP9060 also supports reverse operation whereby it can pass up to 1A of current from the PMIC to the load connected to the USB port. This makes AP9060 suitable for USB On-The-Go enabled devices.

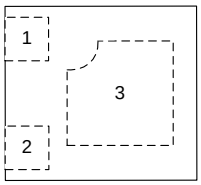
The AP9060 protection device is available in a low-profile W-DFN1114-3 package with a typical height of 0.8mm.

Applications

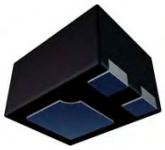
- Power Interface for New Generation PMICs
- Charger Front-End Protection
- Smartphones
- UMPC
- Portable Applications

Pin Assignments

W-DFN1114-3



Top View



Features

- Wide Input Voltage Range of 3V – 30V
- Ultra-Low Bias Current
- Integrated Low On-Resistance P-Channel FET
- Output Voltage Clamped at 11.15V
- PMOS Protection Mechanism – Removes EMI Issues Typically Associated with an NMOS Solution
- Supports Reverse Current Operation (USB OTG)
- Available in a W-DFN1114-3 Package
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Notes: 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit

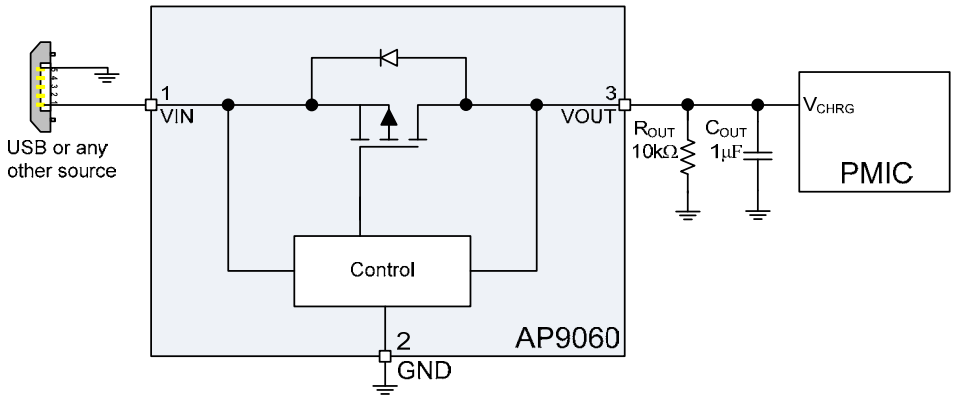


Figure 1. Typical Application Circuit

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Pin Descriptions

Pin Number	Pin Name	Function
1	VIN	Input voltage to the device.
2	GND	System ground.
3/PAD	VOUT	Output voltage, which follows V_{IN} and gets clamped if V_{IN} exceeds the clamp voltage of 11.15V (typ).

Functional Block Diagram

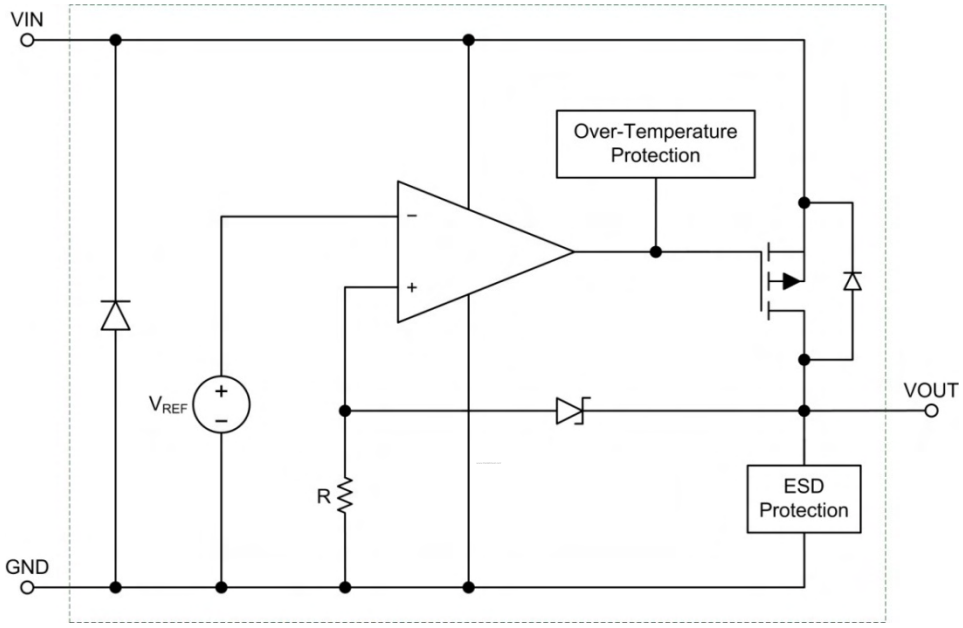

Figure 2. Functional Block Diagram

Absolute Maximum Ratings (Note 4) (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Rating	Unit
V_{IN}	Input Supply Voltage	-0.3 to +30	V
I_{MAX}	Maximum Continuous Switch Current (Note 6) T_A = +25°C T_A = +85°C	 2.6 1.6	A
P_D	Power Dissipation @ T_A = +25°C (Note 6)	1.1	W
T_J	Junction Temperature Range	-40 to +125	°C
T_{STG}	Storage Temperature Range	-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering Purposes	260	°C
ESD Susceptibility (Note 5)			
HBM	Human Body Model	4.0	kV
MM	Machine Model	300	V

Notes:
4. Stresses greater than the 'Absolute Maximum Ratings' specified above, may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time.
5. Semiconductor devices are ESD sensitive and may be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

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Thermal Resistance (Note 6)

Symbol	Parameter	Rating	Unit
θ_{JA}	Junction to Ambient	85	°C/W

Note: 6. Surface mounted on JEDEC's High Effective Thermal Conductivity Test Board (JESD51-7).

Recommended Operating Conditions (Note 7) (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
V_{IN}	Supply Voltage	3	30	V
T_A	Operating Ambient Temperature Range	−40	+85	°C

Note: 7. The device function is not guaranteed outside of the recommended operating conditions.

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

AP9060 is tested at V_{IN} = 5V, I_{OUT} = 0mA, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{CLAMP}	Output clamp voltage	V_{IN} = 30V	11.0	11.15	11.3	V
R_{ON}	On-Resistance (Note 8)	V_{IN} = 5V, I_{OUT} = 1000mA V_{IN} = 3V, I_{OUT} = 1000mA		90 105	120 139	mΩ
V_{pk}	Peak Output Voltage (Note 9)	V_{IN} goes from 0V to 30V with 100ns rise time, C_{OUT} = 100nF			16.0	V
I_{bias}	Input Bias Current	V_{IN} = 5V V_{IN} = 30V		5 25	6 31	µA
THM_{SD}	Thermal Shutdown Threshold (Note 9)	R_{OUT} = 10kΩ		140		°C
THM_{hyst}	Thermal Shutdown Hysteresis(Note 9)	R_{OUT} = 10kΩ		20		°C
V_{OUT_REV}	Reverse Supply Voltage on VOUT(Note 10)	I_{IN} = −500mA	3.0	5.0	8.0	V
I_{IN_REV}	Reverse Load Current on VIN (Note 10)	V_{OUT} = 5V		−500	−1000	mA
T_{start}	Soft-Start Time	V_{IN} = 5V		10		ms

Notes: 8. Pulse tested with a width of 20ms.
9. Guaranteed by design.
10. To support reverse power operation, as in the case of USB OTG systems. A voltage source is connected to V_{OUT} and a load connected on V_{IN}.

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Typical Performance Characteristics

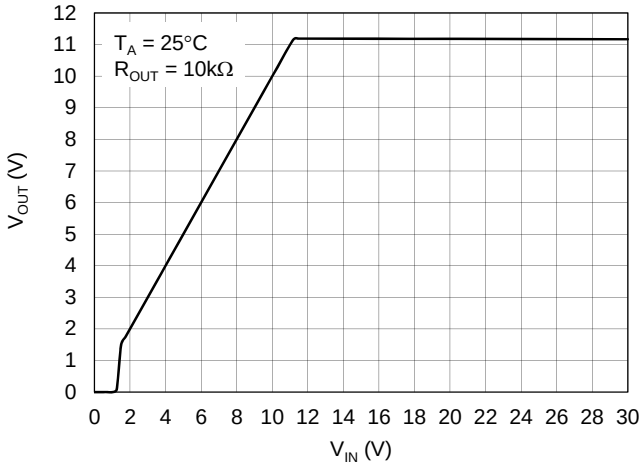


Figure 3. V_{OUT} vs. V_{IN}

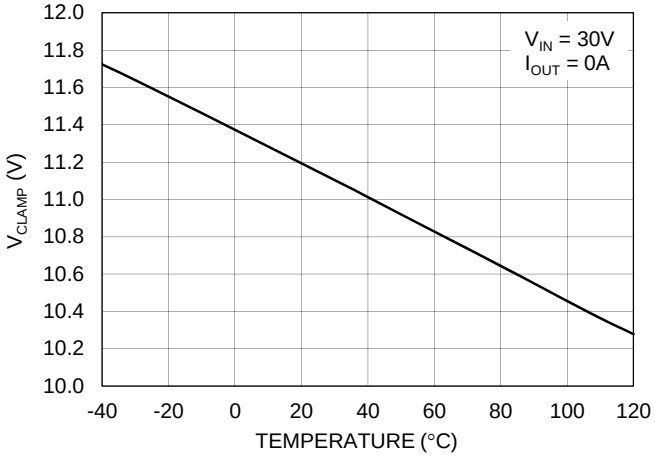


Figure 4. Output Clamp Voltage vs. Temperature

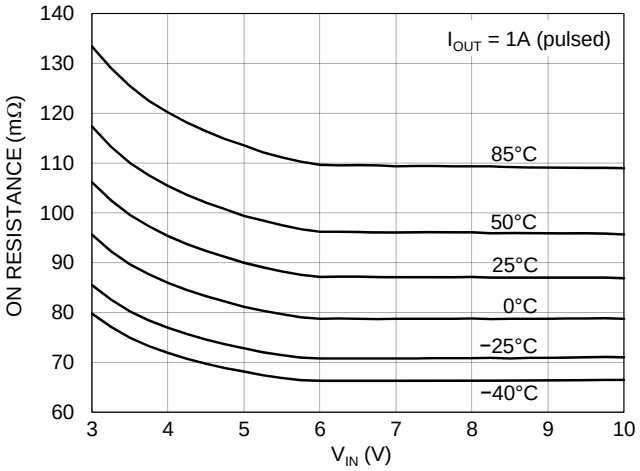


Figure 5. On-Resistance vs. V_{IN} and Temperature

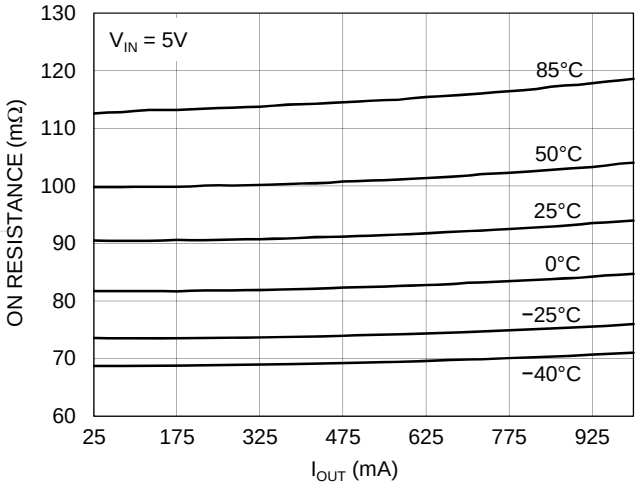


Figure 6. On-Resistance vs. I_{OUT} and Temperature

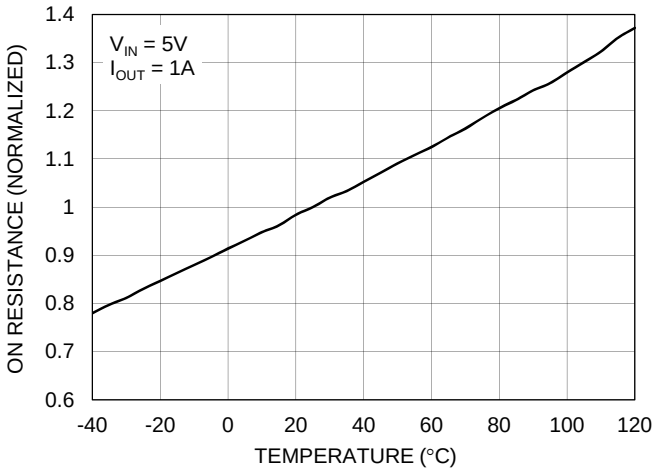


Figure 7. On-Resistance (normalized) vs. Temperature

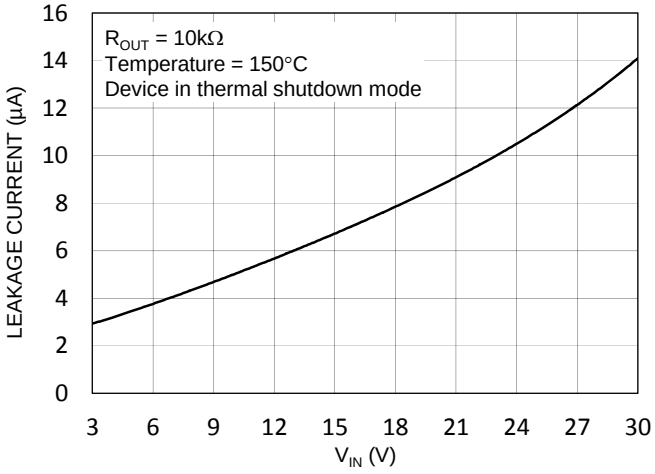


Figure 8. FET Leakage Current (in thermal shutdown) vs. V_{IN}

NEW PRODUCT

Application Information

Over-Voltage Protection

AP9060 protects sensitive circuits by clamping the input voltage to a safe level. In other words, AP9060 conditions the input voltage before presenting it to the sensitive circuitry.

The clamp voltage on AP9060 is set to 11.15V (typically at room temperature). Therefore, the sensitive circuitry will not be exposed to a voltage greater than 11.15V. As a consequence, it is important to ensure that the sensitive ICs that follow AP9060 are safe to operate up to the clamp voltage level (refer to Figure 4 for variation in clamp voltage over temperature).

If the input voltage is below V_{CLAMP}, the PMOS pass transistor in the AP9060 fully turns on and only I x $R_{ON}$is dropped across the FET (where, I is the current drawn by the sensitive ICs). On the other hand, if V_{IN} is greater than the clamp voltage, then AP9060 limits the drive to the FET to ensure that the voltage on VOUT is maintained at the clamp level.

Over-Temperature Protection

As a secondary protection mechanism, AP9060 incorporates an over-temperature shutdown feature. Therefore, if the sensitive circuitry draws too much current either in normal mode or in the clamp mode, AP9060 will turn off the PMOS transistor, provided the junction temperature exceeds the thermal shutdown threshold (THM_{SD}). Thereafter, the device will resume normal operation once the junction temperature falls below $THM_{SD} – THM_{hyst}$.

In the clamp mode, given that any input voltage above V_{CLAMP} is dropped across the pass transistor in AP9060, care must be taken to keep the power dissipation within AP9060 in check by minimising the current drawn in this mode.

Fast Input Transient Protection

AP9060 will also protect the sensitive circuits against fast input transients. Upon detecting a fast transient on VIN, AP9060reduces the drive to the FET in order to minimise the overshoot on VOUT. With 100nF on VOUT, if the voltage on VIN goes from 0V to 30V in 100ns, the output voltage will not peak above V_{pk}.

Reverse Operation

AP9060 supports the USB OTG specification and can operate in the reverse direction as well. Therefore, if the sensitive circuitry drives a voltage on VOUT (V_{OUT_REV}) and a load is connected on VIN(I_{IN_REV}), then AP9060 will turn the FET on in the reverse direction and only I x R_{ON} will be dropped across the device, similar to the forward operation.

However, note that neither over-voltage nor over-temperature protection mechanisms will function in this mode.

Output Capacitor

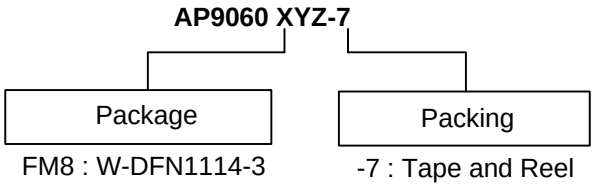
It is recommended to have a capacitor on VOUT in a range between 100nF and 10µF.

Output Resistor

It is recommended to have a resistor on VOUT in a range between 10kΩ and 100kΩ.

NEW PRODUCT

Ordering Information



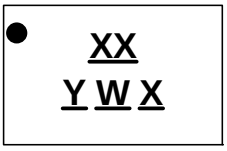
Part Number	Package Code	Packaging (Note 11)	7" Tape and Reel	
			Quantity	Part Number Suffix
AP9060FM8-7	FM8	W-DFN1114-3	3000/Tape & Reel	-7

Note: 11. Pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at http://www.diodes.com/datasheets/ap02001.pdf.

Marking Information

W-DFN1114-3

(Top View)



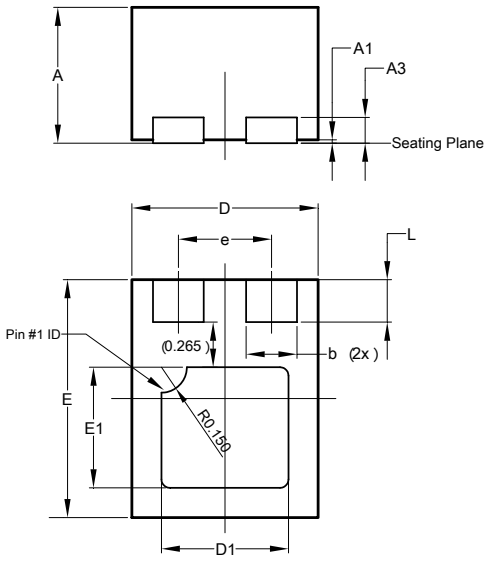
XXX : Identification code
Y : Year 0~9
W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents 52 and 53 week
X : A~Z : Internal Code

Device	Package	Identification Code
AP9060FM8-7	W-DFN1114-3	CZ

NEW PRODUCT

Package Outline Dimensions (All dimensions in mm.)

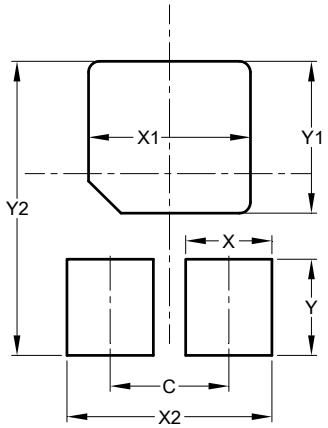
W-DFN1114-3



W-DFN1114-3			
Dim	**Min**	**Max**	**Typ**
A	0.77	0.83	0.80
A1	0	0.05	0.02
A3	-	-	0.152
b	0.25	0.35	0.30
D	1.05	1.15	1.10
D1	0.70	0.80	0.75
e	-	-	0.55
E	1.35	1.45	1.40
E1	0.66	0.76	0.71
L	0.20	0.30	0.25
All Dimensions in mm			

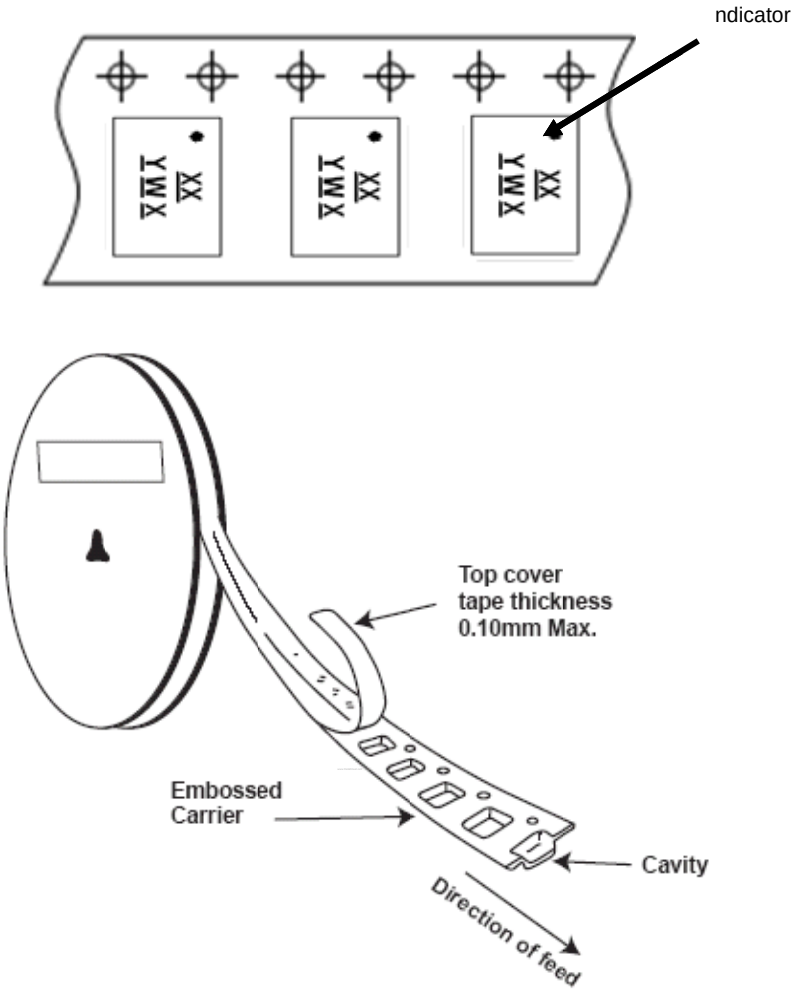
Suggested Pad Layout

W-DFN1114-3



Dimensions	Value (in mm)
C	0.55.
X	0.400
X1	0.750
X2	0.950
Y	0.450
Y1	0.710
Y2	1.375

Tape Orientation (All Dimensions in mm.) (Note 12)



Note: 12. The taping orientation of the other package type can be found on our website at http://www.diodes.com/datasheets/ap02007.pdf

NEW PRODUCT

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