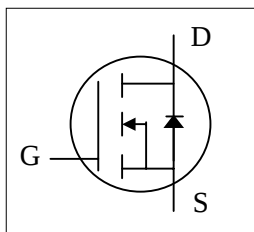




- ▼ Lower Gate Charge
- ▼ Simple Drive Requirement
- ▼ Fast Switching Characteristic

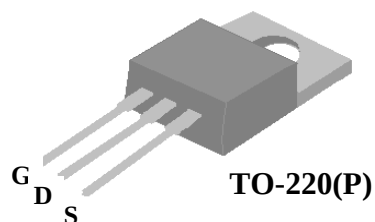


BV_{DSS}	30V
$R_{DS(ON)}$	10m Ω
I_D	53A

Description

Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 package is widely preferred for commercial-industrial power applications and suited for low voltage applications such as DC/DC converters.



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	53	A
$I_D@T_C=100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	33	A
I_{DM}	Pulsed Drain Current ¹	160	A
$P_D@T_C=25^\circ\text{C}$	Total Power Dissipation	44.6	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Value	Units
R_{thj-c}	Maximum Thermal Resistance, Junction-case	2.8	$^\circ\text{C}/\text{W}$
R_{thj-a}	Maximum Thermal Resistance, Junction-ambient	62	$^\circ\text{C}/\text{W}$



AP9408AGP

Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	30	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =30A	-	-	10	mΩ
		V _{GS} =4.5V, I _D =20A	-	-	15	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	1	-	3	V
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =30A	-	30	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =30V, V _{GS} =0V	-	-	10	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V	-	-	±100	nA
Q _g	Total Gate Charge ²	I _D =20A	-	6.5	10.5	nC
Q _{gs}	Gate-Source Charge	V _{DS} =24V	-	1.8	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =4.5V	-	3.7	-	nC
t _{d(on)}	Turn-on Delay Time ²	V _{DS} =15V	-	6	-	ns
t _r	Rise Time	I _D =20A	-	56	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =3.3Ω, V _{GS} =10V	-	15	-	ns
t _f	Fall Time	R _D =0.75Ω	-	3.7	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	600	960	pF
C _{oss}	Output Capacitance	V _{DS} =25V	-	185	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	80	-	pF
R _g	Gate Resistance	f=1.0MHz	-	2.5	3.8	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ²	I _S =30A, V _{GS} =0V	-	-	1.2	V
t _{rr}	Reverse Recovery Time ²	I _S =10A, V _{GS} =0V,	-	23	-	ns
Q _{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	16	-	nC

Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

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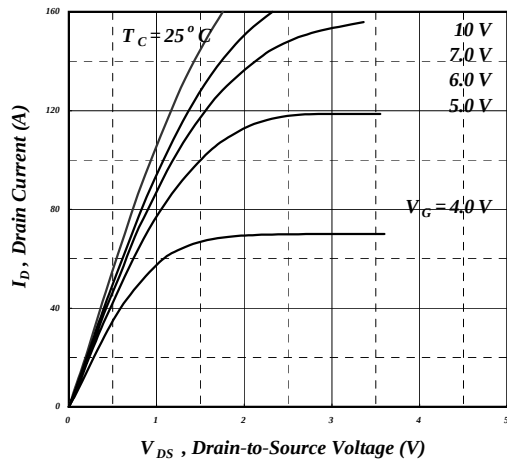


Fig 1. Typical Output Characteristics

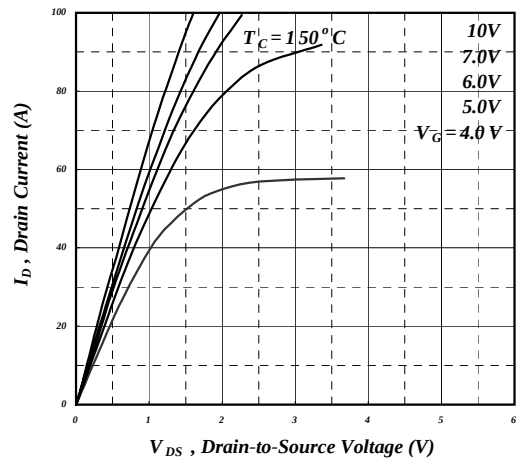


Fig 2. Typical Output Characteristics

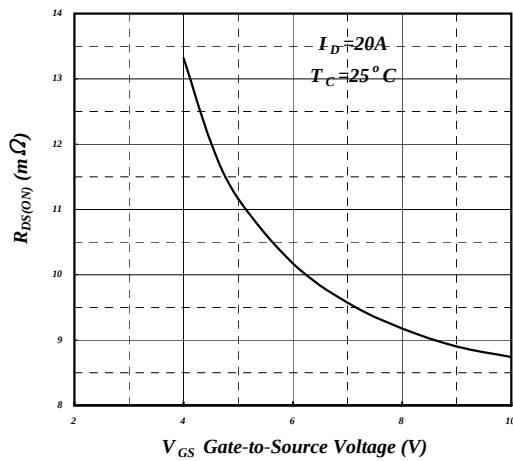


Fig 3. On-Resistance v.s. Gate Voltage

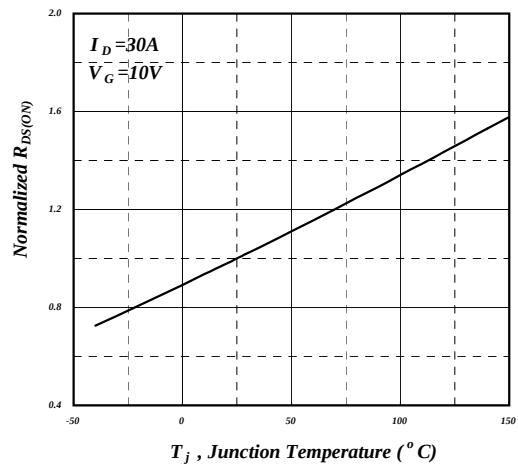


Fig 4. Normalized On-Resistance v.s. Junction Temperature

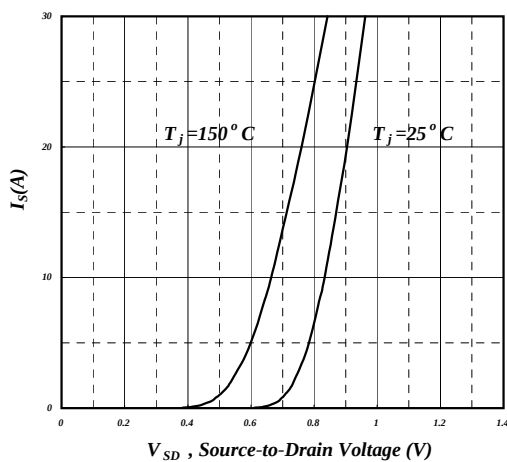


Fig 5. Forward Characteristic of Reverse Diode

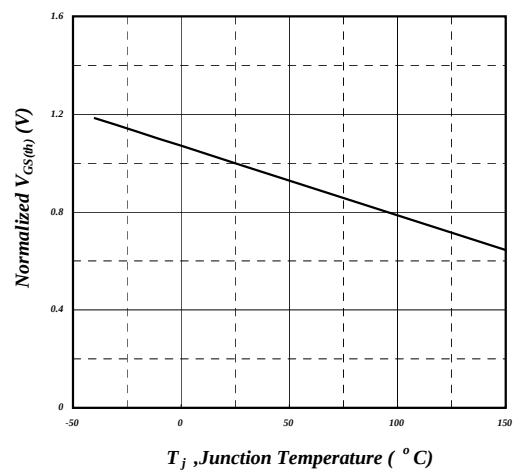


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

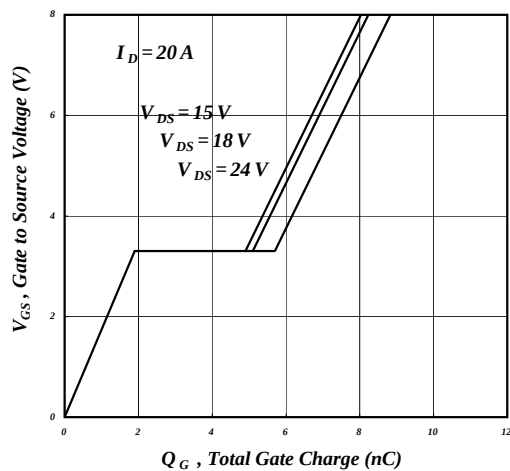


Fig 7. Gate Charge Characteristics

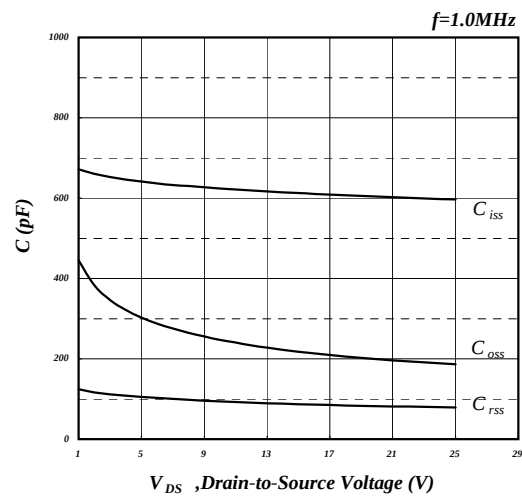


Fig 8. Typical Capacitance Characteristics

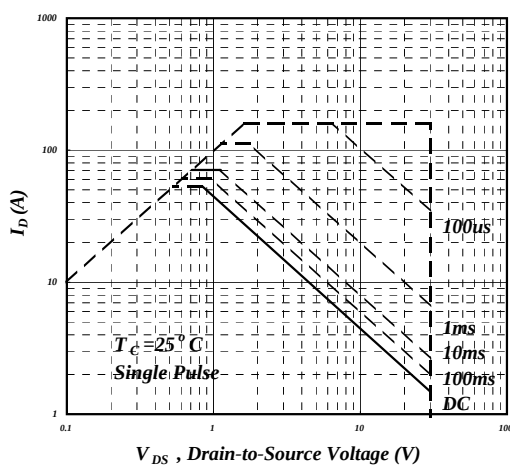


Fig 9. Maximum Safe Operating Area

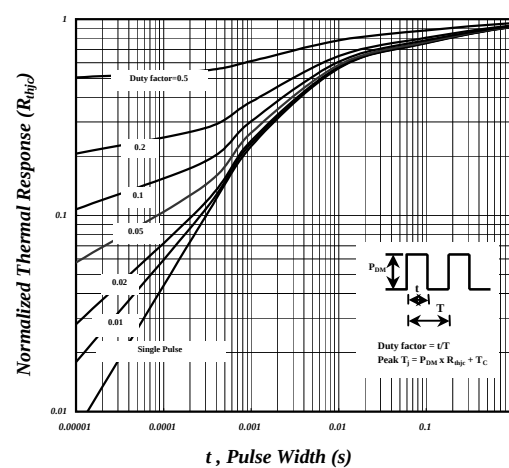


Fig 10. Effective Transient Thermal Impedance

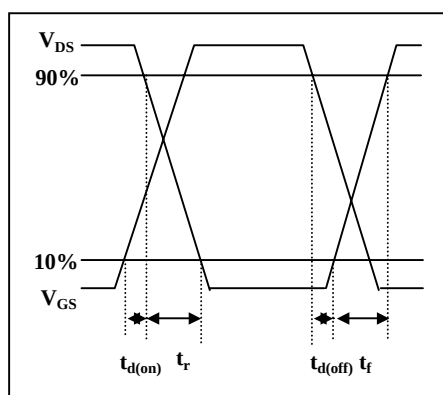


Fig 11. Switching Time Waveform

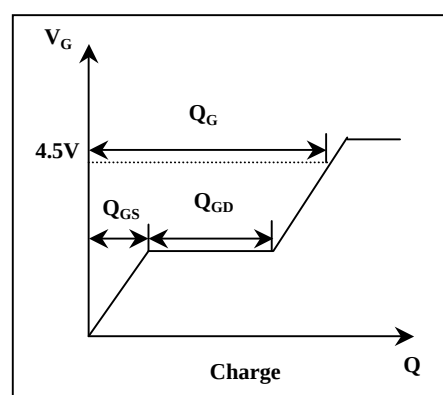


Fig 12. Gate Charge Waveform



Technical drawing of a probe tip showing top and side views with dimensions and a dimension table.

Top View Dimensions:

- E : Total width
- $E1$: Width of the upper section
- ϕ : Diameter of the circular feature
- $L1$: Distance from the top edge to the center of the circular feature
- $L5$: Total height of the upper section
- $D1$: Distance from the top edge to the start of the lower section
- D : Distance from the top edge to the start of the lower section (alternative label)
- $L4$: Distance from the top edge to the start of the lower section (alternative label)
- $b1$: Width of the lower section
- b : Width of the lower section (alternative label)
- e : Width of the lower section (alternative label)

Side View Dimensions:

- A : Total width
- $c1$: Width of the upper section
- L : Total height
- c : Width of the lower section

Dimension Table:

SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	4.40	4.60	4.80
b	0.76	0.88	1.00
D	8.60	8.80	9.00
c	0.36	0.43	0.50
E	9.80	10.10	10.40
L4	14.70	15.00	15.30
L5	6.20	6.40	6.60
D1	5.10 REF.		
c1	1.25	1.35	1.45
b1	1.17	1.32	1.47
L	13.25	13.75	14.25
e	2.54 REF.		
L1	2.60	2.75	2.89
ϕ	3.71	3.84	3.96
E1	7.4 REF.		

1.All Dimensions Are in Millimeters.
2.Dimension Does Not Include Mold Protrusions.

Diagram illustrating the marking layout for a component, specifically a 9408AGP package, showing the relationship between the marking and the component's specifications.

The marking layout includes the following components:

- Part Number:** 9408AGP
- Package Code:** YWWSSS (meet Rohs requirement)
- Logo:** A blue circular logo with a white 'P' inside.
- Date Code (YWWSSS):** YWWSSS

The date code is further defined by the following legend:

- Y :** Last Digit Of The Year
- WW :** Week
- SSS :** Sequence