Creation Date: 2/28/96
Revision: October 6, 1998

AP9A104

64K x 16 CMOS Static RAM

Features

- Fast access times: 10, 12, 15, and 20 ns
- Drives a 50 pF load vs. 30 pF industry standard load
- Multiple center power and ground pins for improved noise immunity
- Low active power
- Low standby power: 11 mW (Max.)
- Individual byte controls for both Read and Write cycles
- TTL and CMOS-compatible inputs and outputs
- Single 5V ±10% power supply
- Packaged in 44-pin, 400-mil SOJ, TSOP (Type II)

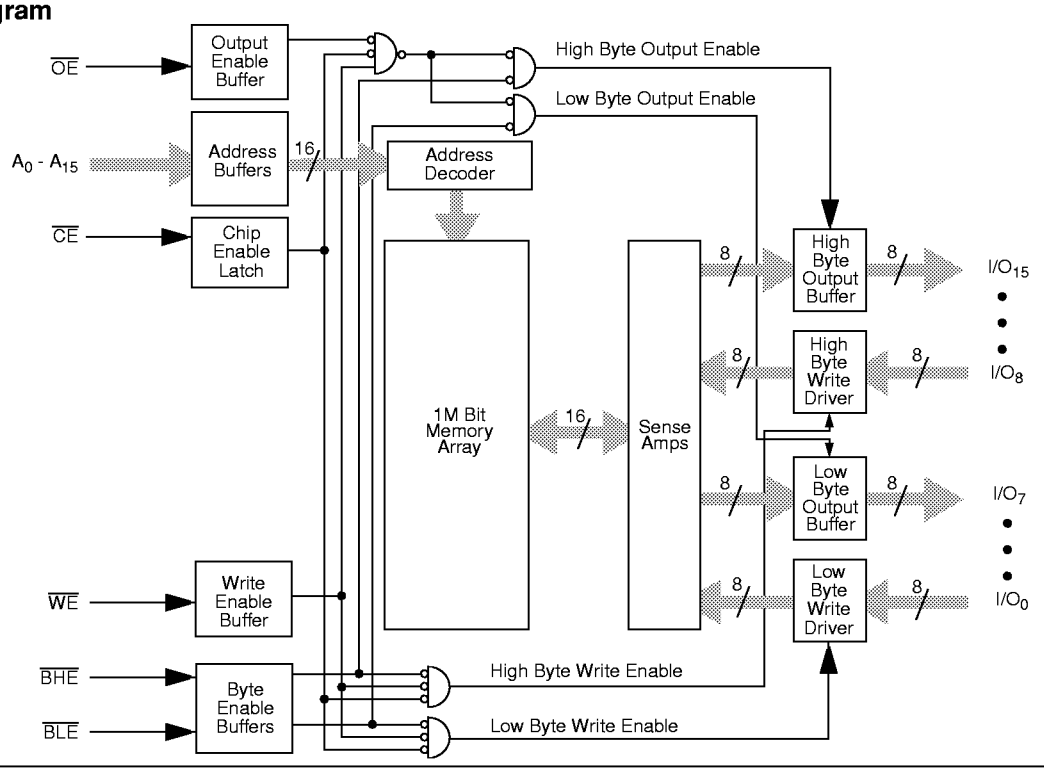
Functional Description

The Aptos AP9A104 is a high-speed, low-power, 64K x 16 CMOS static RAM. It is fabricated using Aptos' high-performance, 0.45µ, CMOS process technology. This highly reliable process, coupled with innovative circuit design techniques yields high performance at low power consumption. Writing to the device is accomplished by bringing Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Enable Low ($\overline{BLE}$) is LOW, then data from I/O_0 through I/O_7 is written into the location specified on the address pins A_0 through A_{15}. If Byte Enable High ($\overline{BHE}$) is LOW, then data from I/O_8 through I/O_{15} is written into the location specified on the address pins A_0 through A_{15}.

Reading from the AP9A104 is accomplished by taking $\overline{CE}$ and $\overline{OE}$ LOW while forcing $\overline{WE}$ HIGH. If $\overline{BLE}$ is LOW, then data from the memory location specified by the address pins will appear on I/O_0 through I/O_7. If $\overline{BHE}$ is LOW, then data from memory will appear on I/O_8 through I/O_{15} (See Truth Table).

This device offers multiple center power and ground pins for improved noise and speed characteristics.

Block Diagram

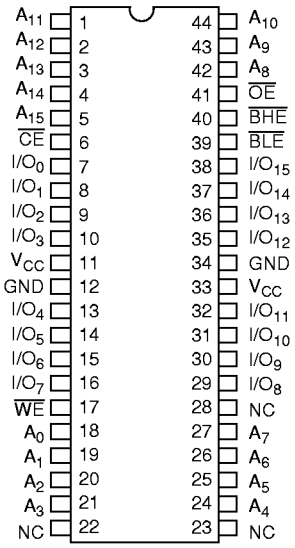


Selection Guide

	AP9A104-10	AP9A104-12	AP9A104-15	AP9A104-20
Maximum Access Time (ns)	10	12	15	20
Maximum Operating Current (mA)	140	130	120	110
Maximum Standby Current (mA)	2	2	2	2

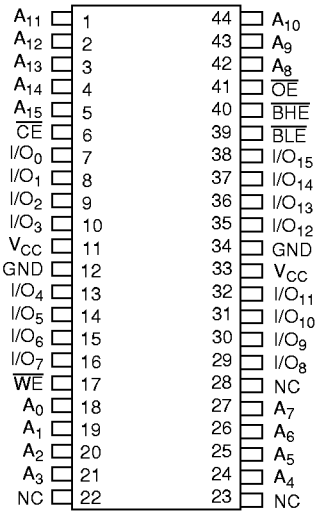
Pin Configurations

44-Pin SOJ
TOP VIEW



9A104-2

44-Pin TSOP
TOP VIEW



9A104-3

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65 °C to +150 °C
Ambient Temperature
with Power Applied ..... -55 °C to +125 °C

V_{CC} Supply Relative to GND .....-1.0 V to +7.0 V
Voltage on any Pin Relative to GND....-0.5 V to V_{CC} +0.5 V
Short Circuit Output Current [1] ..... ± 50 mA
Power Dissipation .....1.0 W

Electrical Characteristics Over the Operating Range ($0°C \le T_A \le 70°$ C, V_{CC} = 5V ±10% Max.)

Symbol	Parameter	Test Conditions	9A104-10		9A104-12		9A104-15		9A104-20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
I_{CC1}	Dynamic Operating Current [2]	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CE} = V_{IL}$, f = fmax		140		130		120		110	mA
I_{CC2}	Static Operating Current [2]	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CE} = V_{IL}$, f = 0		100		100		100		100	mA
I_{SB1}	TTL Standby Current -TTL Inputs	V_{CC} = Max., $V_{IN} = V_{IH}$ or V_{IL}, $\overline{CE} \ge V_{IH}$, f = Max.		20		20		20		20	mA
I_{SB2}	CMOS Standby Current -CMOS Inputs	V_{CC} = Max., $\overline{CE} \ge V_{CC}$ -0.2V, $V_{IN} \ge V_{CC}$ -0.2V or $V_{IN} \le 0.2V$, f = 0		2		2		2		2	mA
I_{LI}	Input Leakage Current	$GND \le V_{IN} \le V_{CC}$	-1	1	-1	1	-1	1	-1	1	µA
I_{LO}	Output Leakage Current	$GND \le V_{OUT} \le V_{CC}$, Output Disabled	-1	1	-1	1	-1	1	-1	1	µA
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4.0 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4		0.4		0.4	V
V_{IH}	Input High Voltage [3]		2.2	V_{CC} +0.5	2.2	V_{CC} +0.5	2.2	V_{CC} +0.5	2.2	V_{CC} +0.5	V
V_{IL}	Input Low Voltage [3]		-0.5	0.8	-0.5	0.8	-0.5	0.8	-0.5	0.8	V

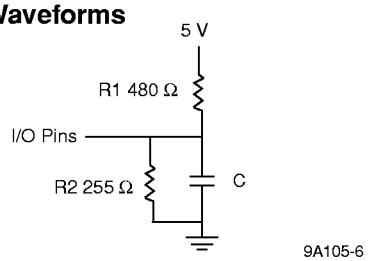
Capacitance [4]

Symbol	Description	Max.	Unit
C_{IN}	Input Capacitance	5	pF
C_{OUT}	I/O Capacitance	5	pF

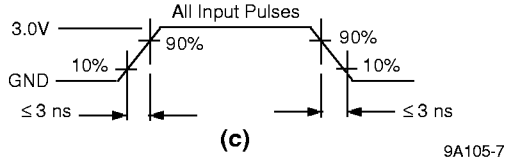
AC Test Loads and Waveforms

(a) C_1= 50 pF INCLUDING JIG AND SCOPE

(b) C_2=5 pF INCLUDING JIG AND SCOPE

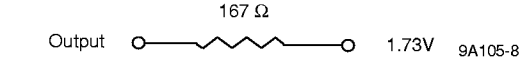


9A105-6



(c)

9A105-7



9A105-8

Notes:

1. No more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open.
3. V_{IL} undershoot = -1.0V where $t=t_{RC}/4$ per cycle. V_{IH} overshoot = V_{CC} +1.0V where $t=t_{RC}/4$ per cycle.
4. Tested initially and after any design or process changes that may effect these parameters.

Switching Characteristics Over the Operating Range [5, 6]

Parameter	Description	9A104-10		9A104-12		9A104-15		9A104-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle [7]										
t_{RC}	Read Cycle Time	10		12		15		20		ns
t_{AA}	Address Access Time		10		12		15		20	ns
t_{OHA}	Output Hold Time	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ Access Time		10		12		15		20	ns
t_{DOE}	$\overline{OE}$ Access Time		5		5		5		6	ns
t_{LZOE} [8]	$\overline{OE}$ to Low-Z Output	0		0		0		0		ns
t_{HZOE} [8]	$\overline{OE}$ to High-Z Output		3		3		5		6	ns
t_{LZCE} [8]	$\overline{CE}$ to Low-Z Output	3		3		3		3		ns
t_{HZCE} [8]	$\overline{CE}$ to High-Z Output		5		6		8		9	ns
t_{PU}	$\overline{CE}$ to Power Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ to Power Down		10		12		15		20	ns
t_{ABE}	Byte Enable Access Time		5		5		5		6	ns
t_{LZBE}	Byte Enable to Output Low-Z	0		0		0		0		ns
t_{HZBE}	Byte Enable to Output High-Z		3		3		5		6	ns
Write Cycle [9]										
t_{WC}	Write Cycle Time	10		12		15		20		ns
t_{SCE}	$\overline{CE}$ to Write End	9		10		12		12		ns
t_{AW}	Address to Set-up Time to Write End	9		10		12		12		ns
t_{HA}	Address Hold to Write End	0		0		0		0		ns
t_{SA}	Address Set-up Time to Write Start	0		0		0		0		ns
t_{PWE1} [10]	$\overline{WE}$ Pulse Width ($\overline{OE}$ =HIGH)	7		8		10		12		ns
t_{PWE2}	$\overline{WE}$ Pulse Width ($\overline{OE}$ =LOW)	10		12		12		15		ns
t_{SD}	Data Set-up to Write End	6		6		7		10		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{HZWE} [8]	$\overline{WE}$ LOW to High-Z Output		5		6		7		9	ns
t_{LZWE} [8]	$\overline{WE}$ HIGH to Low-Z Output	2		2		2		2		ns
t_{BW}	Byte Enable to End of Write	9		10		12		12		ns

Notes:

5. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 V to 3.0 V and output loading specified in AC Test Loads and Waveforms *Figure (a)*, unless otherwise noted..
6. I/O will assume the High-Z state if $\overline{OE} \geq V_{IH}$.
7. $\overline{WE}$ is HIGH for a Read Cycle.
8. Tested with the load in AC Test Loads and Waveforms *Figure (b)*. Transition is measured ±500mV from steady state voltage.
9. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any can be deasserted to terminate the Write. The Data Input Set-up and Hold timing is referenced to the rising or falling edge of the signal that terminates the write.
10. Tested with $\overline{OE}$ HIGH for a minimum of 4 ns before $\overline{WE}$ = LOW to place I/O in High-Z state.
11. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
12. Address is valid prior to, or coincident with, $\overline{CE}$ LOW transitions.
13. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE} and t_{HZBE} is less than t_{LZBE}.
14. $\overline{BHE}$ and $\overline{BLE}$ are held in their asserted state (LOW).

Pin Descriptions

A_0 - A_{15}: Address Inputs

These 16 address inputs select one of the 65,536 16-bit words in the RAM.

$\overline{CE}$: Chip Enable Input

$\overline{CE}$ is asserted LOW. The Chip Enable is asserted LOW to read from or write to the device. If Chip Enable is deasserted, the device is deselected and is in a standby power mode. The I/O pins will be in the high-impedance state when the device is deselected.

$\overline{OE}$: Output Enable Input

The Output Enable input is asserted LOW. If the Output Enable is asserted LOW while $\overline{CE}$ is asserted (LOW) and $\overline{WE}$ is deasserted (HIGH), data from the SRAM will be present on the I/O pins. The I/O pins will be in the high-impedance state when $\overline{OE}$ is deasserted.

$\overline{WE}$: Write Enable Input

The Write Enable input is asserted LOW and controls read and write operations. When $\overline{CE}$ and $\overline{WE}$ are both asserted (LOW) input data present on the I/O pins will be written into the selected memory location.

$\overline{BHE}$, $\overline{BLE}$: Byte Enables

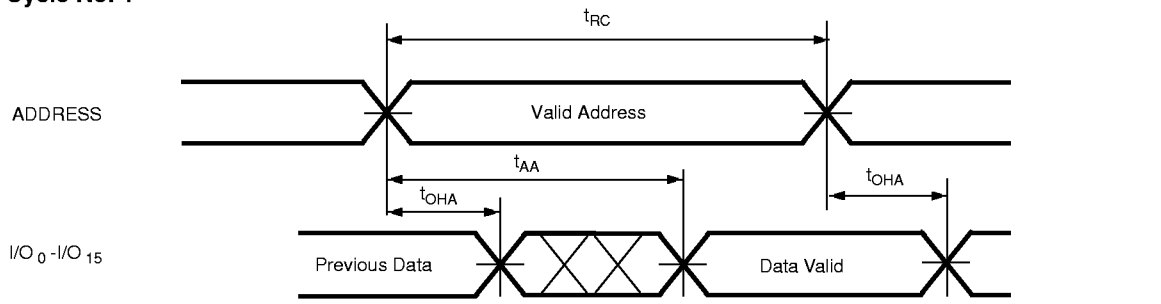
These active LOW inputs allow individual bytes to be written or read. When $\overline{BLE}$ is LOW, data is written or read to the lower byte (I/O_0 - I/O_7). When $\overline{BHE}$ is LOW, data is written or read to the upper byte (I/O_8 - I/O_{15}).

I/O_0 - I/O_{15}: Common Input/Output Pins

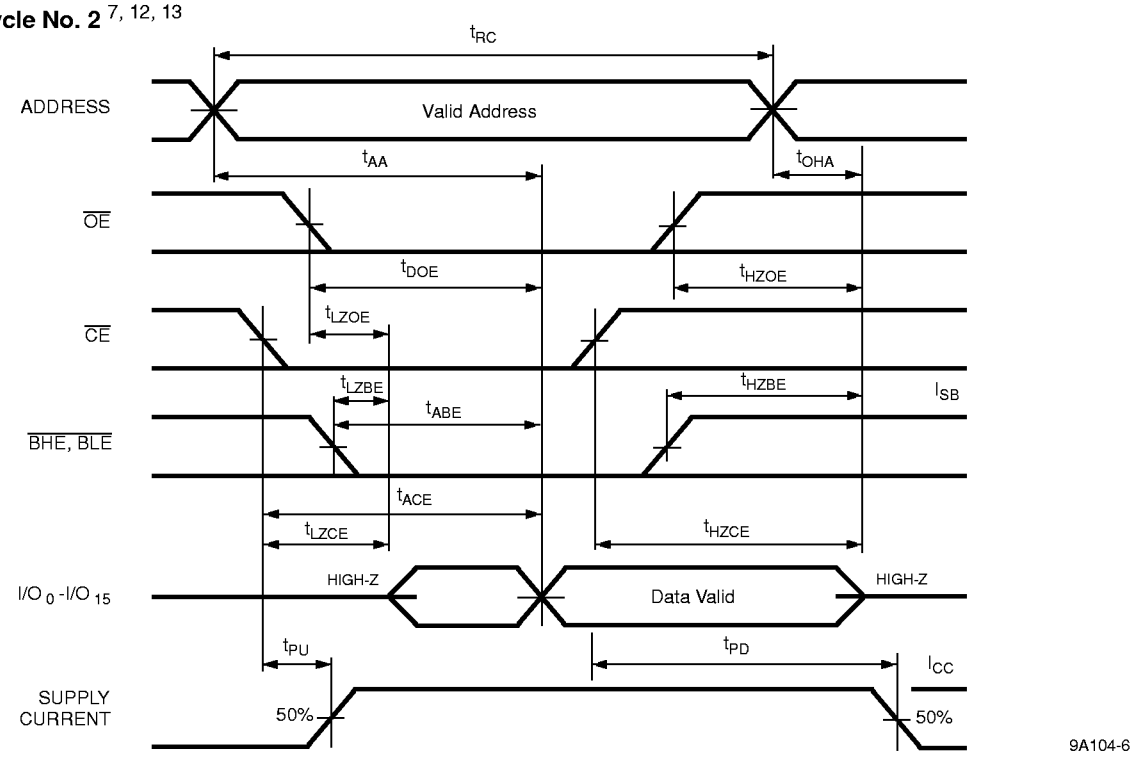
GND: Ground

Switching Waveforms

Read Cycle No. 1 [7, 11, 14]

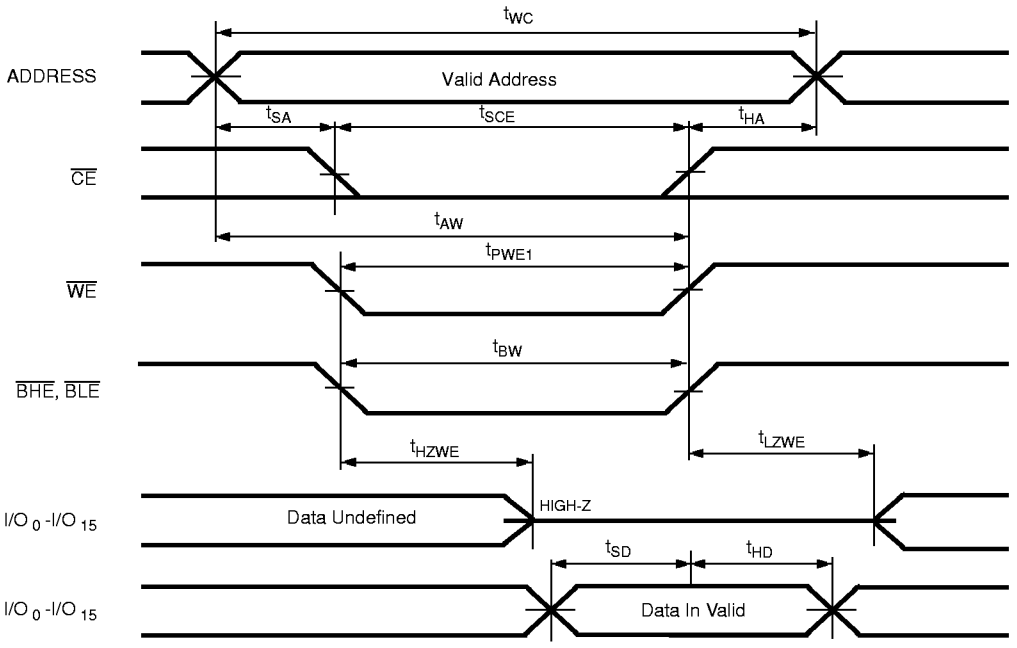


Read Cycle No. 2 [7, 12, 13]

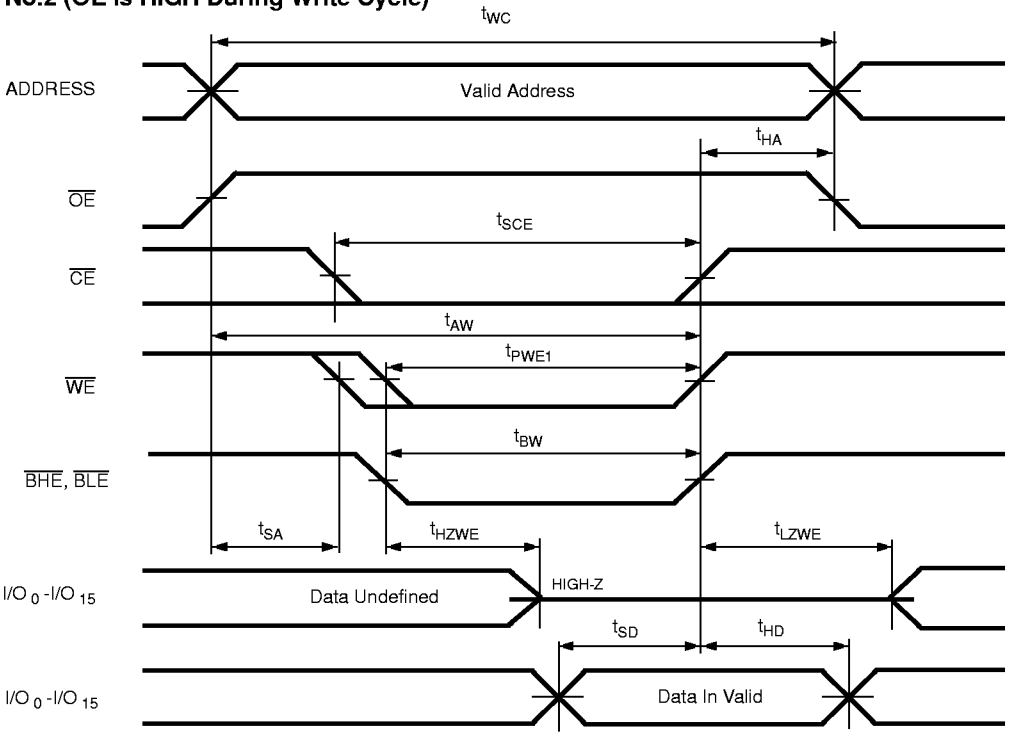


Switching Waveforms (continued)

Write Cycle No.1 ($\overline{CE}$ controlled, $\overline{OE}$ is HIGH or LOW) [9]

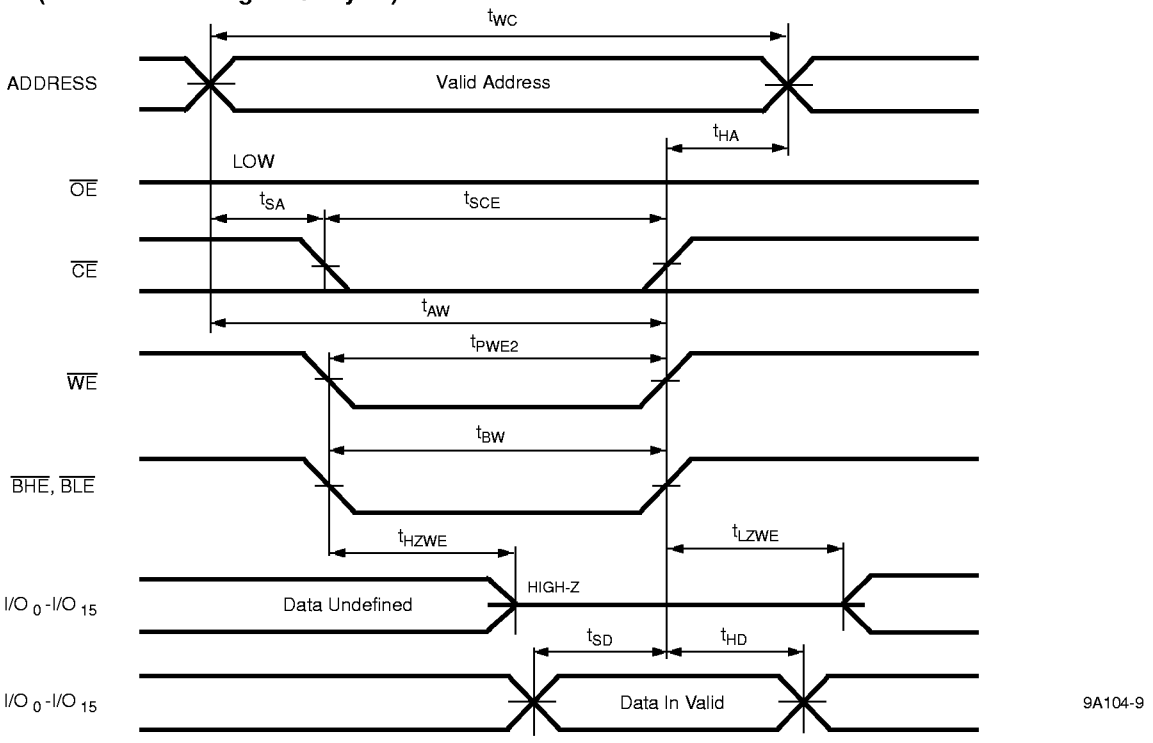


Write Cycle No.2 ($\overline{OE}$ is HIGH During Write Cycle) [9]



Switching Waveforms (continued)

Write Cycle No.3 ($\overline{OE}$ is LOW During Write Cycle) [9]



Truth Table

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O_0 - I/O_7	I/O_8 - I/O_{15}	Power
Standby	H	X	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
Low Byte Read (I/O_0 - I/O_8)	L	L	H	L	H	D_{OUT}	High-Z	I_{CC1}, I_{CC2}
High Byte Read (I/O_9 - I/O_{15})	L	L	H	H	L	High-Z	D_{OUT}	I_{CC1}, I_{CC2}
Word Read (I/O_0 - I/O_{15})	L	L	H	L	L	D_{OUT}	D_{OUT}	I_{CC1}, I_{CC2}
Word Write (I/O_0 - I/O_{15})	L	X	L	L	L	D_{IN}	D_{IN}	I_{CC1}, I_{CC2}
Low Byte Write (I/O_0 - I/O_8)	L	X	L	L	H	D_{IN}	High-Z	I_{CC1}, I_{CC2}
High Byte Write (I/O_9 - I/O_{15})	L	X	L	H	L	High-Z	D_{IN}	I_{CC1}, I_{CC2}
Output Disable	L	H	H	X	X	High-Z	High-Z	I_{CC1}, I_{CC2}
	L	X	X	H	H	High-Z	High-Z	I_{CC1}, I_{CC2}

Ordering Information [10]

Speed	Part Number	Package Name	Package Type	Temperature Range
10	AP9A104-10VC	V44.1	44-Pin Small Outline J-Bend	Commercial
	AP9A104-10TC	T44.1	44-Pin Thin Small Outline Package	Commercial
12	AP9A104-12VC	V44.1	44-Pin Small Outline J-Bend	Commercial
	AP9A104-12TC	T44.1	44-Pin Thin Small Outline Package	Commercial
15	AP9A104-15VC	V44.1	44-Pin Small Outline J-Bend	Commercial
	AP9A104-15TC	T44.1	44-Pin Thin Small Outline Package	Commercial
20	AP9A104-20VC	V44.1	44-Pin Small Outline J-Bend	Commercial
	AP9A104-20TC	T44.1	44-Pin Thin Small Outline Package	Commercial

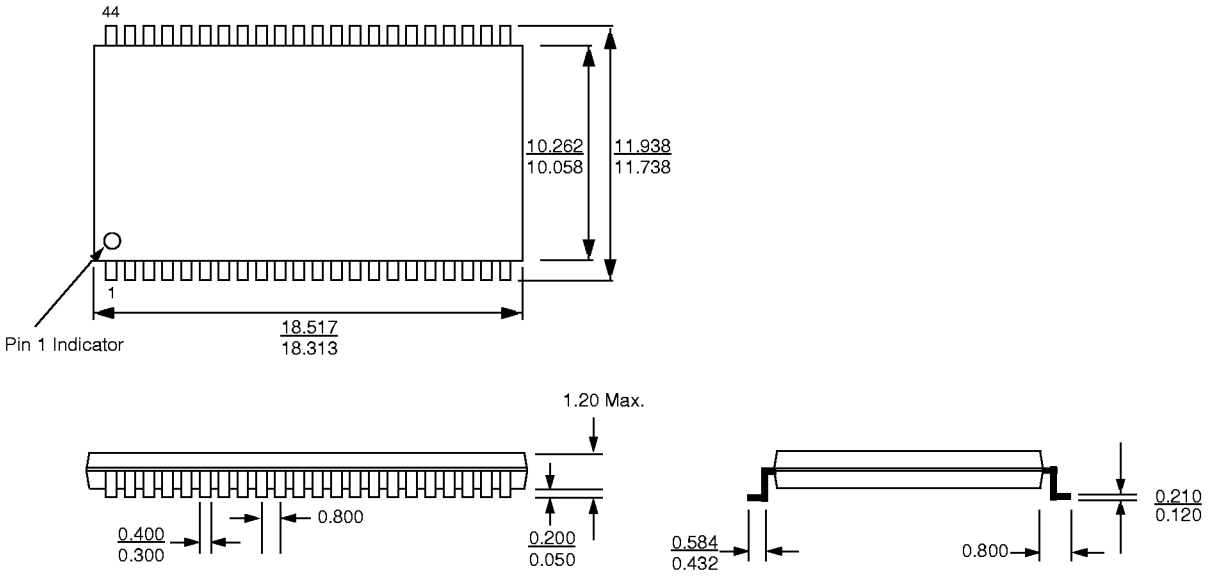
Document # DS-00008-Rev C

Note:

10. For information regarding additional temperature ranges, please contact factory.

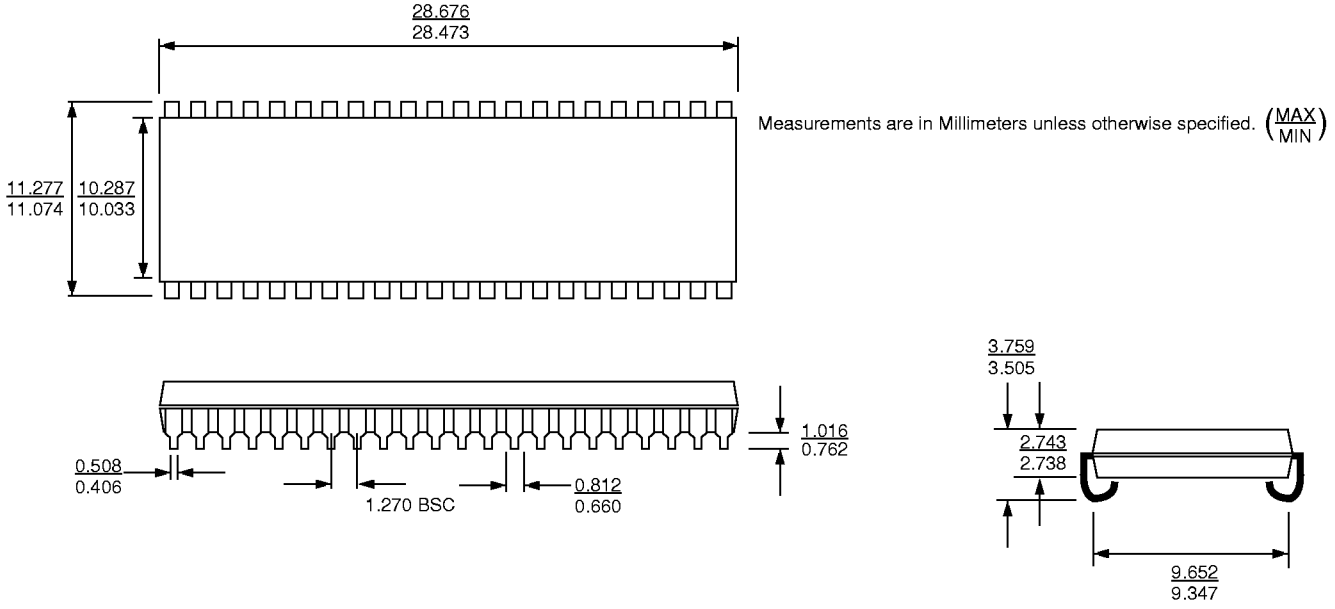
Package Diagrams

T44.1 - 44-Pin (400-Mil) Thin Small Outline Package (TSOP)



Measurements are in Millimeters unless otherwise specified. (MAX / MIN)

V44.1 - 44-Pin (400-Mil) Small Outline J-Bend (SOJ)



Measurements are in Millimeters unless otherwise specified. (MAX / MIN)