Stereo Cap-Free Line Driver

Features

- **Operating Voltage: 2.3V-4.5V**
- **Supply Current**
  - **I_{DD}=5mA at V_{DD}=3.3V**
- **Low Shutdown Current**
  - **I_{DD}=1μA at V_{DD}=3.3V**
- **Ground Reference Output**
  - **No Output Capacitor Required (for DC Blocking)**
  - **Save the PCB Space**
  - **Reduce the BOM Costs**
  - **Improve the Low Frequency Response**
- **Output Voltage Swing Can Reach 2Vrms/Ch into 600Ω at V_{DD}=3.3V**
- **High PSRR: 90dB at 217Hz**
- **Fast Start-Up Time: 500ms**
- **Integrate the De-pop Circuitry**
- **Separate Shutdown Function for Flexible Application**
- **Thermal Protection**
- **Surface-Mount Packaging**
  - **TQFN4x4-20B (with Enhanced Thermal Pad)**
  - **TSSOP-16**
  - **SOP-14**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

- **Set-Top Boxes**
- **CD / DVD Players**
- **LCD TVs**
- **HTIBs (Home Theater in Box)**

General Description

The APA2174 is a stereo, single supply and cap-free line driver, which is available in TQFN4x4-20B, TSSOP-16, and SOP-14 packages.

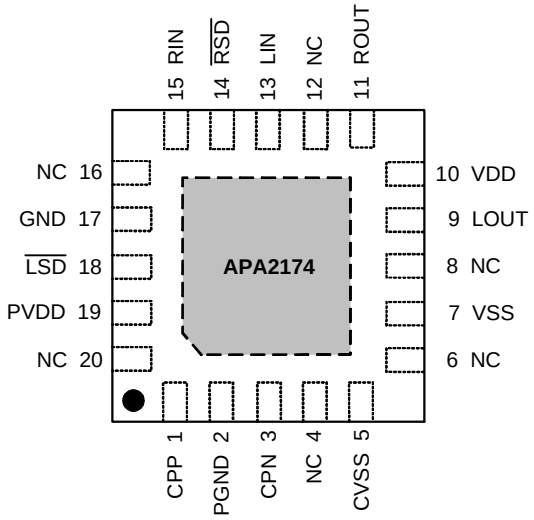
The APA2174 is a ground-reference output and doesn't need the output capacitors for DC blocking. The advantages of eliminating the output capacitor are saving the cost, eliminating component height, and improving the low frequency response.

The external gain setting is recommended using from -1V/V to -10V/V. High PSRR provides increased immunity to noise and RF rectification. The independent shutdown control of APA2174 is for right channel and left channel.

The APA2174 is capable of driving 2Vrms at 3.3V into 600Ω load, and provides thermal protection.

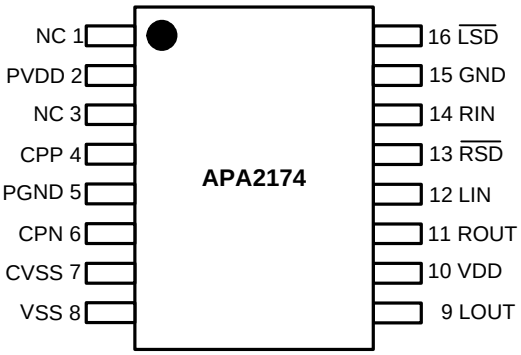
Simplified Application Circuit

Pin Configuration

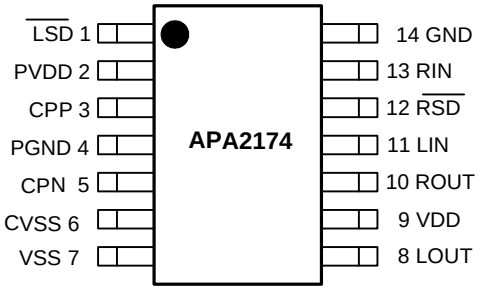


TQFN4x4-20B
(Top View)

=ThermalPad (connected the ThermalPad to GND plane for better heat dissipation)



TSSOP-16
(Top View)



SOP-14
(Top View)

Ordering and Marking Information

APA2174 □□□-□□□

- Assembly Material
- Handling Code
- Temperature Range
- Package Code

Package Code
QB : TQFN4x4-20B O : TSSOP-16 K : SOP-14
Operating Ambient Temperature Range
I : -40 to 85 °C
Handling Code
TR : Tape & Reel
Assembly Material
G : Halogen and Lead Free Device

APA2174 QB :	APA2174 XXXXX	XXXXX - Date Code
APA2174 O :	APA2174 XXXXX	XXXXX - Date Code
APA2174 K :	APA2174 XXXXX	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{PVDD_VDD}	PVDD to VDD Voltage	-0.3 to 0.3	V
V_{PGND_GND}	PGND to GND Voltage	-0.3 to 0.3	
V_{DD}	Supply Voltage (VDD and PVDD to GND and PGND)	-0.3 to 5.5	
$V_{control}$	Input Voltage ($\overline{RSD}$ and $\overline{LSD}$ to GND)	GND-0.3 to V_{DD}+0.3	V
V_{SS}	VSS and CVSS to GND and PGND Voltage	-5.5 to 0.3	
V_{OUT}	ROUT and LOUT to GND Voltage	V_{SS}-0.3 to V_{DD}+0.3	
V_{CPP}	CPP to PGND Voltage	PGND-0.3 to V_{DD}+0.3	
V_{CPN}	CPN to PGND Voltage	V_{SS}-0.3 to PGND+0.3	
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-65 to +150	
T_{SDR}	Maximum Soldering Temperature Range, 10 Seconds	260	
P_D	Power Dissipation	Internally Limited	W

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Thermal Resistance - Junction to Ambient (Note 2) TQFN4x4-20B TSSOP-16 SOP-14	 45 100 110	°C/W
θ_{JC}	Thermal Resistance - Junction to Case (Note 3) TQFN4x4-20B	 8	°C/W

Note 2: Please refer to " Layout Recommendation", the Thermal Pad on the bottom of the IC should soldered directly to the PCB's Thermal Pad area that with several thermal vias connect to the ground plan, and the PCB is a 2-layer, 5-inch square area with 2oz copper thickness.

Note 3: The case temperature is measured at the center of the Thermal Pad on the underside of the TQFN4x4-20B package.

Recommended Operating Conditions

Symbol	Parameter		Range		Unit
			Min.	Max.	
V_{DD}	Supply Voltage		2.3	4.5	V
V_{IH}	High Level Threshold Voltage	$\overline{RSD}$, $\overline{LSD}$	1	-	
V_{IL}	Low Level Threshold Voltage	$\overline{RSD}$, $\overline{LSD}$	-	0.35	
R_i	Input Resistance		1	47	kΩ
R_f	Feedback Resistance		4.7	100	
R_L	Load Resistance		500	-	Ω
C_L	Maximum Capacitive Load		-	400	pF
T_A	Operating Ambient Temperature Range		-40	85	°C
T_J	Operating Junction Temperature Range		-40	125	

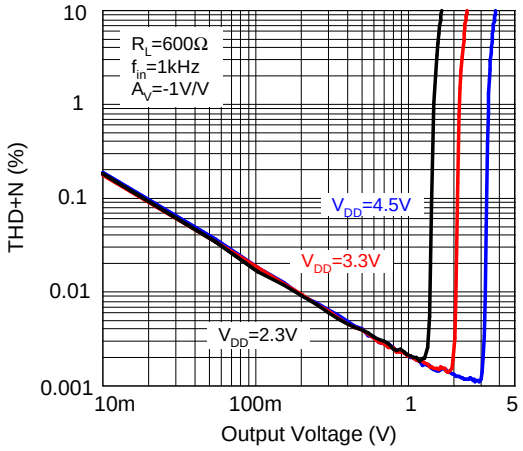
Electrical Characteristics

V_{DD}=3.3V, V_{GND}=V_{PGND}=0V, $V_{\overline{RSD}}$=$V_{\overline{LSD}}$=V_{DD}, C_{CPF}=C_{CPO}=2.2µF, C_i=1µF, R_i=R_f=10kΩ, T_A=25°C (unless otherwise noted)

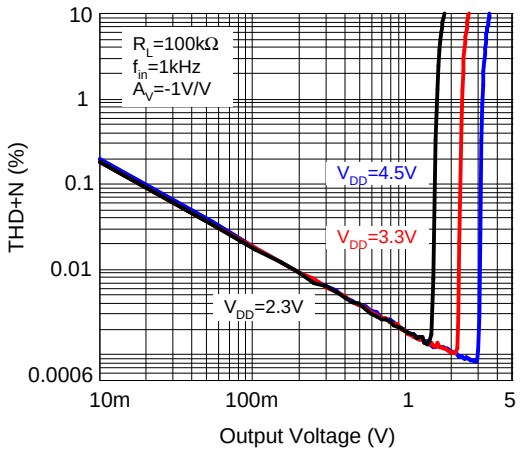
Symbol	Parameter	Test Conditions	APA2174			Unit
			Min.	Typ.	Max.	
I_{DD}	Supply Current		-	5	10	mA
I_{SD}	Shutdown Current	$V_{\overline{RSD}}$=$V_{\overline{LSD}}$=0V	-	1	5	µA
I_i	Input current	$\overline{RSD}$, $\overline{LSD}$	-	0.1	-	µA
CHARGE PUMP						
f_{OSC}	Switching Frequency		400	500	600	kHz
R_{eq}	Equivalent Resistance		-	21	25	Ω
DRIVERS						
A_{VO}	Open Loop Voltage Gain		80	100	-	dB
G_{BW}	Unity Gain Bandwidth		8	10	-	MHz
R_O	Output Resistance	I_O=10mA	-	-	100	Ω
V_{SR}	Slew Rate		-	2.5	-	V/µs
V_{OS}	Output Offset Voltage	V_{DD}=2.3V to 4.5V, R_L = 600Ω	-8	-	8	mV
V_n	Noise Output Voltage		-	10	20	µVrms
PSRR	Power Supply Rejection Ratio	V_{DD}=2.3V to 4.5V, V_{rr}=200mVrms f_{in}= 217Hz f_{in}= 1kHz f_{in}= 20kHz	-	 -90 -90 -65	 -70 -70 -60	dB
$T_{start-up}$	Start-up Time		-	500	-	µs
V_{ESD}	ESD Protection	OUTR, OUTL	-	8	-	kV
V_O	Output Voltage (Stereo, in Phase)	THD+N=1%, f_{in}=1kHz R_L=600Ω R_L=100kΩ	2	 2.1 2.3	-	Vrms
		V_{DD}=4.5V, THD+N=1%, f_{in}=1kHz R_L=600Ω R_L=100kΩ	-	 2.9 3.2	-	
THD+N	Total Harmonic Distortion Plus Noise	V_O=2Vrms, R_L=600Ω f_{in}=20Hz f_{in}=1kHz f_{in}=20kHz	-	 0.020 0.002 0.020	-	%
Crosstalk	Channel Separation	V_O=2Vrms, R_L=600Ω f_{in}=20Hz f_{in}=1kHz f_{in}=20kHz	-	 100 90 70	-	dB
S/N	Signal to Noise Ratio	V_O=2Vrms, R_L=600Ω With A-weighting Filter	-	105	-	

Typical Operating Characteristics

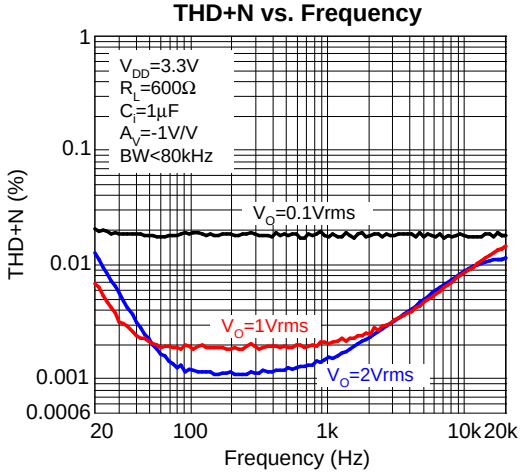
THD+N vs. Output Voltage



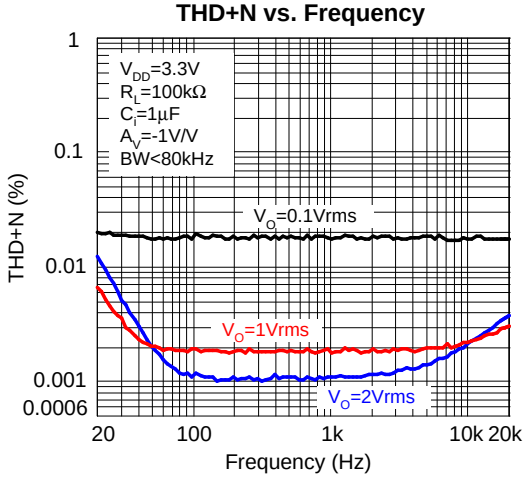
THD+N vs. Output Voltage



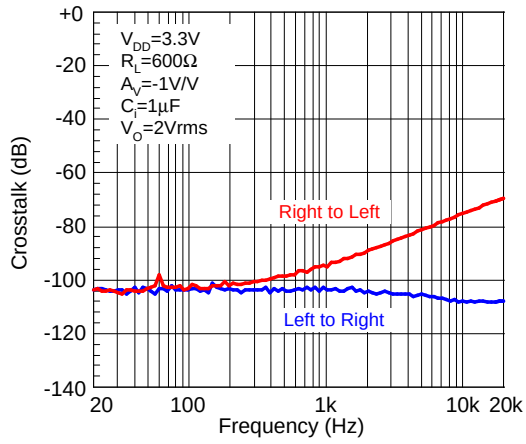
THD+N vs. Frequency



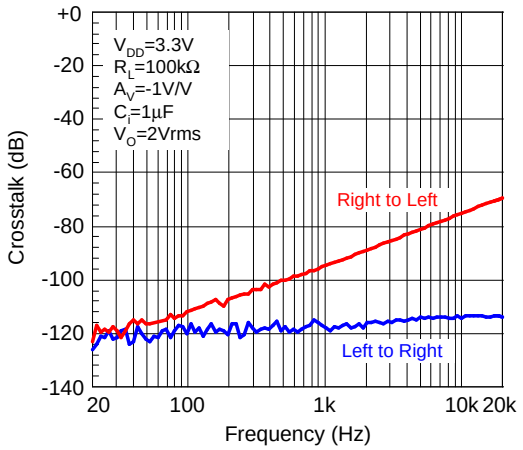
THD+N vs. Frequency



Crosstalk vs. Frequency

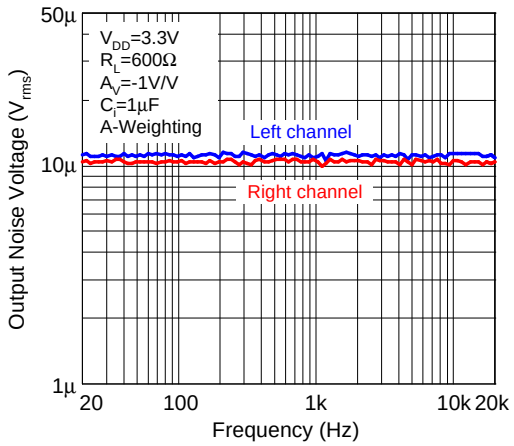


Crosstalk vs. Frequency

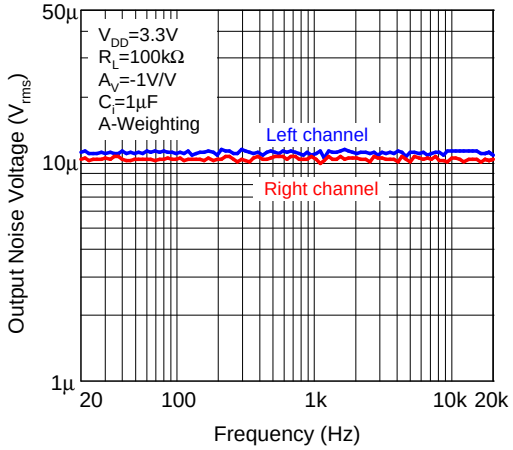


Typical Operating Characteristics (Cont.)

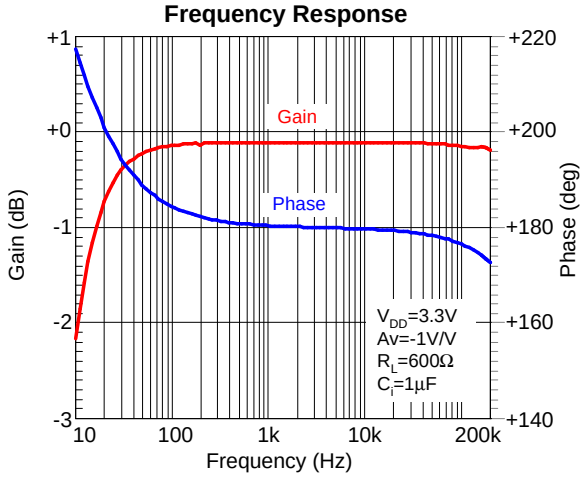
Output Noise Voltage vs. Frequency



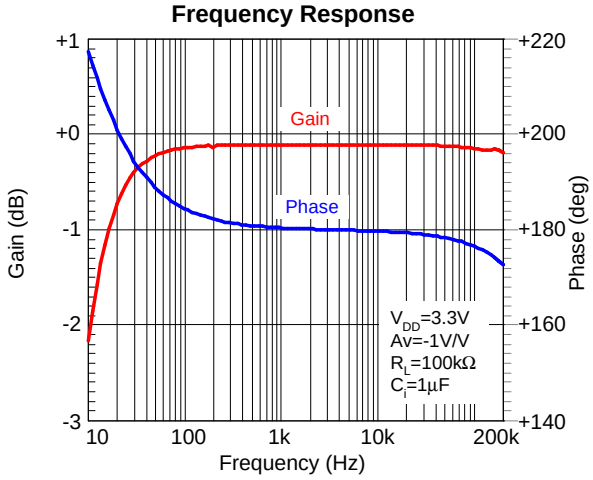
Output Noise Voltage vs. Frequency



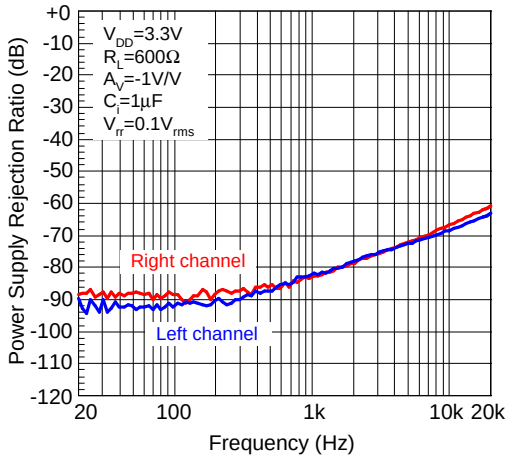
Frequency Response



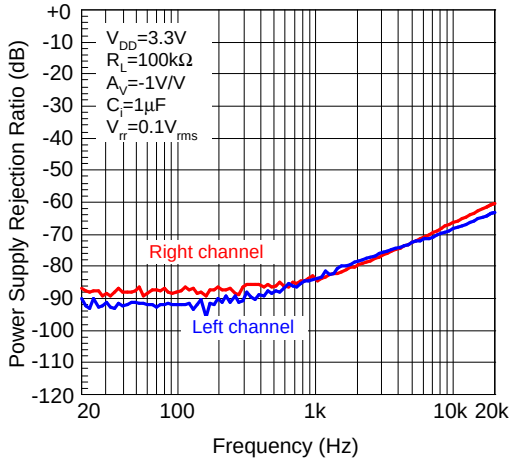
Frequency Response



PSRR vs. Frequency

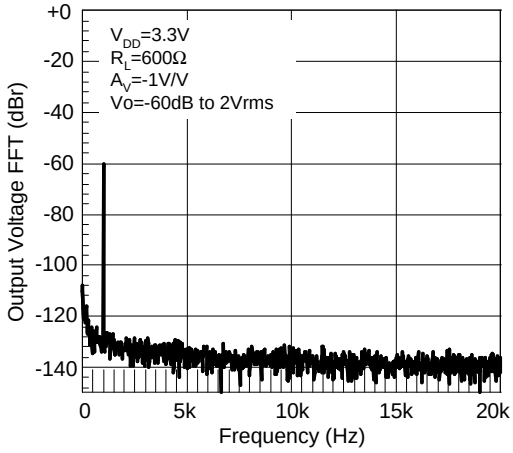


PSRR vs. Frequency

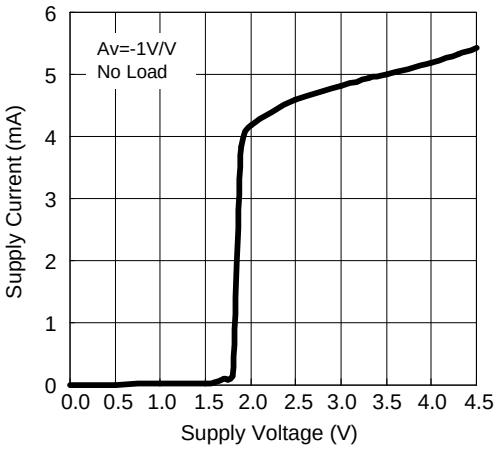


Typical Operating Characteristics (Cont.)

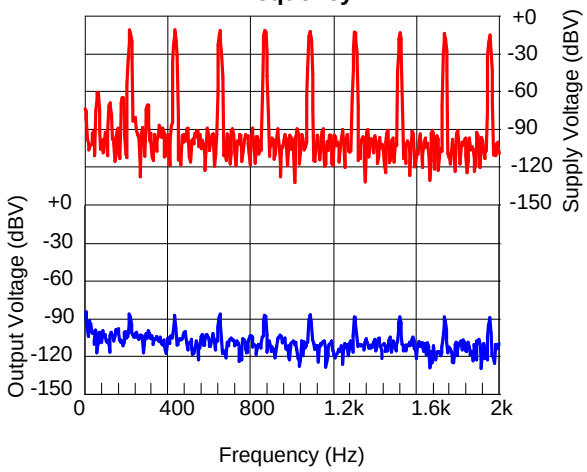
Output Voltage FFT vs. Frequency



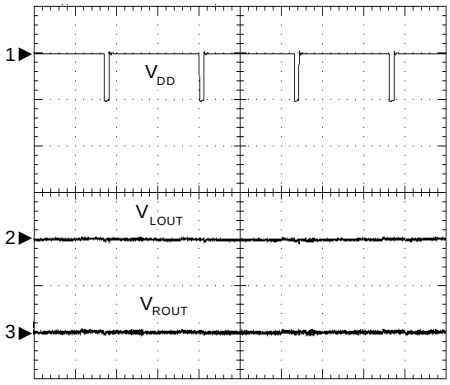
Supply Current vs. Supply Voltage



GSM Power Supply Rejection vs. Frequency



GSM Power Supply Rejection vs. Time

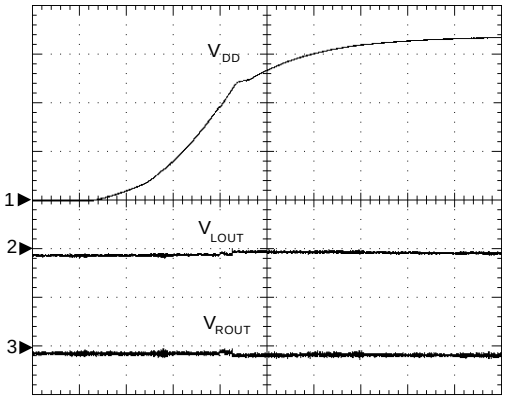


CH1: V_{DD}, 500mV/Div, DC, Offset=3.3V
CH2: V_{LOUT}, 20mV/Div, DC
CH3: V_{ROUT}, 20mV/Div, DC
TIME:2ms/Div

Operating Waveforms

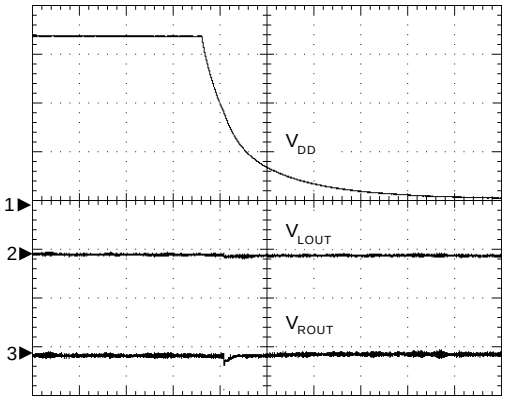
Refer to the typical application circuit. The test condition is V_{DD}=$V_{\overline{SD}}$=3.3V, R_L=600Ω, T_A= 25°C, unless otherwise specified.

Output Transient at Power On



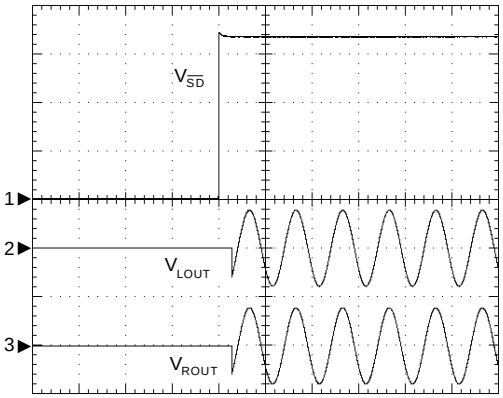
CH1: V_{DD}, 1V/Div, DC
CH2: V_{LOUT}, 20mV/Div, DC
CH3: V_{ROUT}, 20mV/Div, DC
TIME:2ms/Div

Output Transient at Power Off



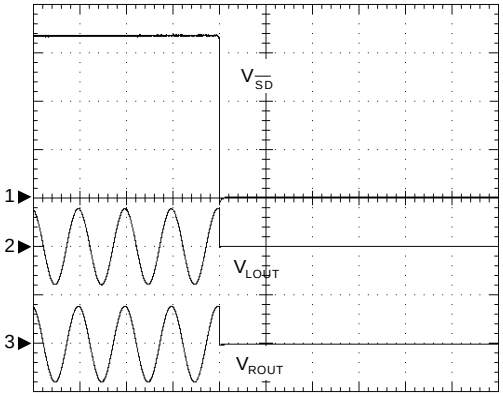
CH1: V_{DD}, 1V/Div, DC
CH2: V_{LOUT}, 20mV/Div, DC
CH3: V_{ROUT}, 20mV/Div, DC
TIME:2ms/Div

Shutdown Release



CH1: $V_{\overline{SD}}$, 1V/Div, DC
CH2: V_{LOUT}, 1V/Div, DC
CH3: V_{ROUT}, 1V/Div, DC
TIME:2ms/Div

Load Transient Response

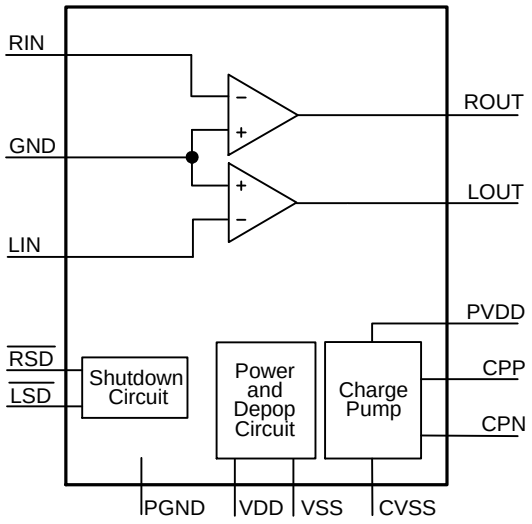


CH1: $V_{\overline{SD}}$, 1V/Div, DC
CH2: V_{LOUT}, 1V/Div, DC
CH3: V_{ROUT}, 1V/Div, DC
TIME:2ms/Div

Pin Description

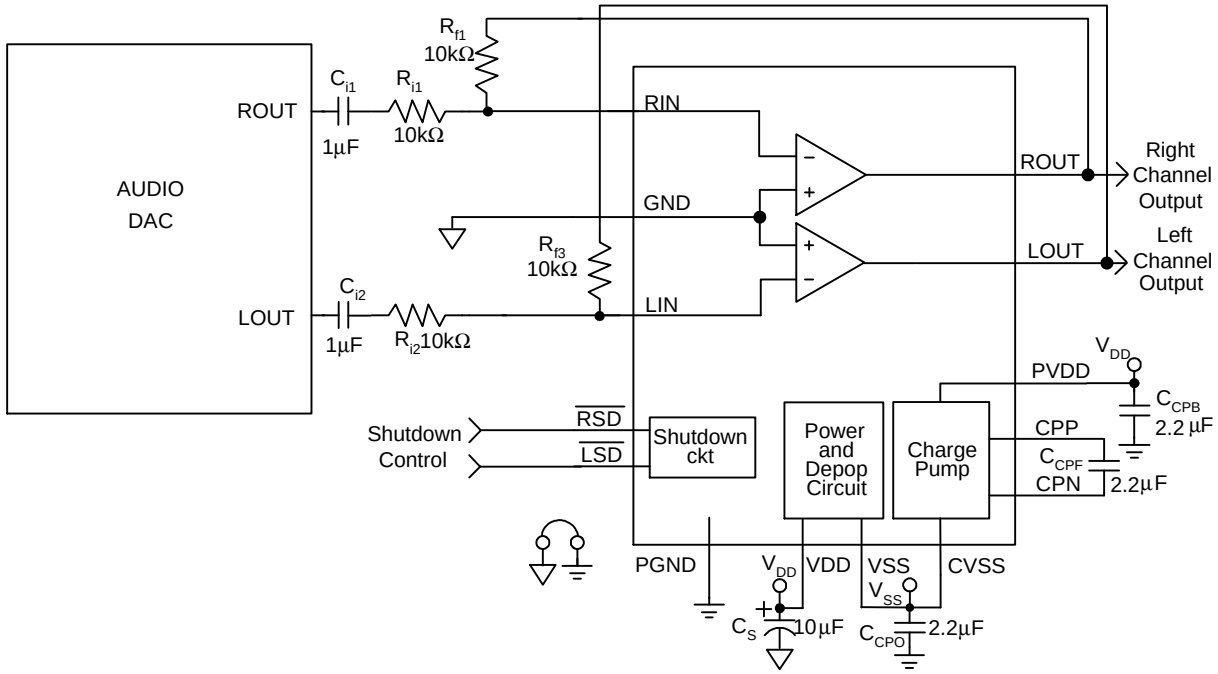
PIN				I/O/P	FUNCTION
NO.			NAME		
TQFN4x4-20B	TSSOP-16	SOP-14			
1	4	3	CPP	I/O	Charge pump flying capacitor positive connection.
2	5	4	PGND	P	Charge pump's ground.
3	6	5	CPN	I/O	Charge pump flying capacitor negative connection.
4,6,8,12, 16,20	1,3	-	NC	-	No Connection.
5	7	6	CVSS	O	Charge pump output, connect to the "VSS".
7	8	7	VSS	P	Line Driver negative power supply.
9	9	8	LOUT	O	Left channel output for line driver.
10	10	9	VDD	P	Power supply.
11	11	10	ROUT	O	Right channel output for line driver.
13	12	11	LIN	I	Left channel input terminal.
14	13	12	$\overline{RSD}$	I	Right channel shutdown mode control input signal, pull low for shutdown the right channel line driver.
15	14	13	RIN	I	Right channel input terminal.
17	15	14	GND	P	Ground connection for circuitry.
18	16	1	$\overline{LSD}$	I	Left channel shutdown mode control input signal, pull low for shutdown the left channel line driver.
19	2	2	PVDD	P	Charge pump's power supply.

Block Diagram

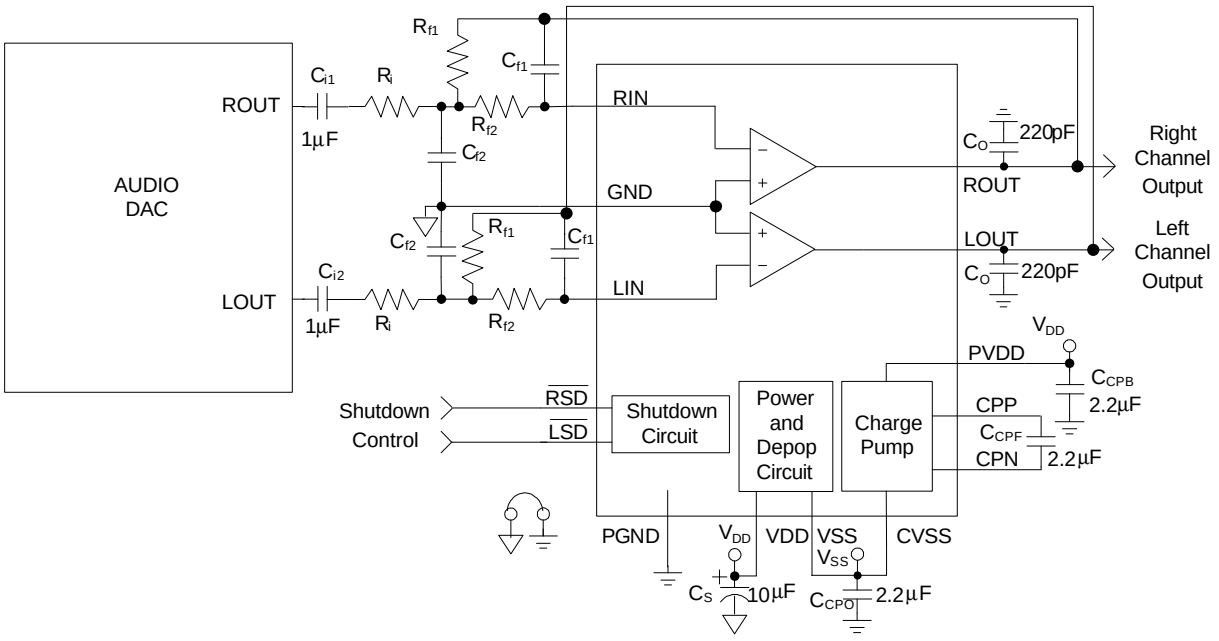


Typical Application Circuit

1. Inverting Amplifier



2. Secind-Order Active Low-Pass Filter



Function Description

Line Driver Operation

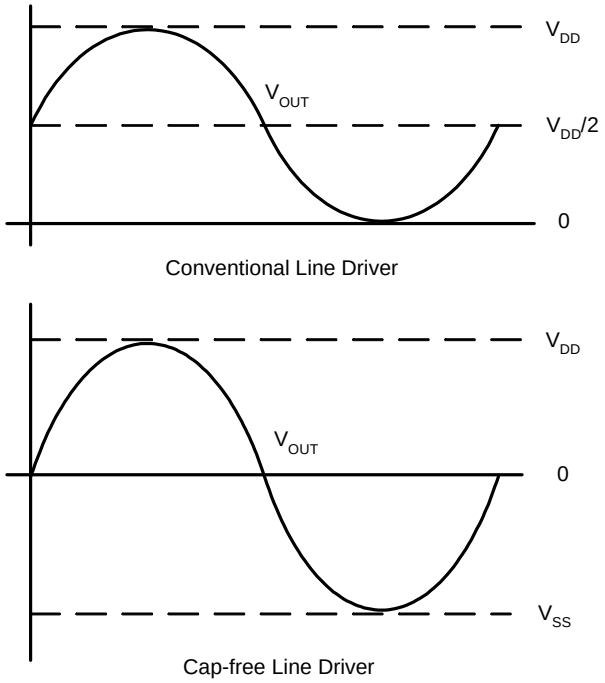


Figure 1: Cap-free Line Driver's Operation

The APA2174's line drivers use a charge pump to invert the positive power supply (V_{DD}) to negative power supply (V_{SS}), see figure1. The line drivers operate at this bipolar power supply (V_{DD} and V_{SS}) and the outputs reference refers to the ground. This feature eliminates the output capacitor that is using in conventional single-ended line drive amplifier. Compare with the single power supply amplifier, the power supply range has almost doubled.

Thermal Protection

The thermal protection circuit limits the junction temperature of the APA2174. When the junction temperature exceeds T_J = +150°C, a thermal sensor turns off the driver, allowing the devices to cool. The thermal sensor allows the driver to start-up after the junction temperature down about 125°C. The thermal protection is designed with a 25°C hysteresis to lower the average T_J during continuous thermal overload conditions, increasing lifetime of the ICs.

Shutdown Function

In order to reduce power consumption while not in use, the APA2174 contains two shutdown controllers to allow either channel being independent and externally turns off the amplifier bias circuitry. $\overline{LSD}$ controls the left channel and $\overline{RSD}$ controls the right channel. This shutdown feature turns the amplifier off when logic low is placed on the $\overline{RSD}$ and $\overline{LSD}$ pins for the APA2174. The trigger point between a logic high is 1.0V and logic low level is 0.35V. It is recommended to switch between ground and the supply voltage V_{DD} to provide maximum device performance. By switching the both $\overline{RSD}$ and $\overline{LSD}$ pins to a low level, the amplifier enters a low-consumption current circumstance, charge pump is disabled, and I_{DD} for the APA2174 is in shutdown mode. The charge pump is enabled once either $\overline{RSD}$ or $\overline{LSD}$ pin is pulled to high. In normal operating, the APA2174's $\overline{RSD}$ and $\overline{LSD}$ pins should be pulled to a high level to keep the IC out of the shutdown mode. The $\overline{RSD}$ and $\overline{LSD}$ pins should be tied to a definite voltage to avoid unwanted circumstance change.

Application Information

Second Order Low Pass Filter

Using the APA2174 as a second order, Multi-Feedback active Butterworth filter for audio DACs. The topology is like the figure 2.

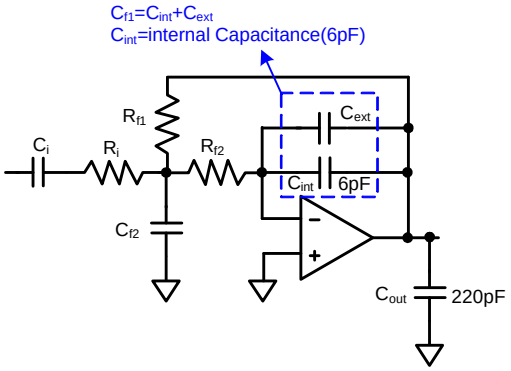


Figure 2: Active Butterworth Filter

Table 1: The recommended components' value.

A_V	High Pass	Low Pass	C_i	C_{f1}	C_{f2}	R_i	R_{f1}	R_{f2}
-1V/V	16Hz	40kHz	1μF	100pF	680pF	10kΩ	10kΩ	24kΩ
-1.5V/V	19Hz	40kHz	1μF	68pF	680pF	8.2kΩ	12kΩ	30kΩ
-2V/V	11Hz	40kHz	1μF	33pF	330pF	15kΩ	30kΩ	47kΩ
-2V/V	11Hz	30kHz	1μF	47pF	470pF	15kΩ	30kΩ	43kΩ
-3.3V/V	12Hz	30kHz	1μF	33pF	470pF	13kΩ	43kΩ	43kΩ
-10V/V	15Hz	30kHz	2.2μF	22pF	1nF	4.7kΩ	47kΩ	27kΩ

The overall gain is:

$$A_V = -\frac{R_{f1}}{R_i} \quad (1)$$

The high pass filter's cutoff frequency is:

$$f_{C(highpass)} = \frac{1}{2\pi R_i C_i} \quad (2)$$

The low pass filter's cutoff frequency is:

$$f_{C(lowpass)} = \frac{1}{2\pi\sqrt{R_{f1}R_{f2}C_{f1}C_{f2}}} \quad (3)$$

Input Capacitor, C_i

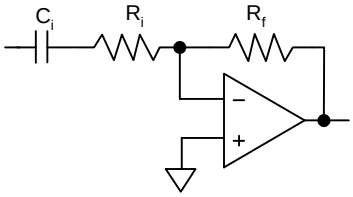


Figure 3: Typical Application Circuit

In the typical application, an input capacitor, C_i, is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, C_i and the minimum input impedance R_i from a high-pass filter with the corner frequency are determined in the following equation:

$$f_{C(highpass)} = \frac{1}{2\pi R_i C_i} \quad (4)$$

The value of C_i must be considered carefully because it directly affects the low frequency performance of the circuit. R_i is the external input resistance that typical value is 10kΩ and the specification calls for a flat bass response down to 20Hz. Equation is reconfigured as below:

$$C_i = \frac{1}{2\pi R_i f_{C(highpass)}} \quad (5)$$

When the input resistance variation is considered, the C_i is 0.8μF, so a value in the range of 1μF to 2.2μF would be chosen. A further consideration for this capacitor is the leakage path from the input source through the input network (R_i + R_f, C_i) to the load.

This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the negative side of the capacitor should face the amplifiers' input in most applications because the DC level of the amplifiers' input is held at GND. Please note that it is important to confirm the capacitor polarity in the application.

Input Resistor, R_i

The gain of the APA2174 is be set by the external input resistor (R_i) and external feedback resistor (R_f). Please see the figure 3.

Application Information (Cont.)

Input Resistor, R_i (Cont.)

$$Gain(A_V) = \frac{R_f}{R_i} \quad (6)$$

The external gain setting is recommended using from -1V/V to -10V/V, and the R_i is in the range from 1kΩ to 47kΩ. It's recommended to use 1% tolerance resistor or better. Keep the input trace as short as possible to limit the noise injection. The gain is recommended to set -1V/V, and R_i is 10kΩ, and R_f is 10kΩ.

Feedback Resistor, R_f

Refer the figure 3, the external gain is setting by R_i and R_f; and the gain setting is recommended using from -1V/V to -10V/V. The R_f is in the range from 4.7kΩ to 100kΩ. It's recommended to use 1% tolerance resistor or better.

Power Supply Decoupling, C_s

The APA2174 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD+N) is as low as possible. Power supply decoupling also prevents the oscillations being caused by long lead length between the amplifier and the speaker.

The optimum decoupling is achieved by using two different types of capacitors that target on different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series- resistance (ESR) ceramic capacitor, typically 0.1µF, is placed as close as possible to the device VDD and PVDD lead for the best performance. For filtering lower frequency noise signals, a large aluminum electrolytic capacitor of 10µF or greater placed near the audio power amplifier is recommended.

Charge Pump Bypass Capacitor, C_{CPB}

The bypass capacitor (CCPB) relates with the charge pump switching transient. The capacitor's value is same as flying capacitor (2.2µF). Place it close to the PVDD and PGND.

Charge Pump Flying Capacitor, C_{CPF}

The flying capacitor affects the load transient of the charge pump. If the capacitor's value is too small, then that will degrade the charge pump's current driver capability and the performance of line drive amplifier.

Increasing the flying capacitor's value will improve the load transient of charge pump. It is recommended using the low ESR ceramic capacitors (X7R type is recommended) above 2.2µF.

Charge Pump Output Capacitor, C_{CPO}

The output capacitor's value affects the power ripple directly at CV_{SS} (V_{SS}). Increasing the value of output capacitor reduces the power ripple. The ESR of output capacitor affects the load transient of CV_{SS} (V_{SS}). Lower ESR and greater than 2.2µF ceramic capacitor is a recommendation.

Layout Consideration

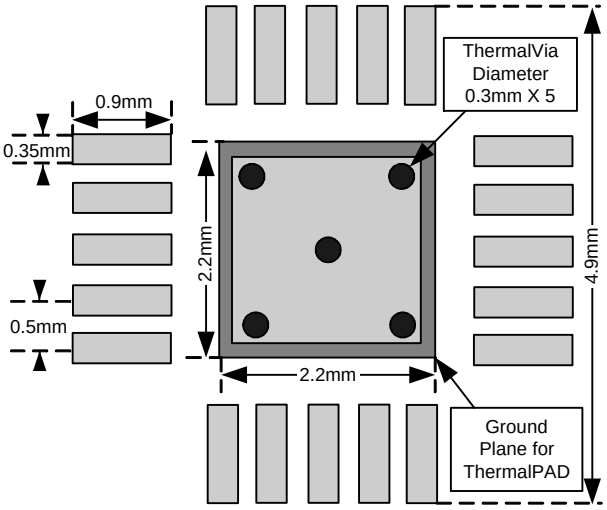
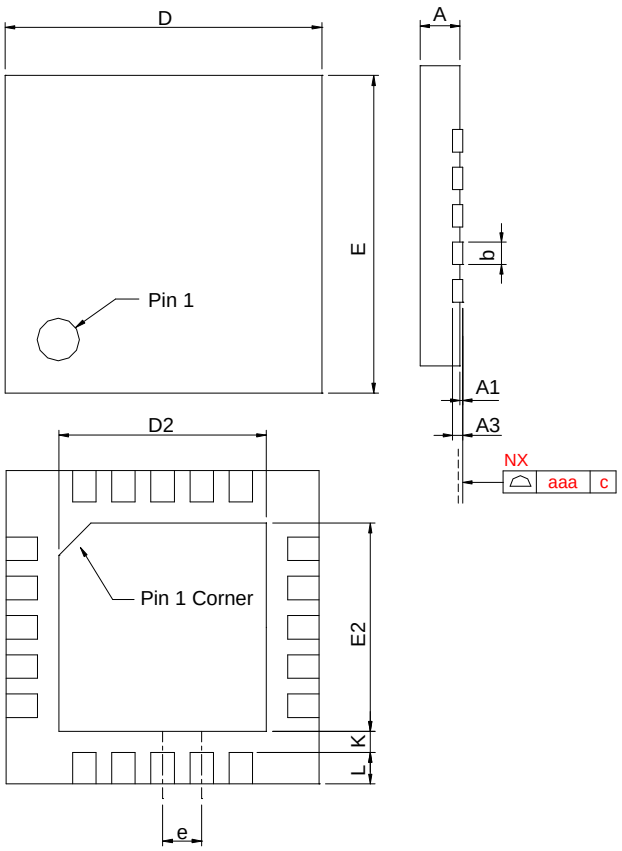


Figure 2: TQFN4x4-20B Land Pattern Recommendation

1. All components should be placed close to the APA2174. For example, the input capacitor (C_i) should be close to APA2174's input pins to avoid causing noise coupling to APA2174's high impedance inputs; the decoupling capacitor (C_S) should be placed by the APA2174's power pin to decouple the power rail noise.
2. The output traces should be short and wide (>20mil),
3. The input trace should be short and symmetric.
4. The power trace width should be greater than 20mil.
5. The TQFN Thermal PAD should be soldered on PCB, and the ground plane needs soldered mask (to avoid short circuit) except the Thermal PAD area.

Package Information

TQFN4x4-20B

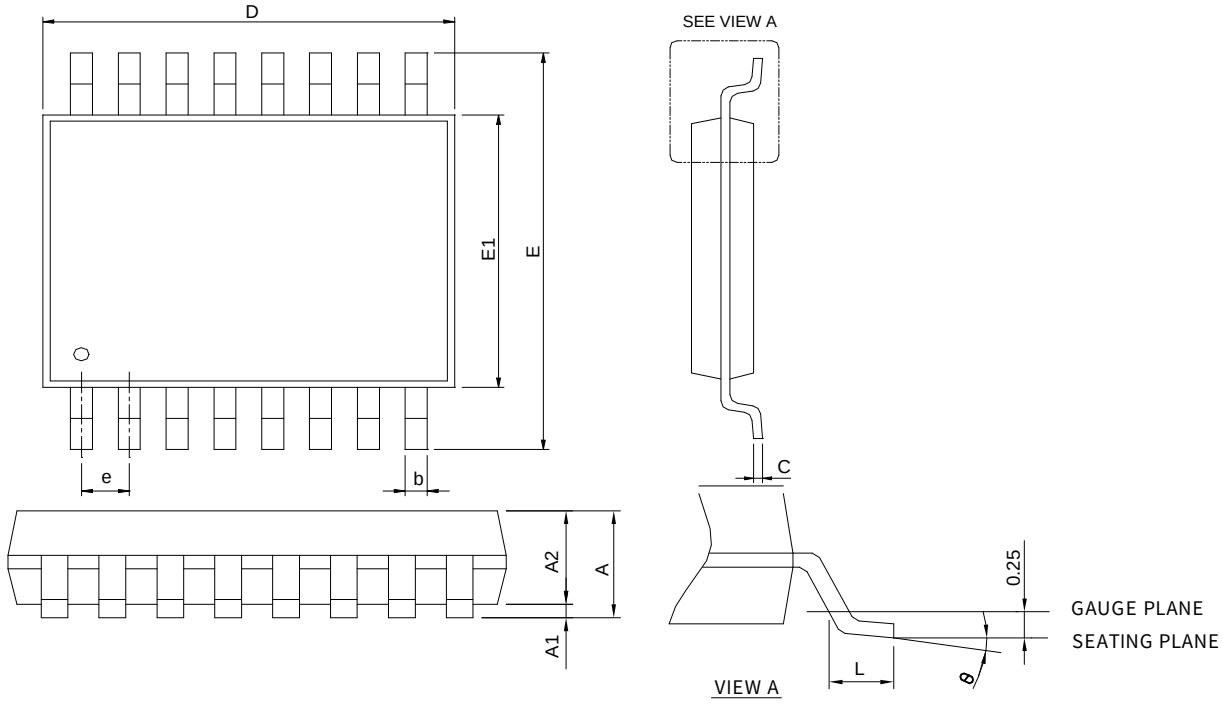


SYMBOL	TQFN4x4-20B			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.008	0.012
D	3.90	4.10	0.154	0.161
D2	2.00	2.70	0.079	0.098
E	3.90	4.10	0.154	0.161
E2	2.00	2.70	0.079	0.098
e	0.50 BSC		0.020 BSC	
L	0.35	0.45	0.014	0.018
K	0.20		0.008	
aaa	0.08		0.003	

Note : 1. Followed from JEDEC MO-220 VGGD-5.

Package Information

TSSOP-16

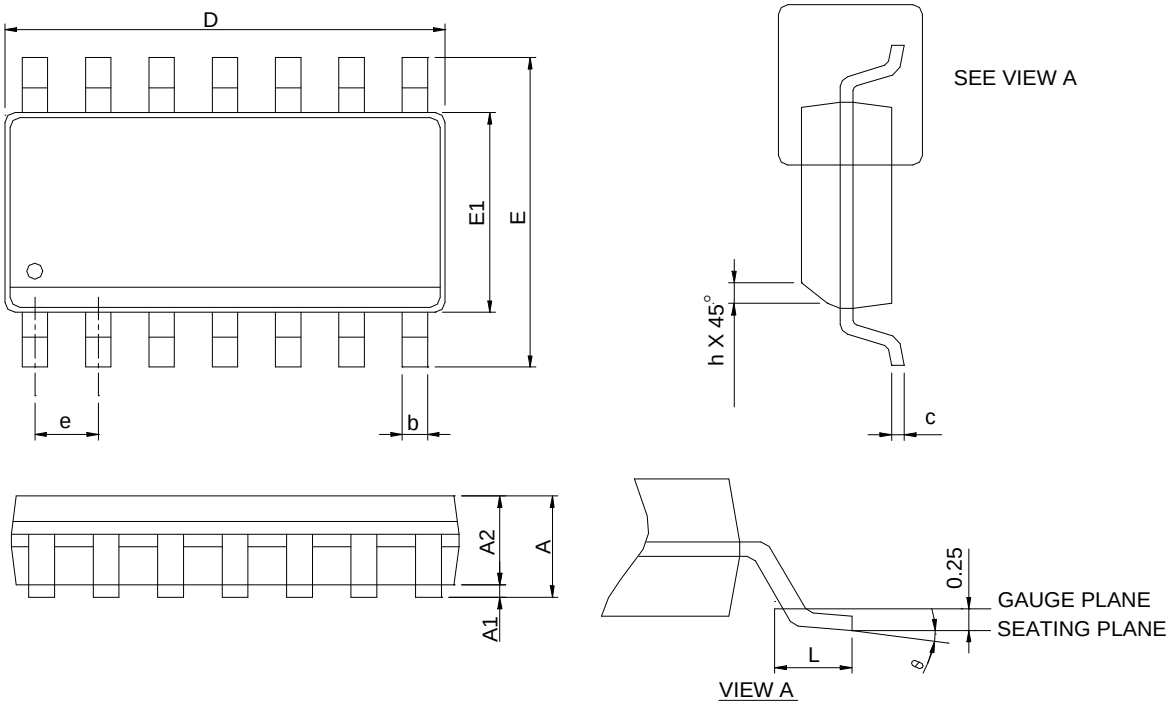


SYMBOL	TSSOP-16			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.20		0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.031	0.041
b	0.19	0.30	0.007	0.012
c	0.09	0.20	0.004	0.008
D	4.90	5.10	0.193	0.201
E	6.20	6.60	0.244	0.260
E1	4.30	4.50	0.169	0.177
e	0.65 BSC		0.026 BSC	
L	0.45	0.75	0.018	0.030
θ	0°	8°	0°	8°

Note : 1. Follow from JEDEC MO-153 AB.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension "E1" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Package Information

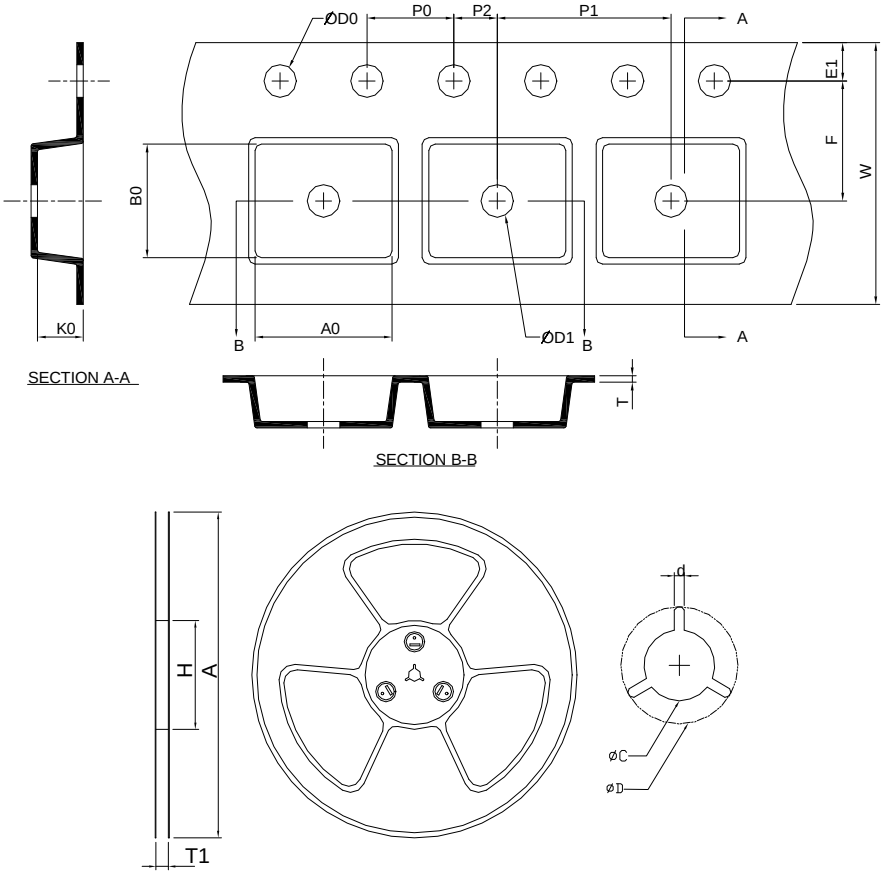
SOP-14



SYMBOL	SOP-14			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	8.55	8.75	0.337	0.344
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MS-012 AB.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension “E” does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFN4x4-20B	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	4.30±0.20	4.30±0.20	1.30±0.20
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
TSSOP-16	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.50±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.00±0.10	8.00±0.10	2.00±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.90±0.20	5.40±0.20	1.60±0.20
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
SOP-14	330.0±2.00	50 MIN.	16.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	16.0±0.30	1.75±0.10	7.50±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	9.00±0.20	2.10±0.20

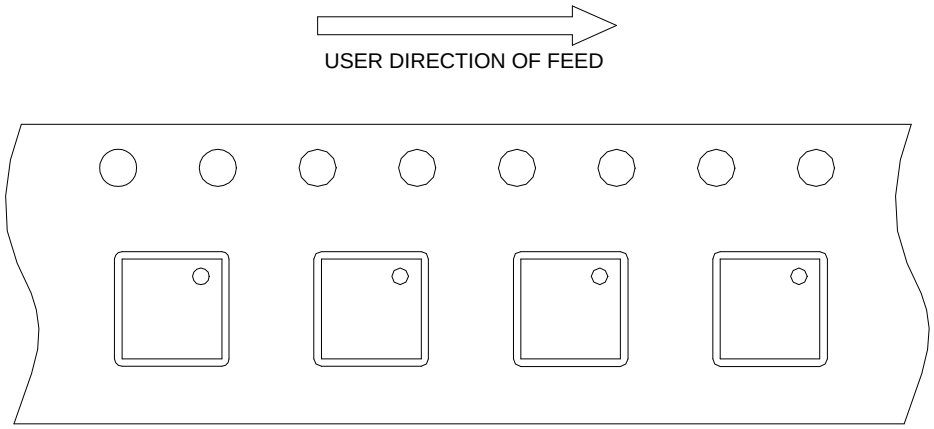
(mm)

Devices Per Unit

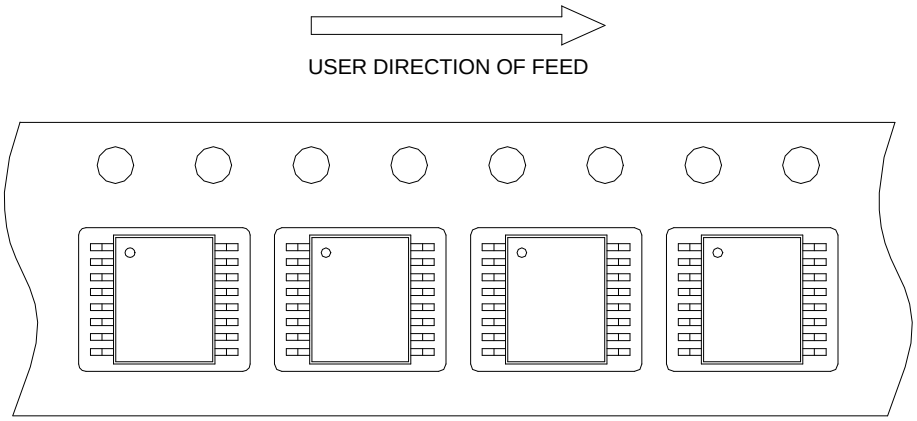
Package Type	Unit	Quantity
TQFN4x4-20B	Tape & Reel	3000
TSSOP-16	Tape & Reel	2500
SOP-14	Tape & Reel	2500

Taping Direction Information

TQFN4x4-20B

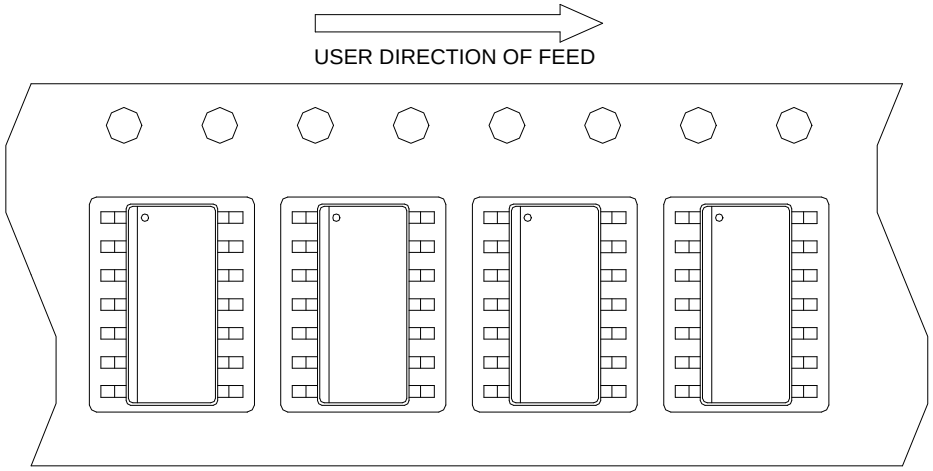


TSSOP-16

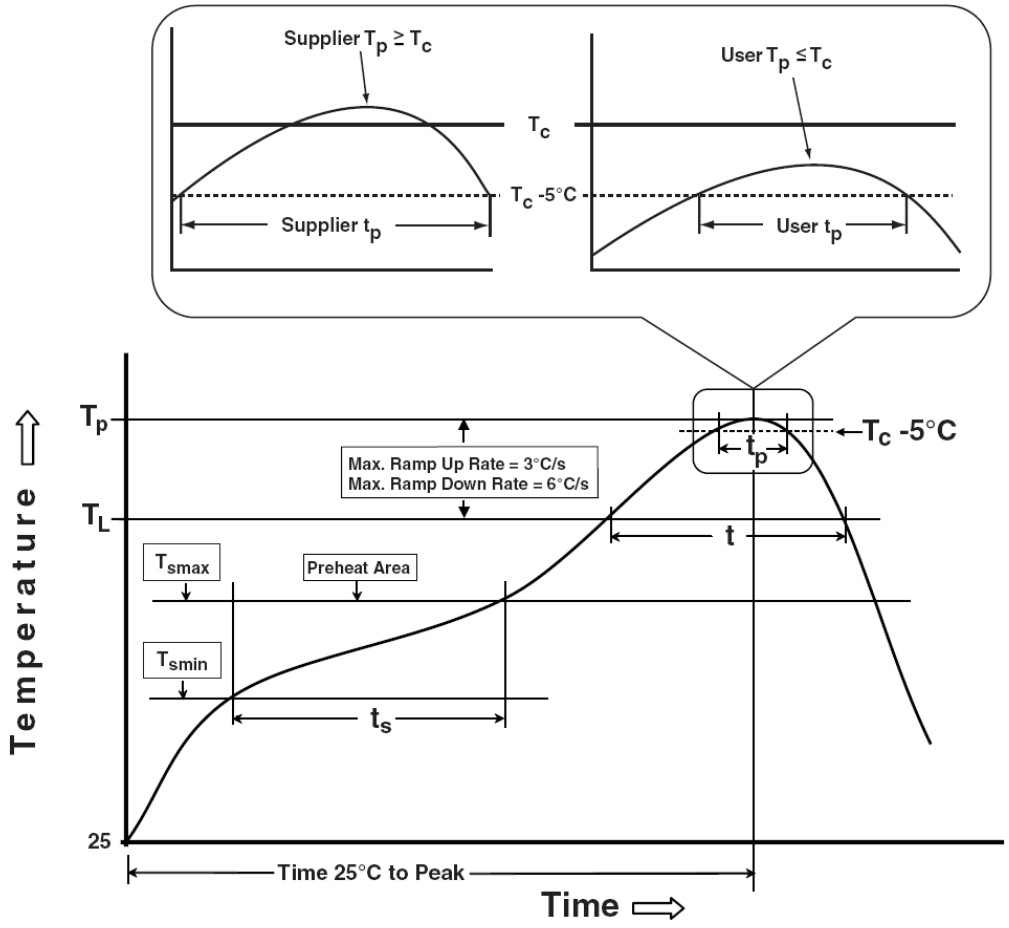


Taping Direction Information

SOP-14



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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