2A ULTRA LOW DROPOUT LINEAR REGULATOR

FEATURES

- **Ultra Low Dropout 0.21V(typical) @ 2A Output Current for 1.2V Output Voltage**
- **Low ESR Output Capacitor (Multi-layer Chip Capacitors (MLCC)) Applicable**
- **EN Pull-low for APE8902CMP-A**
  EN Pull-high for APE8902CMP-B
- **Fast Transient Response**
- **Adjustable Output Voltage by External Resistors**
- **Power-On-Reset Monitoring on Both VCNTL and VIN Pins**
- **Internal Soft-Start**
- **Current-Limit and Thermal Shutdown Protection**
- **Power-OK Output with a Delay Time**
- **SO-8 with Exposed Pad & DFN 3x3-10L Pb-Free Package.**
- **Halogen Free Product**

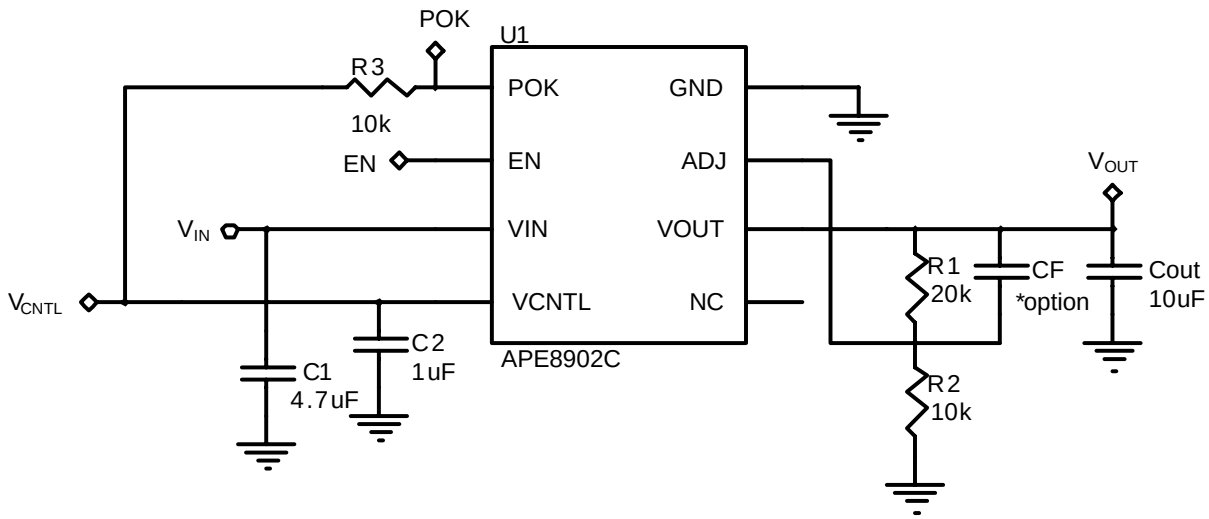
DESCRIPTION

The APE8902C series is a 2A ultra low dropout linear regulator. This product is specifically designed to provide well supply voltage for front-side-bus termination on motherboards and NB applications. The IC needs two supply voltages, a control voltage for the circuitry and a main supply voltage for power conversion, to reduce power dissipation and provide extremely low dropout. The APE8902C series integrates many functions. A Power-On-Reset (POR) circuit monitors both supply voltages to prevent wrong operations. A thermal shutdown and current limit functions protect the device against thermal and current over-loads. A POK indicates the output status with time delay which is set internally. It can control other converter for power sequence.

The APE8902C series can be enabled by other power system. Pulling and holding the EN pin below 0.4V shuts off the output.

The APE8902C series is available in ESOP-8 package which features small size as SO-8 and an Exposed Pad to reduce the junction-to-case resistance, being applicable in 2~3W applications.

TYPICAL APPLICATION

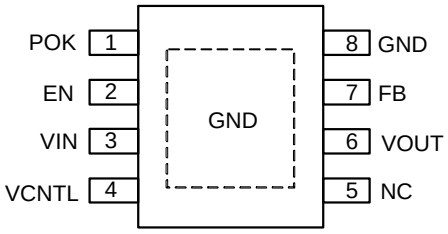


PACKAGE/ORDERING INFORMATION

APE8902CX-X

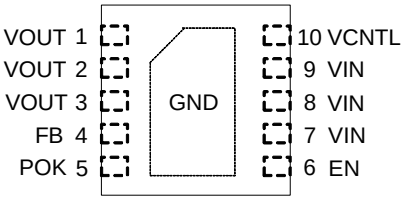
Package Type	EN Function
MP : ESOP-8	A : Internal Pull Low
GN3 : DFN 3x3-10L	B : Internal Pull High

(Top View)



ESOP-8

(Top View)



DFN 3x3-10L

ABSOLUTE MAXIMUM RATINGS (Note1)

CNTL Supply Voltage (V_{CNTL})	-0.3V To 6.5V
Input Supply Voltage (V_{IN})	-0.3V To 6.5V
EN & FB Pin Voltage (V_{EN}/V_{FB})	-0.3V To VCNTL+0.3V
Power Good Voltage (V_{POK})	-0.3V To 6.5V
Power Dissipation (P_D)	2.5W
Storage Temperature Range (T_{ST})	-65°C To 150°C
Junction Temperature Range (T_J)	-40°C To 150°C
Thermal Resistance Junction to Ambient (Rth_{ja}) Note.	
ESOP-8	40°C/W
DFN 3x3-10L	62.5°C/W
Thermal Resistance Junction to Case (Rth_{jc}) Note.	
ESOP-8	15°C/W
DFN 3x3-10L	17°C/W

Note. mounted on a Demo board

RECOMMENDED OPERATING CONDITIONS

Operating Junction Temperature Range (T_{OJ})	-40°C To 125°C
Operating Ambient Temperature Range (T_{OA})	-40°C To 85°C
VCNTL Supply Voltage (V_{CNTL})	3V To 6V
Input Supply Voltage (V_{IN})	1.1V To 5.5V
Output Voltage (V_{OUT})@$V_{CNTL} \geq V_{OUT}$ + 2.5V	0.8V To 2.8V
Output Cunrrent (I_{OUT})	0A To 2A

ELECTRICAL SPECIFICATIONS

V_{CNTL}= 5V, V_{IN}=1.8V, V_{OUT}=1.2V, T_A=25°C unless otherwise specified

Parameter	SYM	TEST CONDITION		MIN	TYP	MAX	UNITS
V_{CNTL} Operation Voltage	V_{CNTL}			2.8	-	5.5	V
V_{IN} POR Threshold	V_{IN}			0.8	0.9	1	V
V_{IN} POR Hysteresis	$V_{IN(hys)}$			-	0.5	-	V
V_{CNTL} Nominal Supply Current	I_{CNTL}	EN= V_{CNTL}		-	1.3	-	mA
VCNTL Shutdown Current	I_{SD}	EN=0V	APE8902CMP-A	-	-	1	uA
			APE8902CMP-B	-	10	30	
Feedback Voltage	V_{FB}	V_{CNTL}=3 ~ 6V, I_{OUT}=10mA, V_{IN}=V_{OUT}+0.5~5.5V		0.784	0.8	0.816	V
Load Regulation		I_{OUT}=0A ~ 2A		-	0.5	1	%
On Resistance	$R_{DS(ON)}$	I_{OUT}=100mA, V_{CNTL}=V_{EN}=5.0V, V_{OUT}=1.2V		-	105	150	mΩ
Dropout Voltage	V_{DROP}	I_{OUT} = 2A, V_{CNTL}=5V, V_{OUT} = 1.2V		-	0.21	0.3	V
V_{OUT} Pull Low Resistance		EN=0V		-	40	-	Ω
Soft Start Time	T_{SS}			-	0.2	-	ms
EN Pin Logic High Threshold Voltage	V_{ENH}	Enable		1.2	-	-	V
	V_{ENL}	Disable		-	-	0.6	
EN Pin Pull-Up Current	I_{EN}	EN=5V, APE8902CMP-A		-	10	20	uA
		EN=GND, APE8902CMP-B		-	10	20	
Current Limit	I_{LIM}	V_{CNTL}=5V, V_{IN}=V_{OUT}+1V		2.5	-	-	A
Ripple Rejection V_{IN}	PSRR	F=120Hz, I_{OUT}=100mA		-	65	-	dB
Ripple Rejection V_{CNTL}				-	65	-	
POK Threshold Voltage for Power OK	V_{POK}	VFB Rising		92%	94%	96%	V_{FB}
POK Threshold Voltage for Power Not OK	V_{PNOK}	VFB Falling		83%	88%	91%	V_{FB}
POK Low Voltage		POK sinks 5mA		-	-	0.1	V
POK Delay Time	T_{DELAY}			0.8	2	10	ms
Thermal Shutdown Threshold (Note1)	T_{SD}			-	160	-	°C
Thermal Shutdown Hysteresis (Note1)				-	40	-	°C

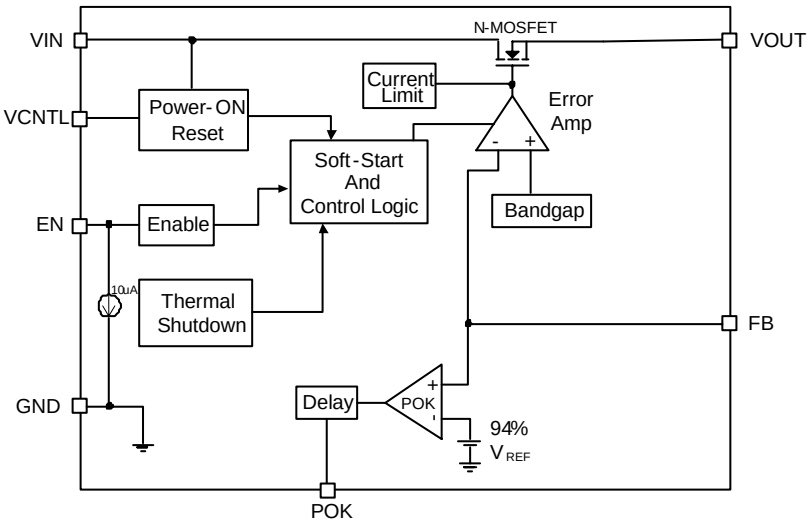
Note1: Guarantee by design, not production tested.

PIN DESCRIPTIONS

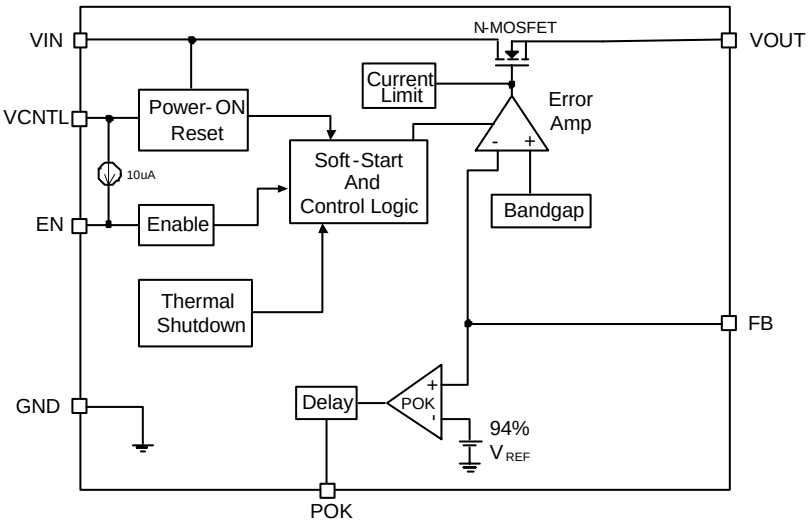
PIN SYMBOL	PIN DESCRIPTION
POK	Power OK Output Pin
EN	Internal Pull High (APE8902CMP-B) or Pull Low (APE8902CMP-A) EN=High or Floating → Enable EN=Low → Shutdown Mode
VIN	Supply input for power conversion. The pin is monitored for Power-On Reset purpose.
VCNTL	Power input pin of the control circuitry. The pin is monitored for Power-On Reset purpose.
NC	No Connect
VOUT	Output Voltage
FB	Feedback Pin
GND	GND Pin

BLOCK DIAGRAM

APE8902CMP-A



APE8902CMP-B



PIN DESCRIPTION

FB

Connecting this pin to an external resistor divider receives the feedback voltage of the regulator. The output voltage set by the resistor divider is determined by:

$$V_{OUT} = 0.8 \cdot \left(1 + \frac{R1}{R2}\right) \quad (V)$$

Where R1 is connected from VOUT to FB with Kelvin sensing and R2 is connected from FB to GND. A bypass capacitor may be connected with R1 in parallel to improve load transient response. The R2 range in 1K~4.7KΩ for AL output capacitor and 30K~100KΩ for MLCC output capacitor are recommended.

VIN

Main supply input pins for power conversions. The voltage at this pin is monitored for Power-On Reset purpose.

VCNTL

Power input pin of the control circuitry. Connecting this pin to a +5V (recommended) supply voltage provides the bias for the control circuitry. The voltage at this pin is monitored for Power-On Reset purpose.

POK

Power-OK signal output pin. This pin is an open-drain output used to indicate status of output voltage by sensing FB voltage. This pin is pulled low when the rising FB voltage is not above the VPOK threshold or the falling FB voltage is below the VPOK threshold, indicating the output is not OK.

EN

Enable control pin. Pulling and holding this pin below 0.4V shuts down the output. When re-enabled, the IC undergoes a new soft-start cycle. For APE8902CMP-B, this pin is internal pulled up to VCNTL voltage, enabling the regulator. For APE8902CMP-A, this pin is internal pulled down to GND voltage, shutdown the regulator. The pull-high current is 10uA (typ.)

VOUT

Output of the regulator. Please connect Pin 6 using wide tracks. It is necessary to connect an output capacitor with this pin for closed-loop compensation and improving transient responses.

FUNCTION DESCRIPTION

Power-On-Reset

A Power-On-Reset (POR) circuit monitors both input voltages at VCNTL and VIN pins to prevent wrong logic controls. The POR function initiates a soft-start process after the two supply voltages exceed their rising POR threshold voltages during powering on. The POR function also pulls low the POK pin regardless the output voltage when the VCNTL voltage falls below its falling POR threshold.

Internal Soft-Start

An internal soft-start function controls rise rate of the output voltage to limit the current surge at start-up. The typical soft-start interval is about 0.2ms.

Output Voltage Regulation

An error amplifier working with a temperature compensated 0.8V reference and an output NMOS regulates output to the preset voltage. The error amplifier designed with high bandwidth and DC gain provides very fast transient response and less load regulation. It compares the reference with the feedback voltage and amplifies the difference to drive the output NMOS which provides load current from VIN to VOUT.

FUNCTION DESCRIPTION

Current-Limit

The APE8902C monitors the current via the output NMOS and limits the maximum current to prevent load and APE8902C from damages during overload or short circuit conditions.

Thermal Shutdown

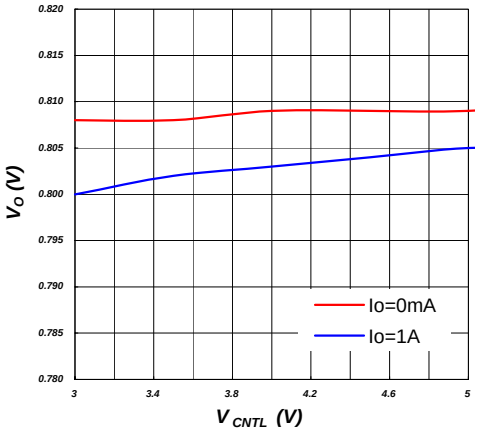
A thermal shutdown circuit limits the junction temperature of APE8902C. When the junction temperature exceeds +160°C, a thermal sensor turns off the output NMOS, allowing the device to cool down. The regulator regulates the output again through initiation of a new soft-start cycle after the junction temperature cools by 40 ° C, resulting in a pulsed output during continuous thermal overload conditions. The thermal shutdown designed.

APPLICATION INFORMATION

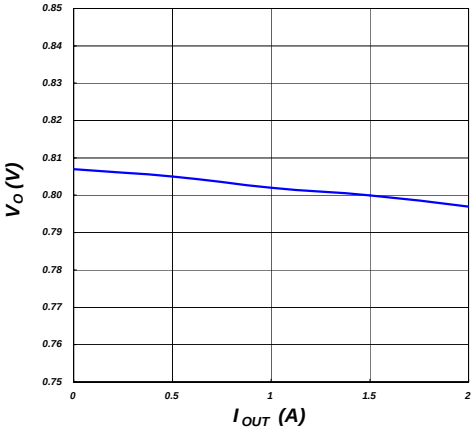
Capacitor Selection

Normally, use a MLCC capacitor on the input and output of the APE8902C. Larger input capacitor values provide better supply-noise rejection and transient response. A higher- value output capacitor may be necessary if large, fast transients are anticipated and the device is located several inches from the power source. The X5R and X7R type in MLCC is recommended. For aluminum electrolytic capacitor application, 100uF in input capacitor and 220uF in output capacitor (30m Ω < ESR < 200m Ω) are recommended. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR.

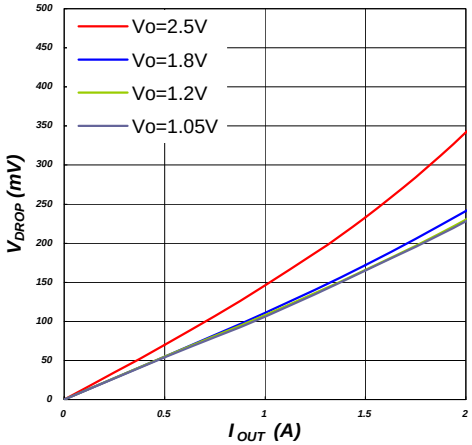
TYPICAL PERFORMANCE CHARACTERISTICS



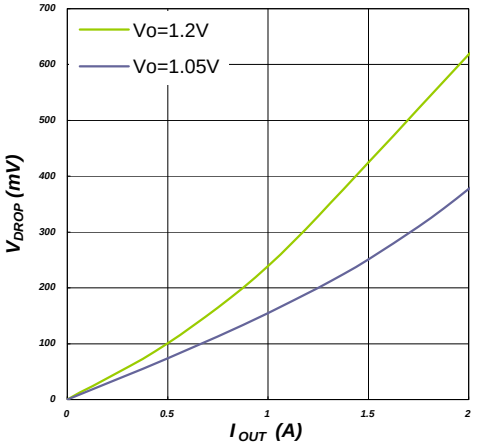
Line Regulation



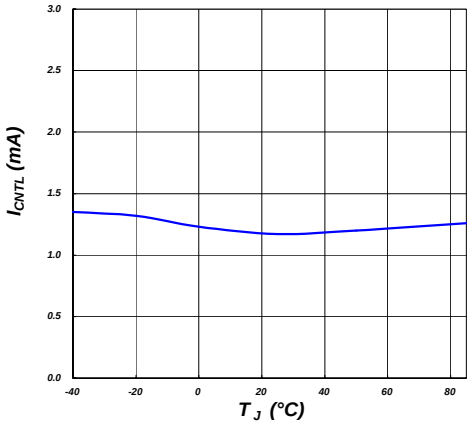
Load Regulation



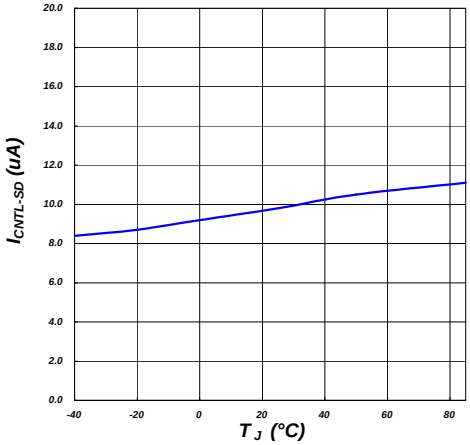
Dropout Voltage at V_{CNTL}=5V



Dropout Voltage at V_{CNTL}=3.3V

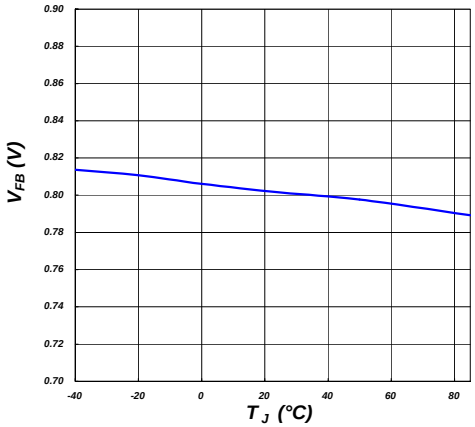


I_{CNTL} vs. T_J

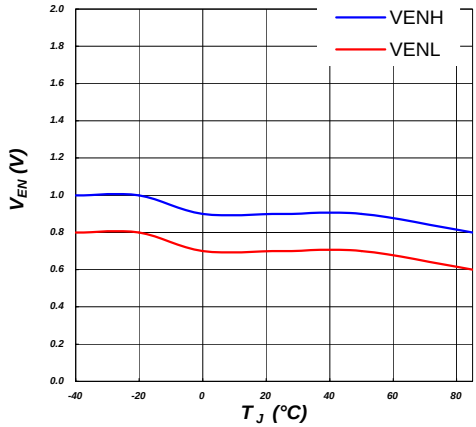


$I_{CNTL-SD}$ (APE8902CMP-B) vs. T_J

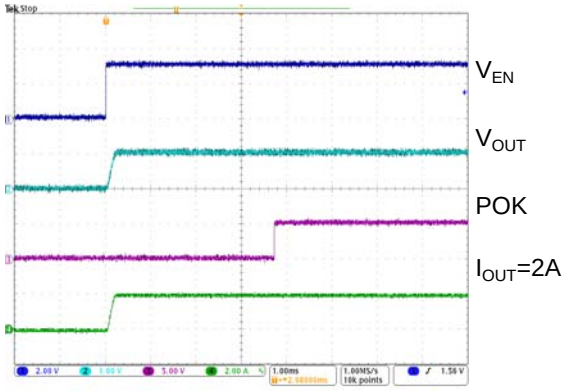
TYPICAL PERFORMANCE CHARACTERISTICS



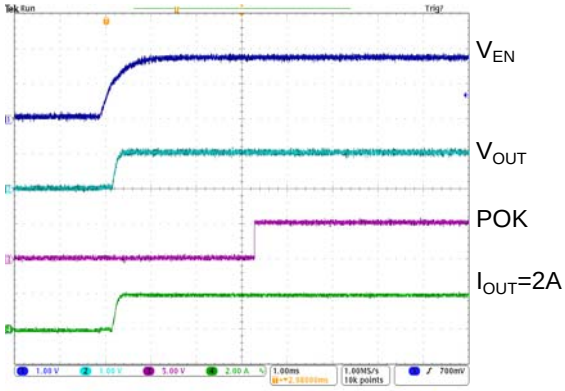
V_{FB} vs. T_J



V_{EN} vs. T_J



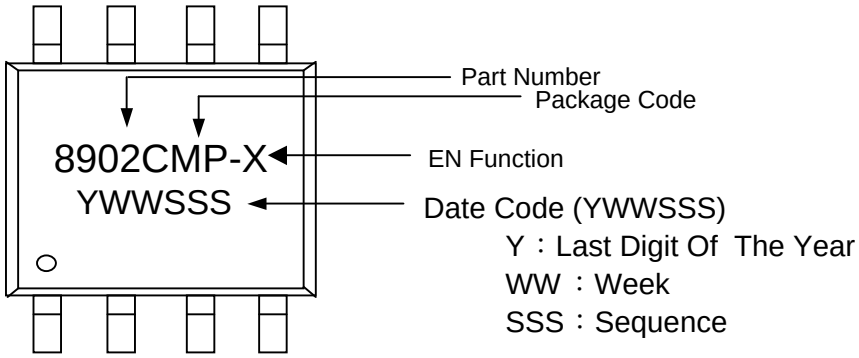
EN on with POK Delay



VIN Power –ON

MARKING INFORMATION

ESOP-8



DFN 3x3-10L