ULTRA- LOW ON RESISTANCE, 6A LOAD SWITCH WITH CONTROLLED TURN-ON

FEATURES

- Integrated 6A Single Channel Load Switch
- Input Voltage Range: 0.8V to 5.5V
- Ultra-low ON-Resistance
  - R_{ON} = 20mΩ at VIN=5V (VBIAS=5V)
  - R_{ON} = 21mΩ at VIN=1.8V (VBIAS=5V)
- Low Threshold Control Input
- Adjustable Rise Time
- Quick Output Discharge Transistor
- ESD Level
  - 2KV for HBM and 1KV for CDM
- Halogen Free Product

APPLICATIONS

- Telecom Systems
- Industrial Systems
- Set-Top-Box
- Consumer Electronics
- Notebooks / Netbooks

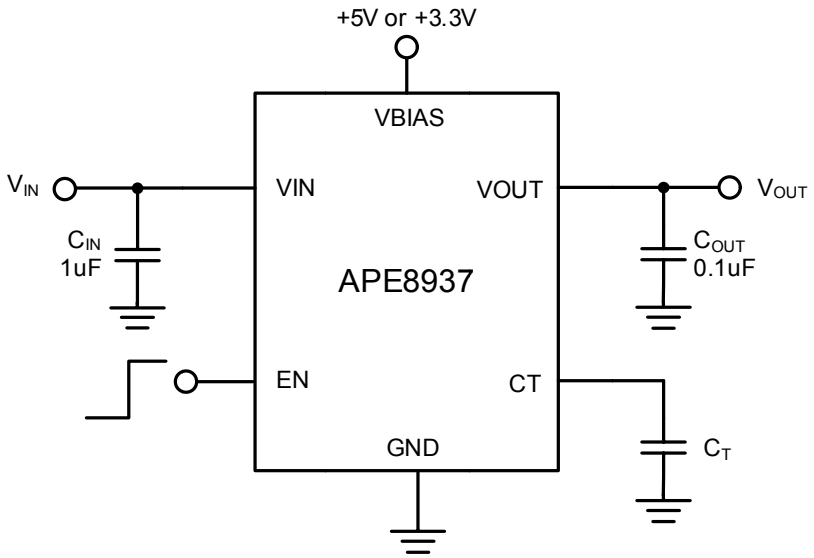
DESCRIPTION

The APE8937 is a small, ultra-low R_{ON} load switch with controlled turn on. It contains one N-channel MOSFET that can operate over an input voltage range of 0.8V to 5.5V and support maximum continuous current up to 6A. The switch is controlled by an on/off input (EN), which is capable of interfacing directly with low-voltage control signals.

Additional features include a 300Ω on-chip load resistor for output quick discharge when switch is turned off, in order to avoid inrush current, the rise time is adjustable by an external ceramic capacitor on the CT pin.

The APE8937 is available in an ultra-small, space saving 2mmx2mm 8-pin DFN package with thermal pad.

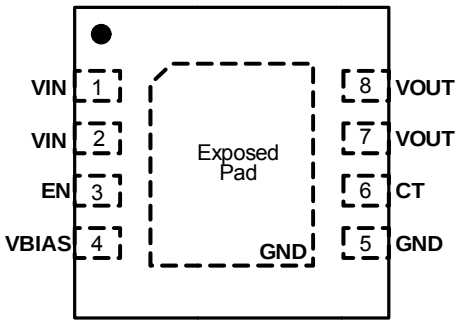
TYPICAL APPLICATION



ORDERING / PACKAGE INFORMATION

APE8937X
└ Package Type
GN2: DFN 2x2-8L

Top View
DFN 2x2-8L



ABSOLUTE MAXIMUM RATINGS (at T_A=25°C)

VIN	-0.3V to 6V
VOUT	VIN+0.3V
EN, CT	-0.3V to 6V
VBIAS	-0.3+6V
I_{MAX}	6A
Storage Temperature Range (T_{ST})	-65 to +150°C
Junction Temperature (T_J)	150°C
Lead Temperature (Soldering, 10sec.)	260°C
Thermal Resistance from Junction to Ambient ($R\theta_{JA}$)	
DFN-8L (2mmX2mm)	100°C/W
Electrostatic Discharge (ESD)	
HBM (MIL-STD-883G Method 3015.7)	2KV
CDM (JESD22-C101-C)	1KV

RECOMMENDED OPERATING CONDITIONS

VIN	0.8V to 5.5V
VBIAS	2.5V to 5.5V (VBIAS≧VIN)
VOUT	VIN
CIN	≧0.1uF
Junction Temperature (T_J)	125°C
Operating Temperature Range	-40°C to 85°C

ELECTRICAL SPECIFICATIONS

(VIN=0.8 to 5.5V, VBIAS=5V,C_{IN}=1uF, C_{OUT}=0.1uF, T_A =25°C, unless otherwise specified)

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNIT
Quiescent Current	I_{BIAS}	V_{BIAS}=V_{IN}=V_{EN}=5V, I_{OUT}=0A		50	75	uA
		V_{BIAS}=V_{IN}=V_{EN}=2.5V, I_{OUT}=0A		30	50	uA
Shutdown Current	I_{SD}	V_{EN}=GND			1	uA
ON Resistance	R_{ON}	VIN=5V, IOUT=-200mA		20	26	mΩ
		VIN=5V, IOUT=-200mA, -40°C < T_A < 85°C			33	mΩ
		VIN=2.5V, IOUT=-200mA		20	26	mΩ
		VIN=2.5V, IOUT=-200mA, -40°C < T_A < 85°C			33	mΩ
		VIN=1.8V, IOUT=-200mA		20	26	mΩ
		VIN=1.8V, IOUT=-200mA, -40°C < T_A < 85°C			33	mΩ
		VIN=1.5V, IOUT=-200mA		20	26	mΩ
		VIN=1.5V, IOUT=-200mA, -40°C < T_A < 85°C			33	mΩ
		VIN=1.05V, IOUT=-200mA		20	26	mΩ
		VIN=1.05V, IOUT=-200mA, -40°C < T_A < 85°C			33	mΩ
		VIN=0.8V, IOUT=-200mA		20	26	mΩ
		VIN=0.8V, IOUT=-200mA, -40°C < T_A < 85°C			33	mΩ
Output Pull Down Resistance	R_{OPD}	V_{BIAS}=5V, V_{EN}=0V		300	350	Ω
EN Input Leakage Current	I_{ON}	V_{EN}=5V or GND			1	uA
EN Threshold	V_{ENH}	on	1.2			V
	V_{ENL}	off			0.5	V

Note1: Guarantee by design, not production tested.

Note2: Make sure $V_{BAIS} \geqq V_{IN}$ for optimum R_{ON} performance.

SWITCHING SPECIFICATIONS

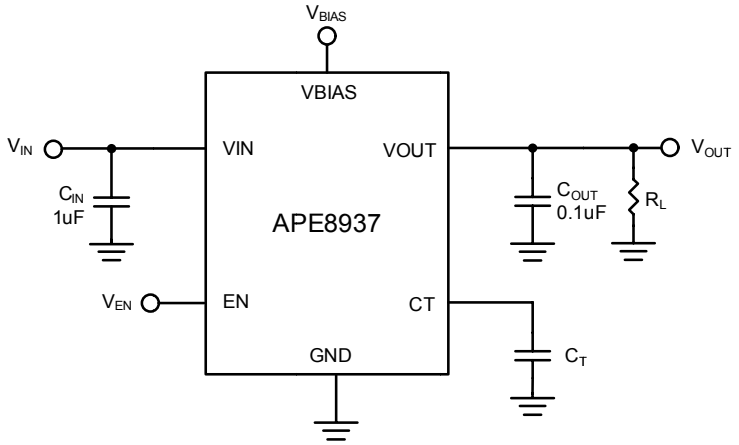


Fig.1 Test Circuit

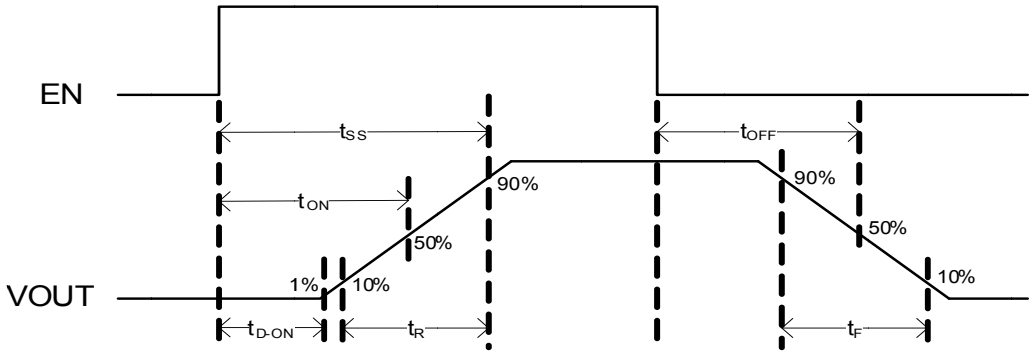


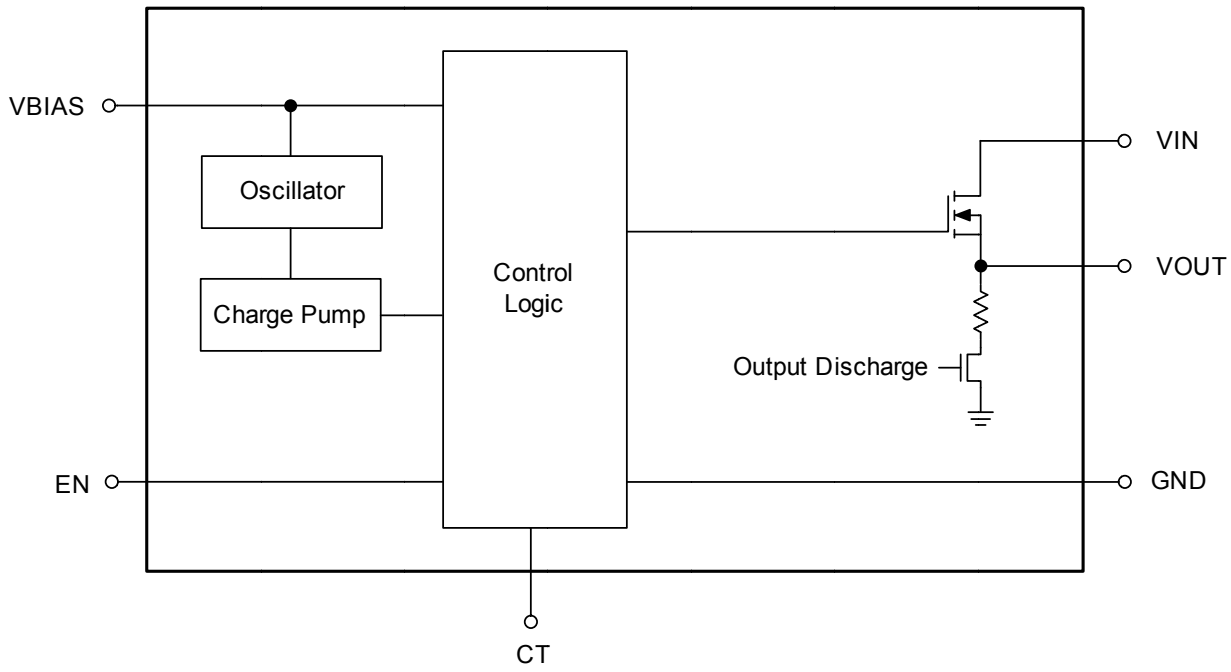
Fig.2 ON/OFF Waveforms

PARAMETER	SYM	TEST CONDITION		MIN	TYP	MAX	UNIT
Turn-on Time	t_{ON}	V_{BIAS}=V_{EN}=5V, C_T=1nF, R_L=10Ω	V_{IN}=5V		1480		us
			V_{IN}=0.8V		520		us
Turn-off Time	t_{OFF}	V_{BIAS}=V_{EN}=5V, C_T=1nF, R_L=10Ω	V_{IN}=5V		1		us
			V_{IN}=0.8V		1		us
Soft Start Time	t_{SS}	V_{BIAS}=V_{EN}=5V, C_T=1nF, R_L=10Ω	V_{IN}=5V		2400		us
			V_{IN}=0.8V		700		us
VOUT Rise Time	t_R	V_{BIAS}=V_{EN}=5V, C_T=1nF, R_L=10Ω	V_{IN}=5V		1910		us
			V_{IN}=0.8V		290		us
VOUT Fall Time	t_F	V_{BIAS}=V_{EN}=5V, C_T=1nF, R_L=10Ω	V_{IN}=5V		1.9		us
			V_{IN}=0.8V		1.6		us
VOUT Turn-on Delay Time	t_{D-ON}	V_{BIAS}=V_{EN}=5V, C_T=1nF, R_L=10Ω	V_{IN}=5V		310		us
			V_{IN}=0.8V		270		us

PIN DESCRIPTIONS

PIN No.	PIN SYMBOL	PIN DESCRIPTION
1, 2	VIN	Input power supply; bypass this input with a ceramic capacitor to ground.
3	EN	Enable control input, active high. Do not leave floating.
4	VBIAS	Bias voltage.
5	GND	Ground.
6	CT	A capacitor to ground set the rise time of VOUT.
7, 8	VOUT	Switch output
Exposed pad	GND	Tie to ground to alleviate thermal stress.

BLOCK DIAGRAM



TYPICAL PERFORMANCE CHARACTERISTICS

Condition: V_{BIAS}=V_{EN}=5V, CT=1nF, C_{IN}=1μF, C_{OUT}=0.1μF, ch1:EN, ch2: I_{IN}, ch3: V_{OUT}

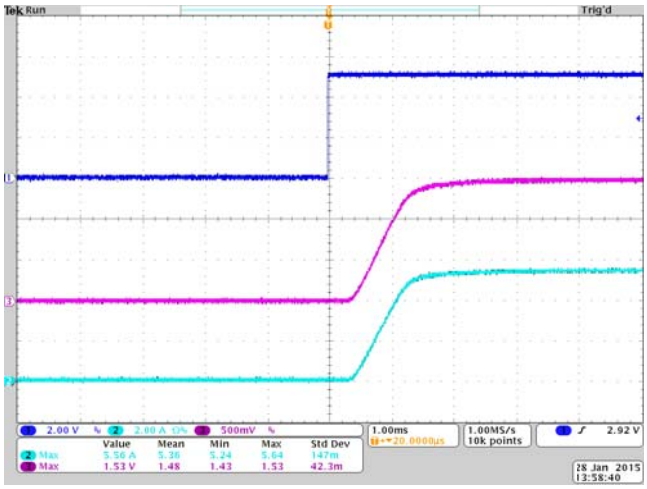


Fig.3 Start-up Waveform, VIN=1.5V, RL=0.25Ω

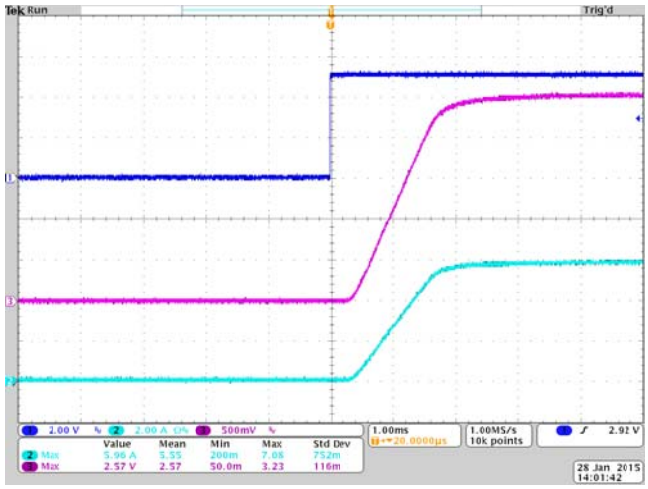


Fig.4 Start-up Waveform, VIN=2.5V, RL=0.6Ω

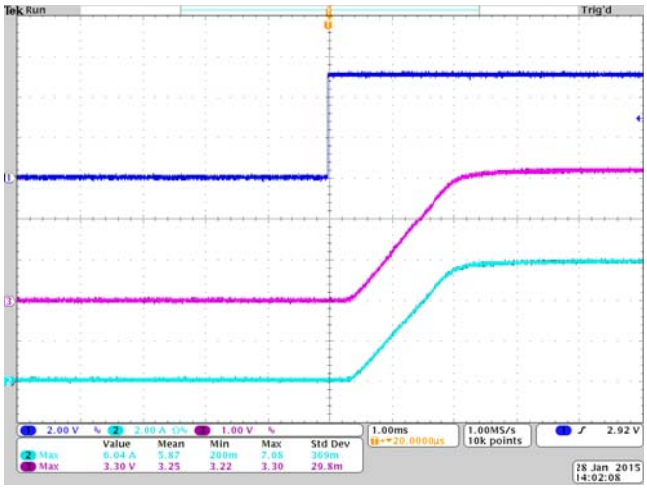


Fig.5 Start-up Waveform, VIN=3.3V, RL=0.5Ω

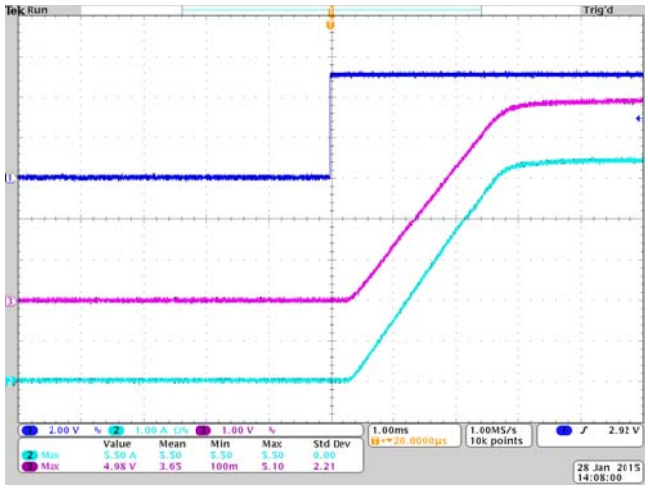


Fig.6 Start-up Waveform, VIN=5V, RL=0.83Ω

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Condition: V_{BIAS}=V_{EN}=2.5V, CT=1nF, C_{IN}=1µF, C_{OUT}=0.1µF, ch1:EN, ch2: I_{IN}, ch3: V_{OUT}

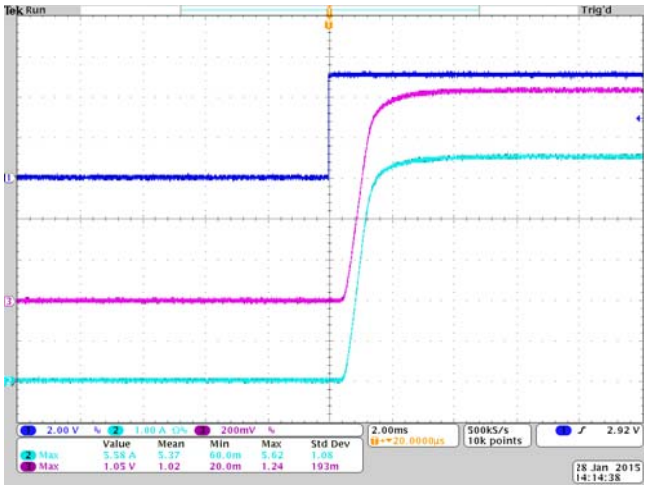


Fig.7 Start-up Waveform, VIN=1.2V, RL=0.2Ω

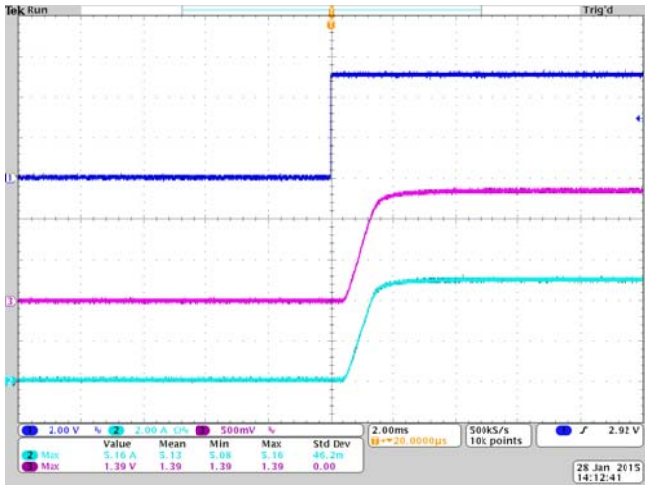


Fig.8 Start-up Waveform, VIN=1.5V, RL=0.25Ω

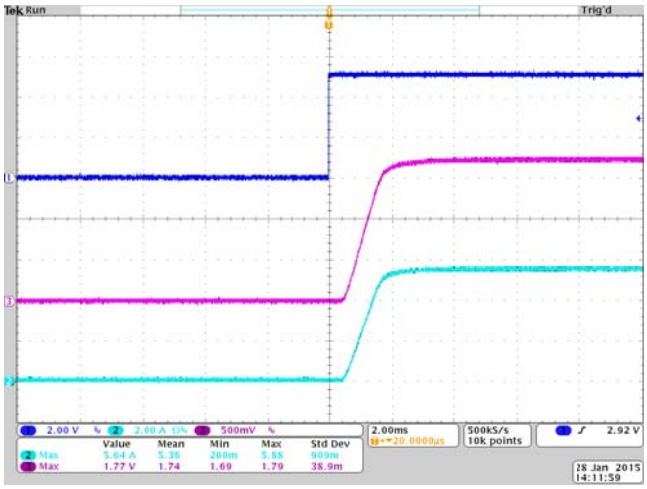


Fig.9 Start-up Waveform, VIN=1.8V, RL=0.33Ω

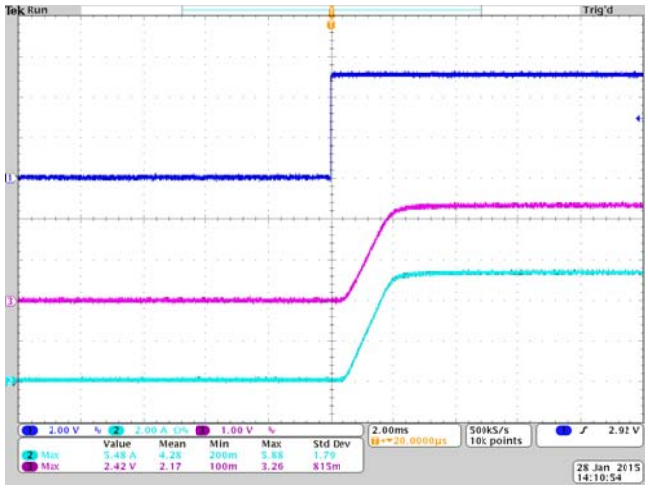


Fig.10 Start-up Waveform, VIN=2.5V, RL=0.4Ω

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Condition: V_{BIAS}=V_{EN}=5V, CT=1nF, C_{IN}=1μF, C_{OUT}=0.1μF, RL=10Ω, ch1:EN, ch2:V_{OUT}

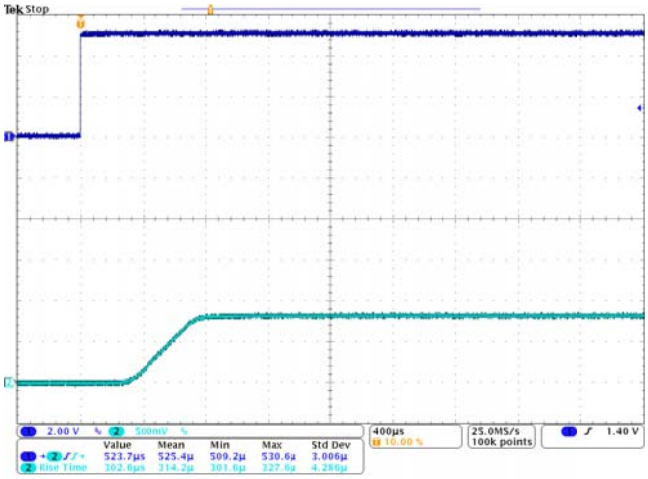


Fig.11 Turn-on Response Time, VIN=0.8V

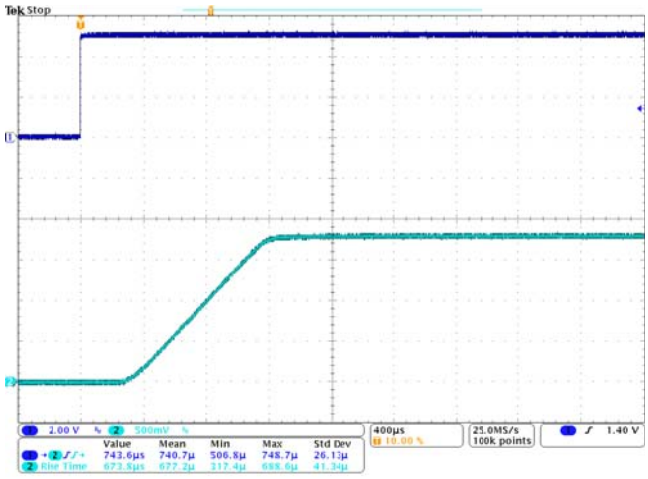


Fig.12 Turn-on Response Time, VIN=1.8V

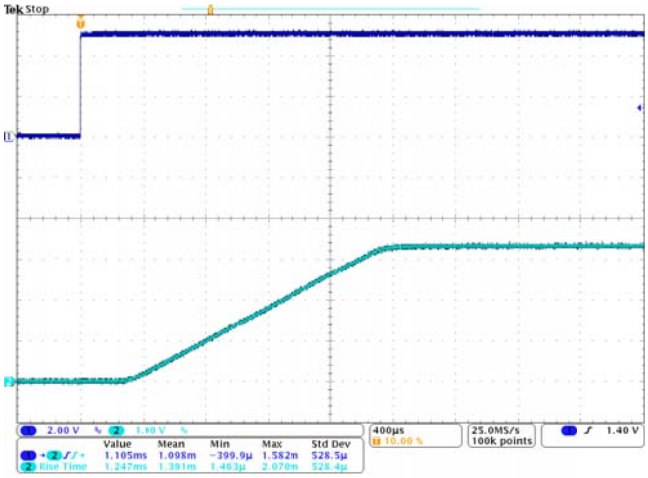


Fig.13 Turn-on Response Time, VIN=3.3V

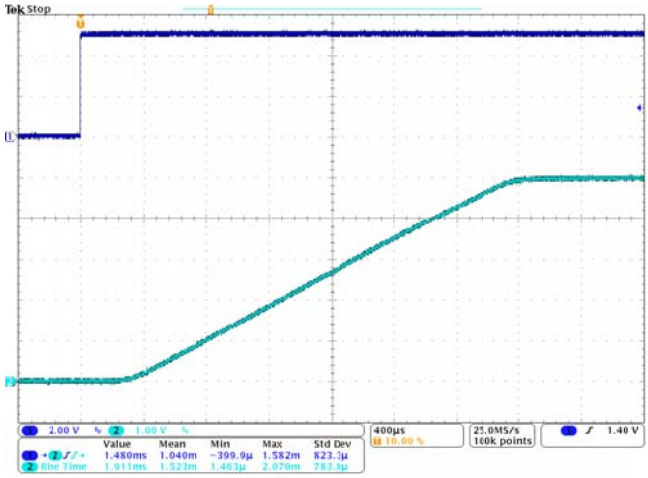


Fig.14 Turn-on Response Time, VIN=5V

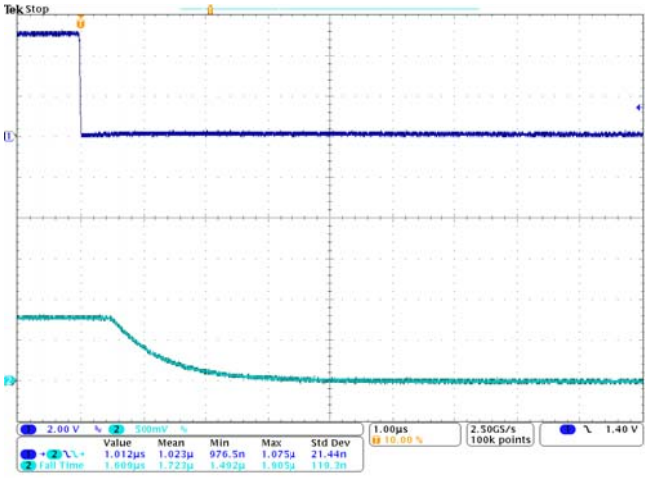


Fig.15 Turn-off Response Time, VIN=0.8V

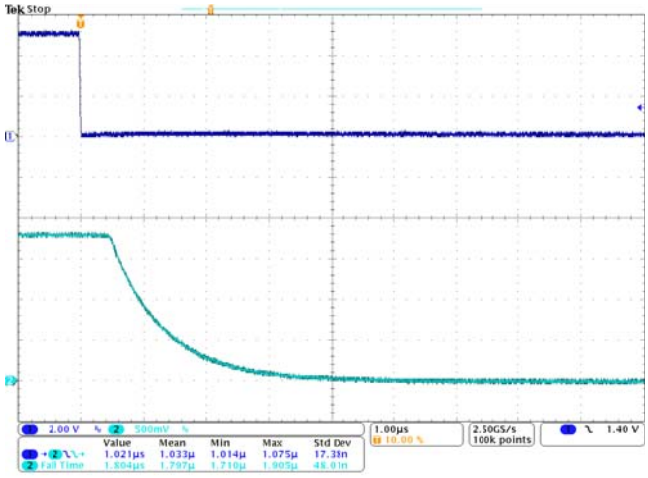


Fig.16 Turn-off Response Time, VIN=1.8V

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Condition: V_{BIAS}=V_{EN}=5V, CT=1nF, C_{IN}=1μF, C_{OUT}=0.1μF, RL=10Ω, ch1:EN, ch2:V_{OUT}

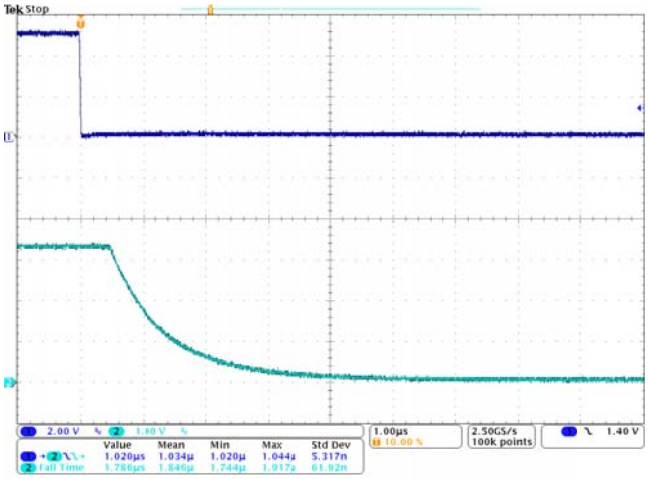


Fig.17 Turn-off Response Time, VIN=3.3V

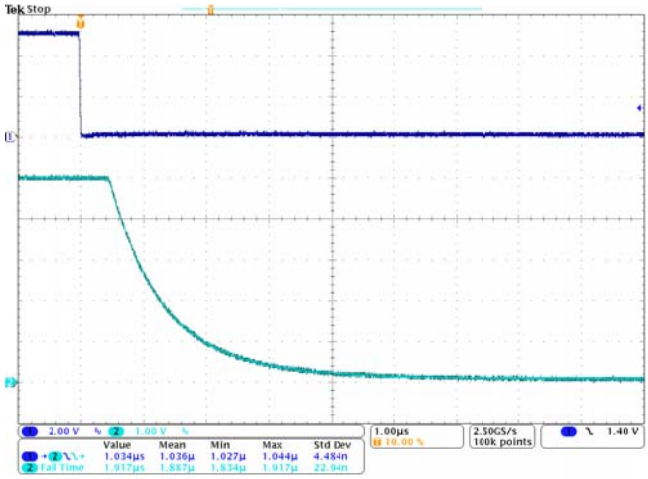


Fig.18 Turn-off Response Time, VIN=5V

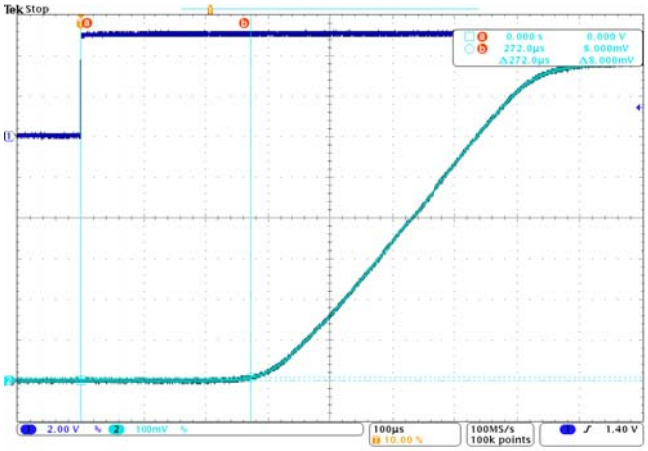


Fig.19 Turn-on Delay Time, VIN=0.8V

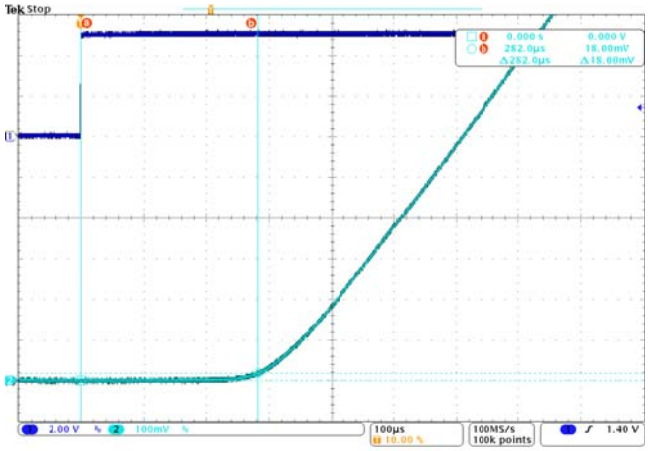


Fig.20 Turn-on Delay Time, VIN=1.8V

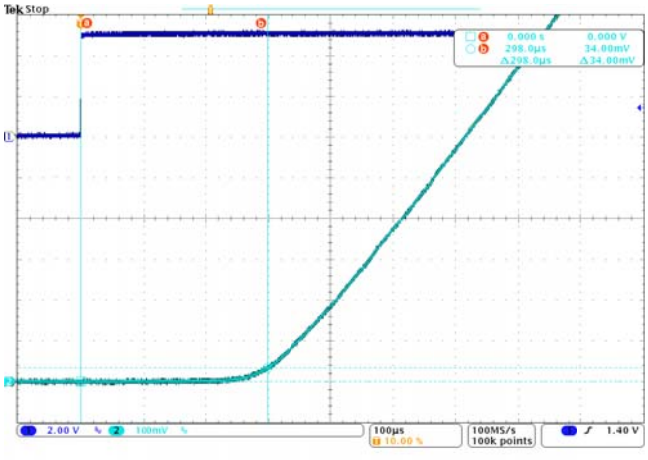


Fig.21 Turn-on Delay Time, VIN=3.3V

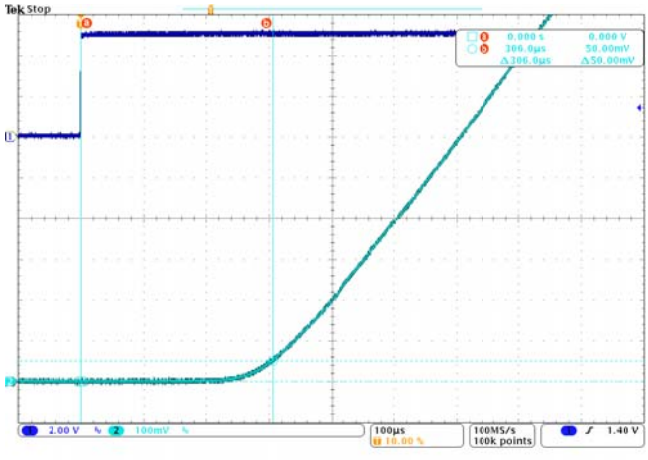


Fig.22 Turn-on Delay Time, VIN=5V

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

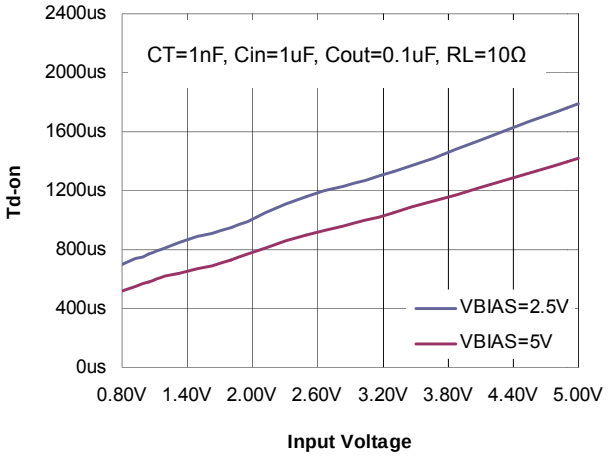


Fig.23 t_{D-ON} vs. VIN

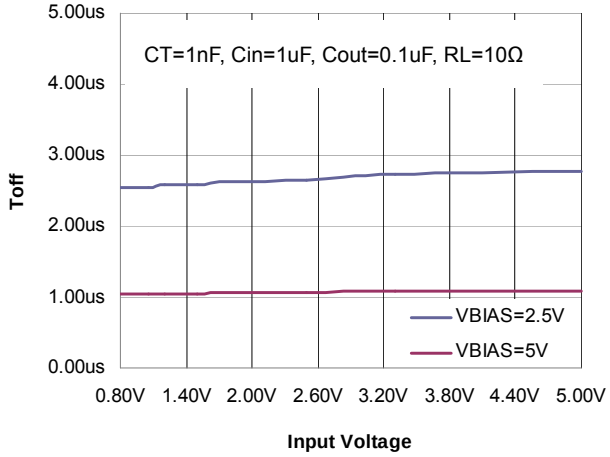


Fig.24 t_{OFF} vs. VIN

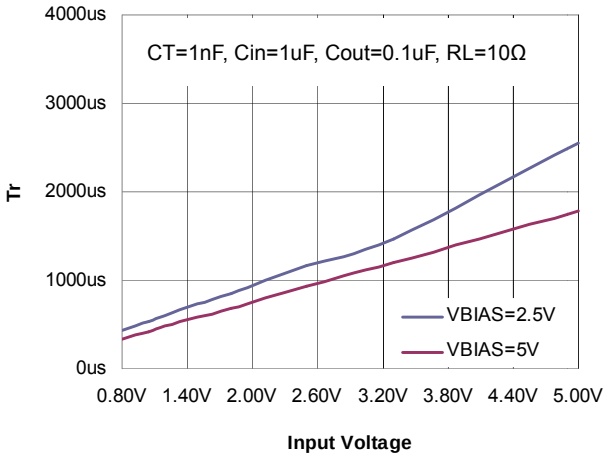


Fig.25 t_R vs. VIN

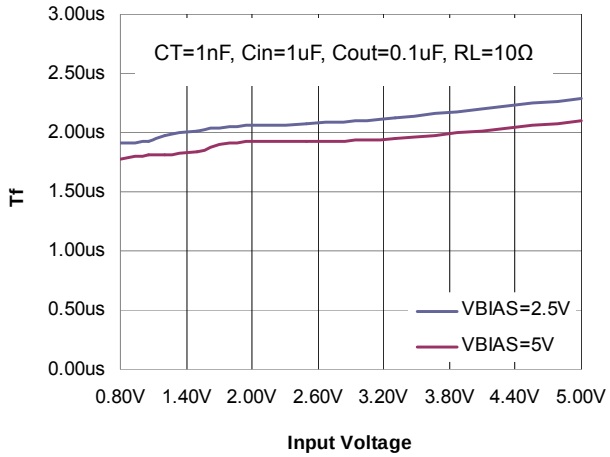


Fig.26 t_F vs. VIN

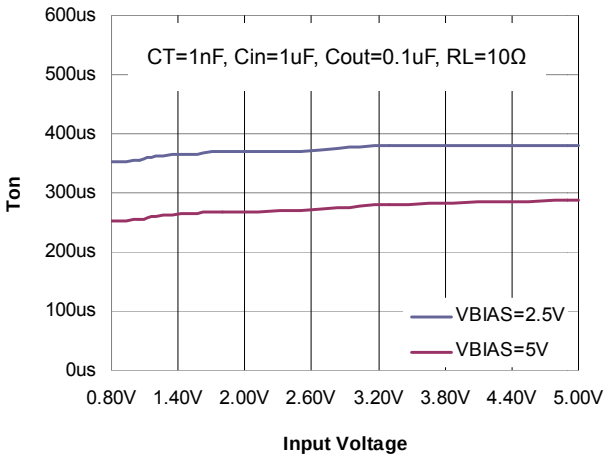


Fig.27 t_{ON} vs. VIN

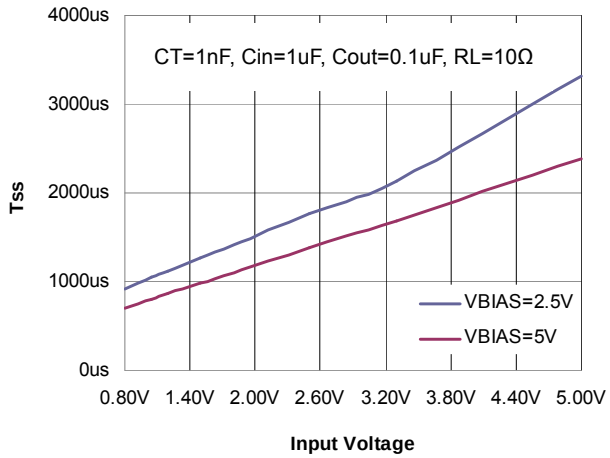


Fig.28 t_{SS} vs. VIN

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

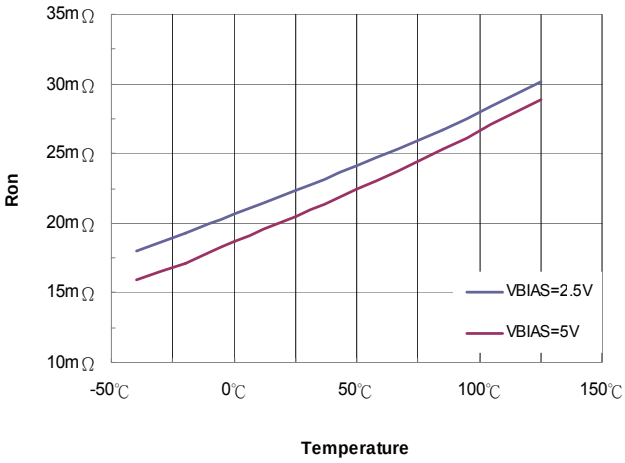


Fig.29 R_{ON} vs. Temperature

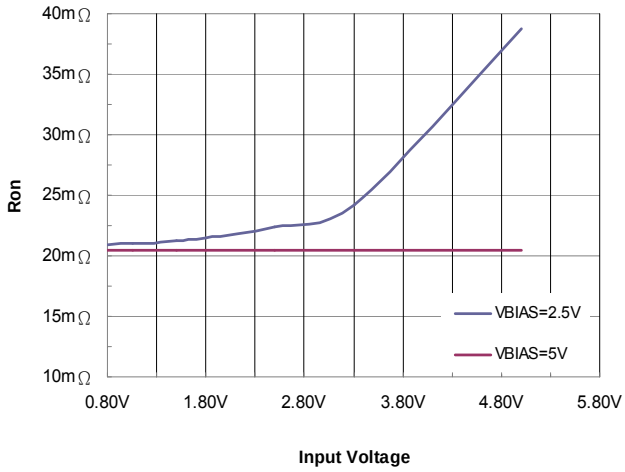


Fig.30 R_{ON} vs. VIN

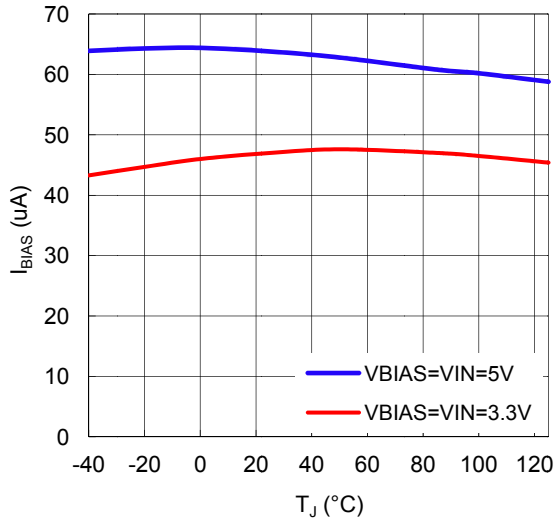


Fig.31 Quiescent Current vs. Temperature

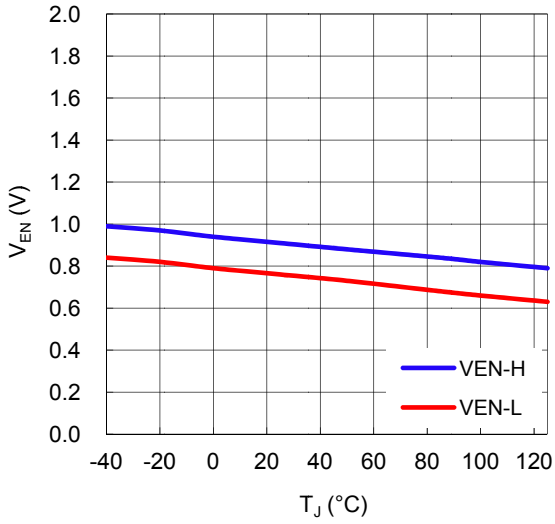


Fig.32 EN Threshold vs. Temperature

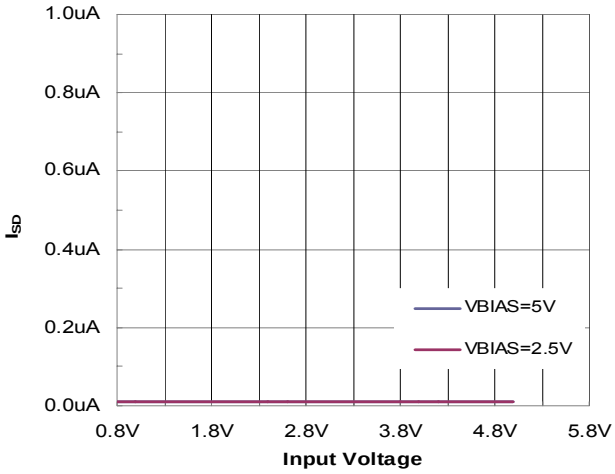


Fig.33 Shutdown Current vs. VIN

APPLICATION INFORMATION

On/Off Control

The load switch is controlled by the EN pin. The EN pin is active high and has a low threshold making it capable of interfacing with low voltage signals. The EN pin can be used with standard 1.2V, 1.8V, 2.5V or 3.3V GPIO logic threshold. Do not leave the EN pin float.

Output Rise Time Control

The rise time of VOUT is adjustable by an external capacitor on the CT pin. The rise time shows on below Table 1 are typical measured value. Please refer it for determined rise time.

VIN	Rise Time，TR(us)，10%~90%，COUT=0.1uF，CIN=1uF							
	T_R							
	VIN=0.8V	VIN=1.05V	VIN=1.2V	VIN=1.5V	VIN=1.8V	VIN=2.5V	VIN=3.3V	VIN=5.0V
0nF	22	26	30	35	38	46	55	75
0.22nF	76	98	115	143	167	232	301	462
0.47nF	136	174	209	261	304	428	559	859
1nF	262	347	412	515	614	847	1111	1712
2.2nF	602	753	902	1136	1348	1835	2493	3884
4.7nF	1246	1638	1832	2312	2742	3906	5146	8084
10nF	2587	3411	3865	4908	5712	8209	10860	17150

<Table 1>

Input Capacitor

An input capacitor is recommended to be placed between VIN and GND to limit the voltage drop on the input supply during high current application.

Output Capacitor

Setting a C_{IN} greater than the C_{OUT} is highly recommended. Since the internal body diode is in the NMOS switch, this prevents the current flows through the body diode from VOUT to VIN when the system supply is removed.

APPLICATION INFORMATION (Continued)

Layout Considerations

Follow the below guidelines for PCB layout to achieve stable operation. Below lists help start layout.

1. The current loop of two load switch should be separated and symmetrized to each other.
2. Keep the high current paths (VIN, VOUT and GND) wide and short to obtain the best effect.
3. The input and output capacitors should be close to the device as possible to minimize the parasitic trace inductances.
4. Place the thermal vias under the exposed pad of the device. This help for thermal diffusion away from the device.

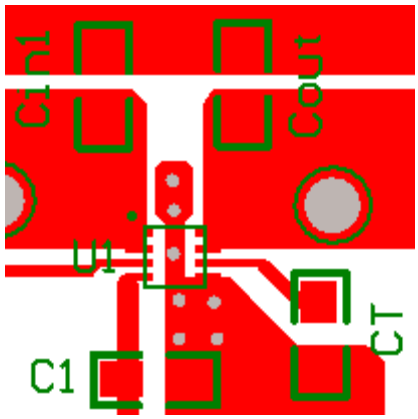


Fig.34 APE8937 Reference Layout

MARKING INFORMATION

DFN 2x2-8L