



## FAST RESPONSE, 6A LOAD SWITCH

### FEATURES

- Integrated 6A Single Channel Load Switch
- Input Voltage Range: 0.8V to 5.5V
- Ultra-low ON-Resistance  $R_{ON} = 4.5m\Omega$
- Low Threshold Control Input
- Quick Output Discharge Transistor
- ESD Performance Tested per JESD 22  
2KV HBM and 1KV CDM
- Halogen Free Product

### APPLICATIONS

- Telecom Systems
- Industrial Systems
- Consumer Electronics
- Notebooks / Netbooks

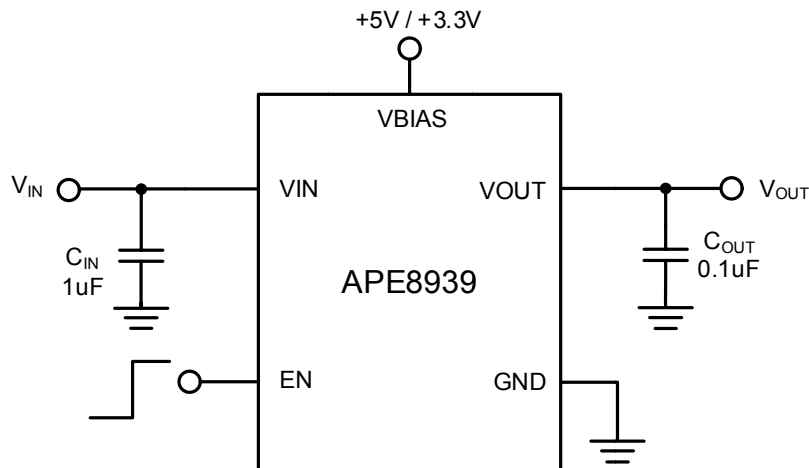
### DESCRIPTION

The APE8939 is a small, ultra-low  $R_{ON}$  load switch with controlled turn on. It contains one N-channel MOSFET that can operate over an input voltage range of 0.8V to 5.5V and support maximum continuous current up to 6A. The switch is controlled by an on/off input (EN), which is capable of interfacing directly with low-voltage control signals.

Additional features include a  $330\Omega$  on-chip load resistor is added for output quick discharge when switch is turned off.

The APE8939 is available in DFN 3x3-8L package with smallest components.

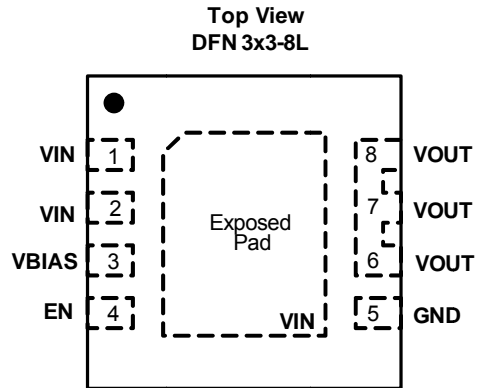
### TYPICAL APPLICATION





ORDERING / PACKAGE INFORMATION

APE8939X Package Type GN3: DFN 3x3-8L



ABSOLUTE MAXIMUM RATINGS (at TA=25°C)

Table of absolute maximum ratings including VIN, VOUT, EN, VBIAS, I\_MAX, Storage Temperature Range, Junction Temperature, Lead Temperature, Thermal Resistance from Junction to Ambient (RθJA), and Thermal Resistance from Junction to Case (RθJC).

RECOMMENDED OPERATING CONDITIONS

Table of recommended operating conditions including VIN, VBIAS, VOUT, CIN, Junction Temperature, Operating Temperature Range, and Power Dissipation (PD@TA=25°C).



**ELECTRICAL SPECIFICATIONS**

( $V_{IN}=0.8V$  to  $5.5V$ ,  $V_{BIAS}=5V$ ,  $C_{IN}=1\mu F$ ,  $C_{OUT}=0.1\mu F$ ,  $T_A=25^\circ C$ , unless otherwise specified)

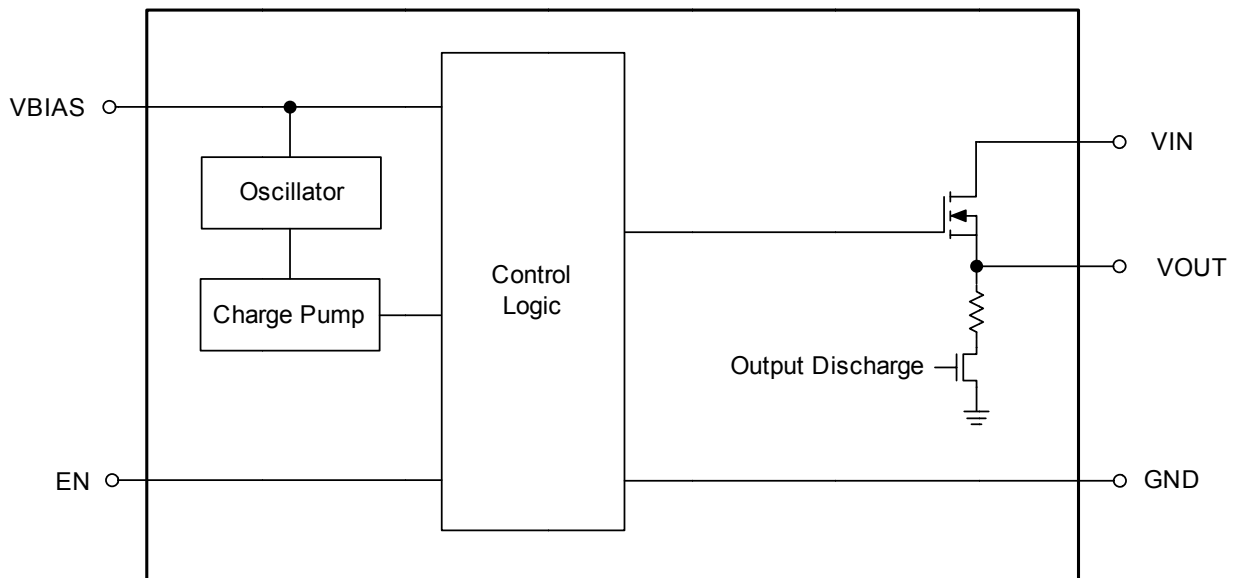
PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNIT
Quiescent Current	$I_{BIAS}$	$V_{BIAS}=V_{IN}=V_{EN}=5V$ , $I_{OUT}=0A$		30	50	$\mu A$
		$V_{BIAS}=V_{IN}=V_{EN}=3.3V$ , $I_{OUT}=0A$		20	33	$\mu A$
Shutdown Current	$I_{SD}$	$V_{EN}=GND$			1	$\mu A$
ON Resistance	$R_{ON}$	$V_{IN}=5V$ , $I_{OUT}=-200mA$		4.9	8	$m\Omega$
		$V_{IN}=5V$ , $I_{OUT}=-200mA$ , $-40^\circ C < T_A < 85^\circ C$			10	$m\Omega$
		$V_{IN}=3.3V$ , $I_{OUT}=-200mA$		4.8	7.8	$m\Omega$
		$V_{IN}=3.3V$ , $I_{OUT}=-200mA$ , $-40^\circ C < T_A < 85^\circ C$			10	$m\Omega$
		$V_{IN}=1.8V$ , $I_{OUT}=-200mA$		4.6	7.3	$m\Omega$
		$V_{IN}=1.8V$ , $I_{OUT}=-200mA$ , $-40^\circ C < T_A < 85^\circ C$			10	$m\Omega$
		$V_{IN}=1.5V$ , $I_{OUT}=-200mA$		4.6	7.3	$m\Omega$
		$V_{IN}=1.5V$ , $I_{OUT}=-200mA$ , $-40^\circ C < T_A < 85^\circ C$			10	$m\Omega$
		$V_{IN}=1.05V$ , $I_{OUT}=-200mA$		4.5	7.2	$m\Omega$
		$V_{IN}=1.05V$ , $I_{OUT}=-200mA$ , $-40^\circ C < T_A < 85^\circ C$			10	$m\Omega$
		$V_{IN}=0.8V$ , $I_{OUT}=-200mA$		4.5	7.2	$m\Omega$
		$V_{IN}=0.8V$ , $I_{OUT}=-200mA$ , $-40^\circ C < T_A < 85^\circ C$			10	$m\Omega$
Rise Time	$t_R$	$V_{IN}=1.05V$ , $R_L=10\Omega$	7	14	20	$\mu s$
Soft-Start Time	$t_{SS}$	$V_{IN}=1.05V$ , $R_L=10\Omega$		40	50	$\mu s$
Output Pull-Down Resistance	$R_{OPD}$	$V_{IN}=5V$ , $V_{EN}=0V$		330	400	$\Omega$
EN Input Leakage Current	$I_{EN}$	$V_{EN}=5V$ or $GND$			1	$\mu A$
EN Threshold	$V_{IH}$	on	1.3			V
	$V_{IL}$	off			0.5	V



### PIN DESCRIPTIONS

PIN No.	PIN SYMBOL	PIN DESCRIPTION
1, 2	VIN	Input Power Supply
3	VBIAS	Bias Voltage
4	EN	Switch control input, active high. Do not leave floating.
5	GND	Ground
6, 7, 8	VOUT	Switch output
Exposed pad	VIN	Input Power Supply

### BLOCK DIAGRAM





### TYPICAL PERFORMANCE CHARACTERISTICS

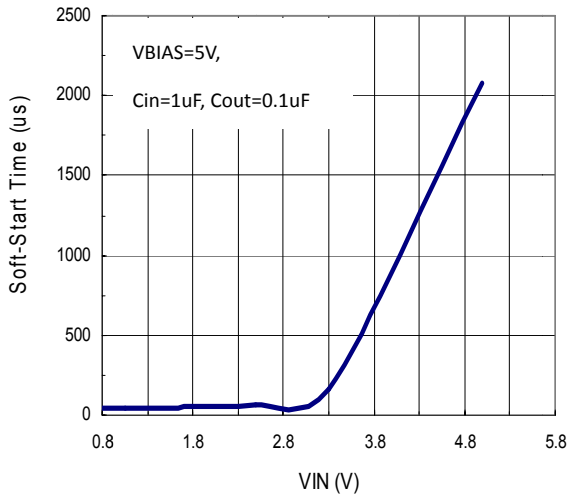


Fig.1 Soft-Start Time vs.  $V_{IN}$

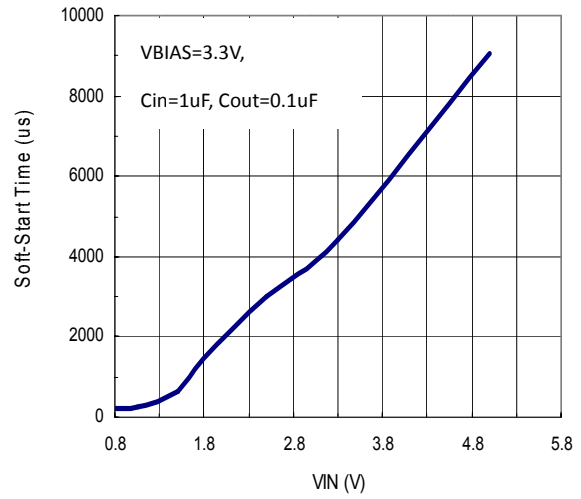


Fig.2 Soft-Start Time vs.  $V_{IN}$

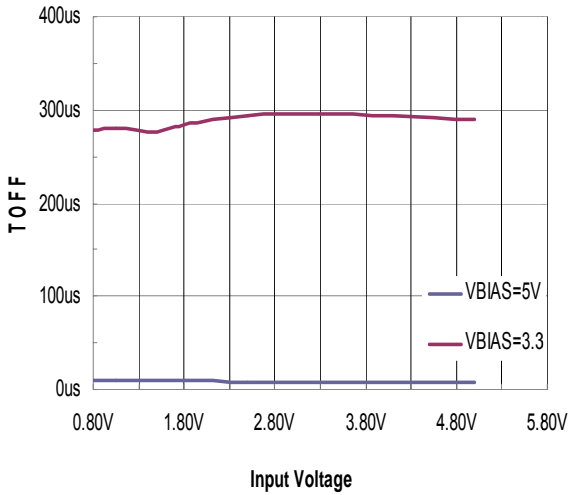


Fig.3  $T_{OFF}$  vs.  $V_{IN}$

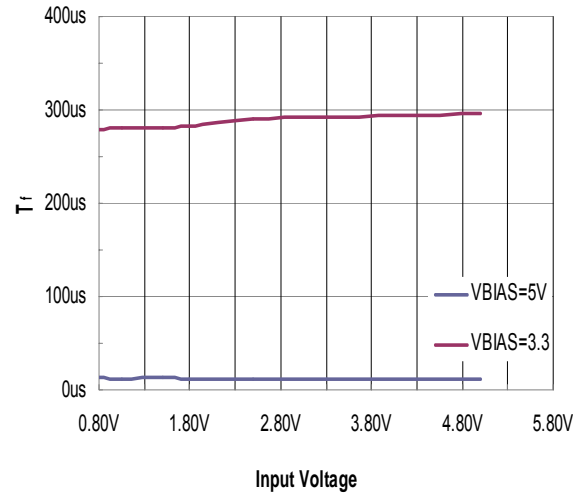


Fig.4  $T_f$  vs.  $V_{IN}$

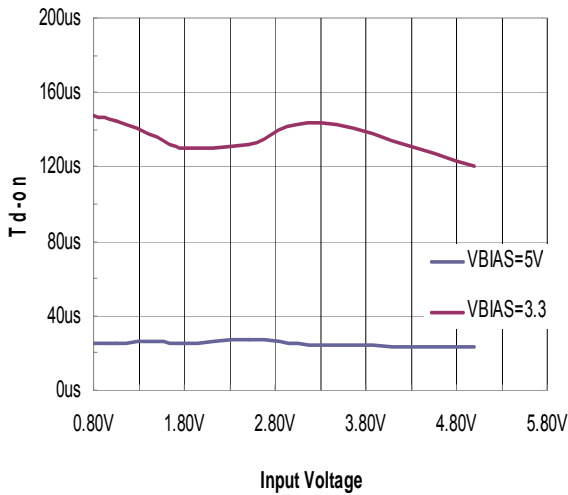


Fig.5  $T_{d-on}$  vs.  $V_{IN}$

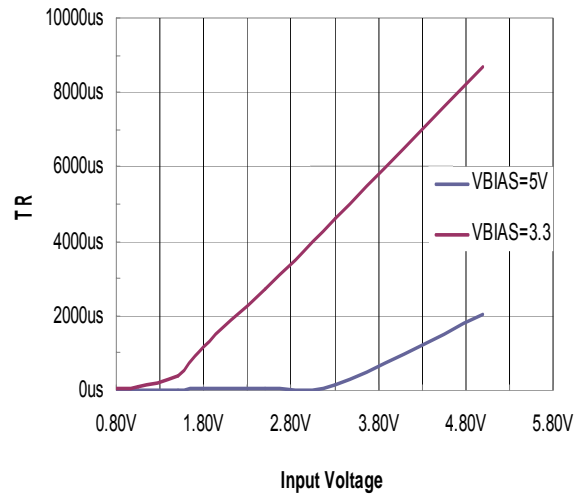


Fig.6  $T_R$  vs.  $V_{IN}$



### TYPICAL PERFORMANCE CHARACTERISTICS

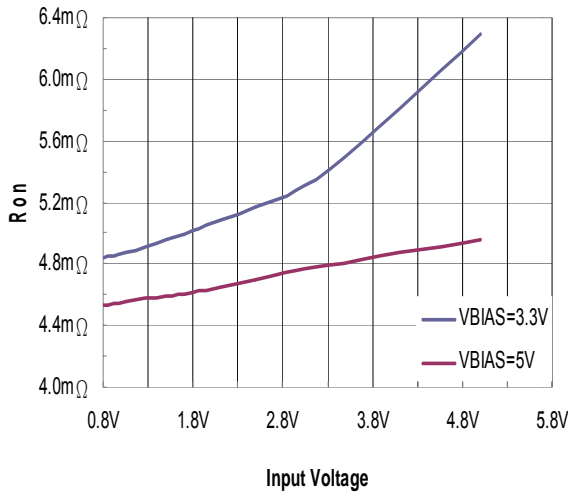


Fig.7  $R_{ON}$  vs.  $V_{IN}$

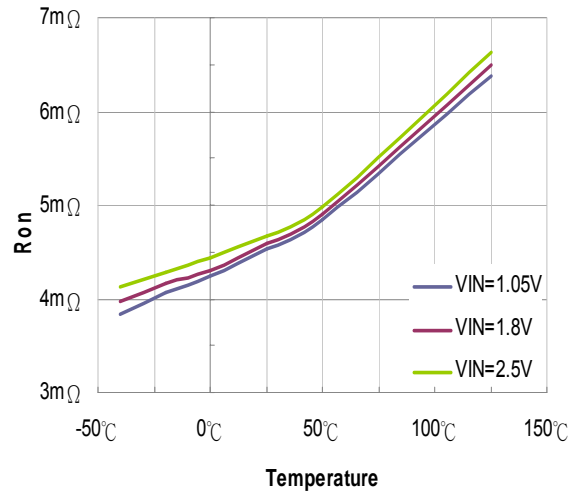


Fig.8  $R_{ON}$  vs. Temperature

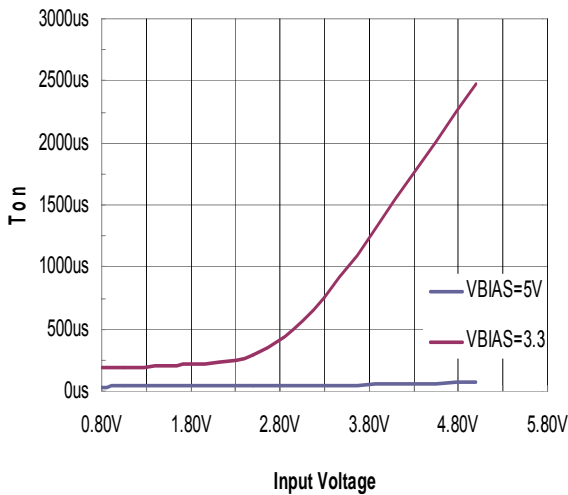


Fig.9  $T_{ON}$  vs.  $V_{IN}$

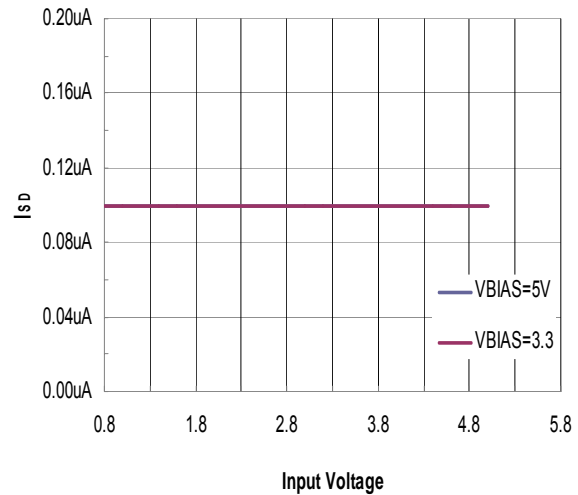


Fig.10  $I_{SD}$  vs.  $V_{IN}$

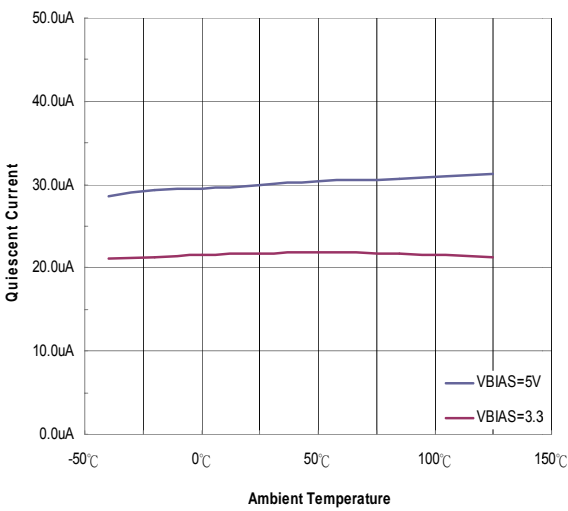


Fig.11 VBIAS Current vs. Temperature

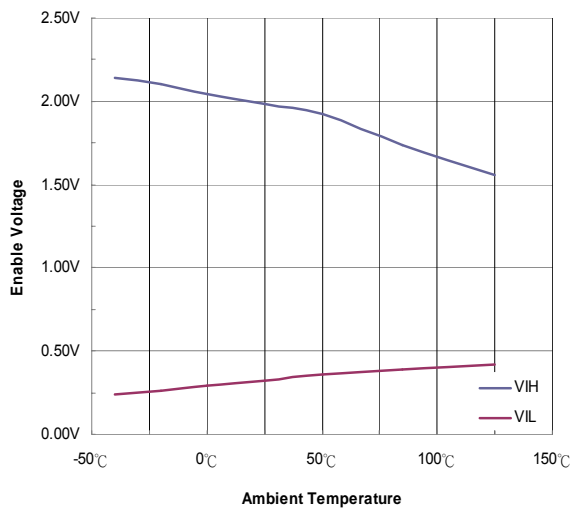


Fig.12 EN Threshold vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS

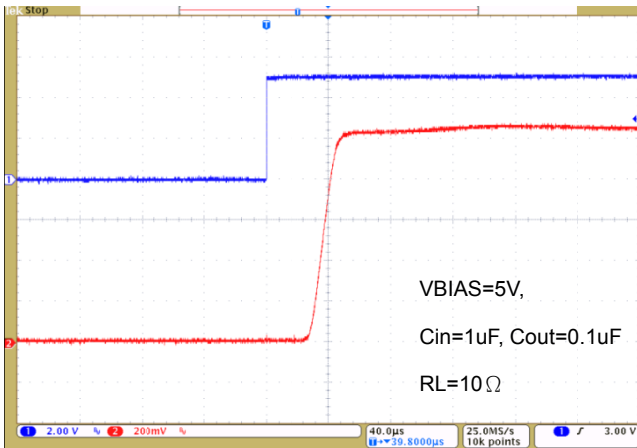


Fig.13 Enable Waveform, VIN=1.05V

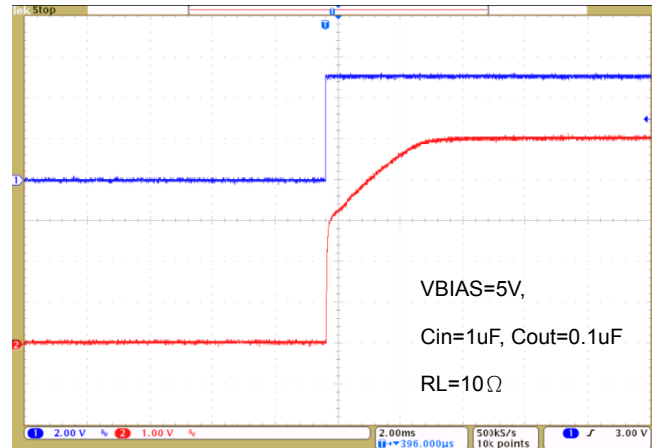


Fig.14 Enable Waveform, VIN=5V

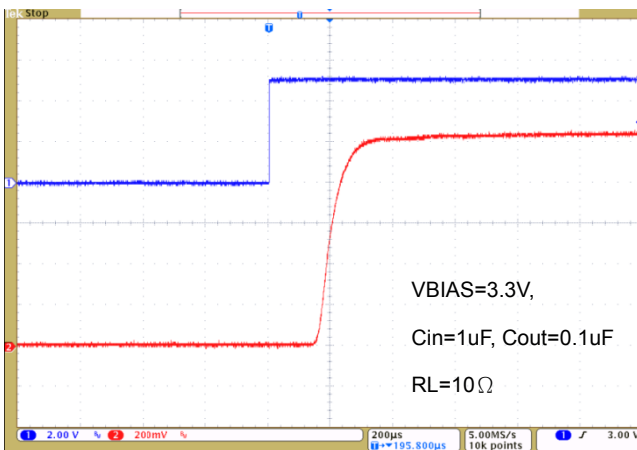


Fig.15 Enable Waveform, VIN=1.05V

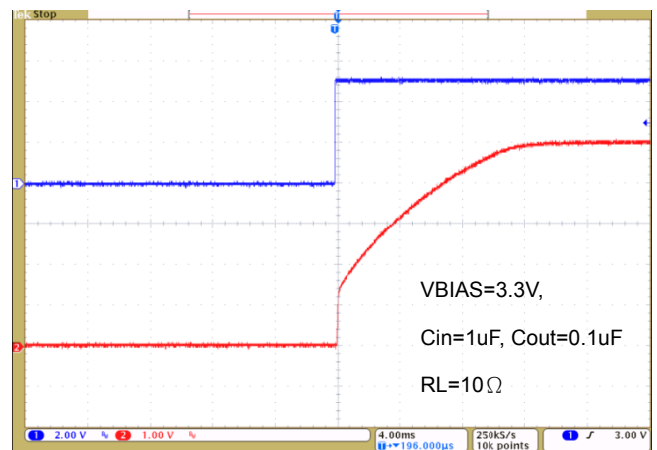


Fig.16 Enable Waveform, VIN=5.0V



### APPLICATION INFORMATION

#### On/Off Control

The load switch is controlled by the EN pin. The EN pin is active high and has a low threshold making it capable of interfacing with low voltage signals. The EN pin can be used with standard 1.5V, 1.8V, 2.5V or 3.3V GPIO logic threshold. Do not leave the EN pin float.

The Figure17 shows the VOUT on/off definition.

$t_{SS}$ : Soft start time

$t_{D-ON}$ : VOUT turn on delay

$t_R$ : VOUT rise time

$t_{D-OFF}$ : VOUT turn off delay

$t_F$ : VOUT fall time

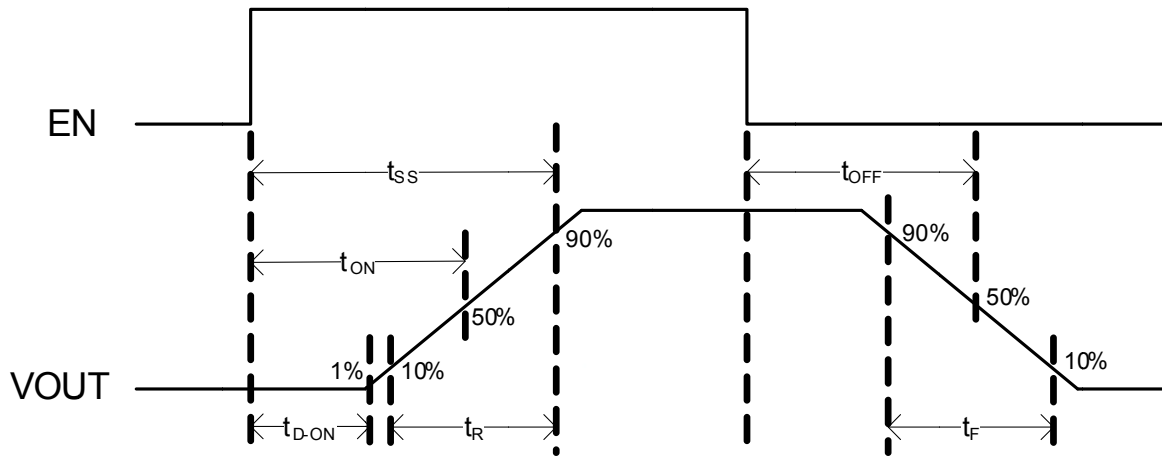


Fig.17 ON/OFF Waveform

#### Output Switch Time Control

The switch time shows on below Table 1 are typical measured value. Please refer it for determined rise time.

VIN	VBIAS=5V					
	VOUT					
	Td-on(us)	Tr(us)	Tss(us)	Ton(us)	Toff(us)	Tf(us)
0.80V	25	11	41	34	9	13.2
1.05V	25	14	43	36	9	11.4
1.50V	26	19	48	39	8.88	12.7
1.80V	25	26	57	40	8.96	12.2
2.50V	26	40	68	43	8.54	11.8
3.30V	24	127	164	48	8.32	11.1
5.00V	23	2055	2080	68	7.9	12.2

Table 1





**Input Capacitor**

An input capacitor is recommended to be placed between VIN and GND to limit the voltage drop on the input supply during high current application.

**Output Capacitor**

Setting a  $C_{IN}$  greater than the  $C_{OUT}$  is highly recommended. Since the internal body diode is in the NMOS switch, this prevents the current flows through the body diode from VOUT to VIN when the system supply is removed.

**Layout Considerations**

Follow the below guidelines for PCB layout to achieve stable operation. Take below figure for reference.

1. Keep the high current paths (VIN, VOUT and GND) wide and short to obtain the best effect.
2. The input and output capacitors should be close to the device as possible to minimize the parasitic trace inductances.
3. Place the thermal vias under the exposed pad. This help for thermal diffusion away from the device.

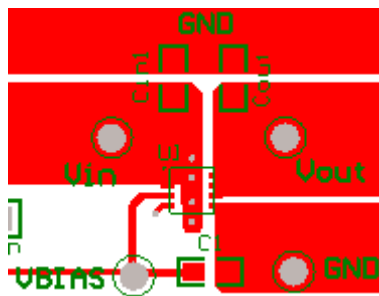


Fig.18 Reference layout



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**MARKING INFORMATION**

DFN 3x3-8L

