ULTRA- LOW ON RESISTANCE, 3A LOAD SWITCH WITH CONTROLLED TURN-ON

FEATURES

- Integrated 3A Single Channel Load Switch
- Input Voltage Range: 6V to 13.2V
- Low Threshold Control Input
- Quick Output Discharge Transistor
- Over-Temperature Protection
- Over Current Protection
- Short Circuit Protection
- Low ON-Resistance R_{ON} = 21mΩ
- Halogen Free Product

APPLICATIONS

- Telecom Systems
- Industrial Systems
- Set-Top-Box
- Consumer Electronics
- Notebooks / Netbooks

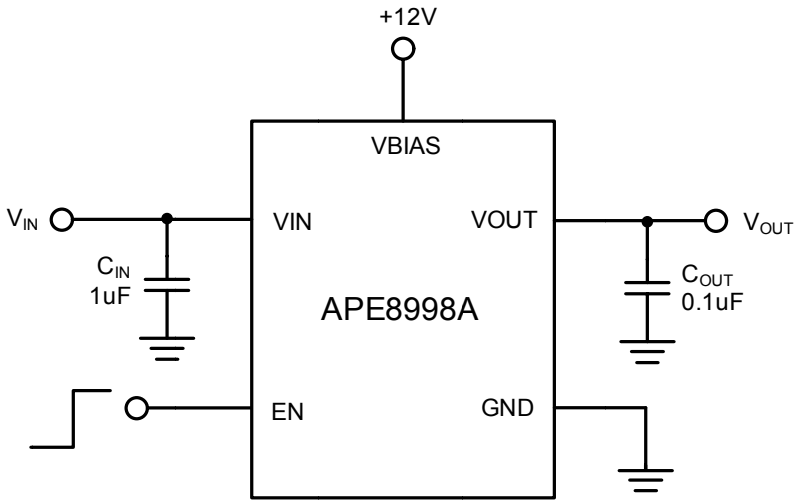
DESCRIPTION

The APE8998A is a small, ultra-low R_{ON} load switch with controlled turn on. It contains one N-channel MOSFET that can operate over an input voltage range of 6V to 13.2V and support maximum continuous current up to 3A. The switch is controlled by an on/off input (EN), which is capable of interfacing directly with low-voltage control signals.

Additional features include a 330Ω on-chip load resistor is added for output quick discharge when switch is turned off. A well protection of APE8998A is equipped when the device enters hard short circuit or current limit and thermal shutdown.

The APE8998A is available in ESOP-8 package with smallest components.

TYPICAL APPLICATION

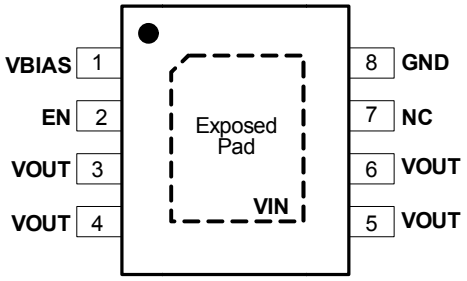


ORDERING / PACKAGE INFORMATION

APE8998AX

Package Type
MP: ESOP-8L

Top View
ESOP-8L



ABSOLUTE MAXIMUM RATINGS (at T_A=25°C)

VIN	-0.3V to 17.5V
VOUT	V_{IN}+0.3V
EN	-0.3V to 17.5V
VBIAS	-0.3+17.5V
Storage Temperature Range (T_{ST})	-65 to +150°C
Junction Temperature (T_J)	150°C
Lead Temperature (Soldering, 10sec.)	260°C
Thermal Resistance from Junction to Ambient ($R\theta_{JA}$)	
ESOP-8L.....	50°C/W

RECOMMENDED OPERATING CONDITIONS

VIN	6V to 13.2V
VBIAS	6V to 13.2V (VBIAS≧VIN)
VOUT	V_{IN}
CIN	≧0.1uF
Junction Temperature (T_J)	125°C
Operating Temperature Range (T_A)	-40°C to 85°C

ELECTRICAL SPECIFICATIONS

(V_{IN}=6V to 13.2V, V_{BIAS}=12V, C_{IN}=1uF, C_{OUT}=0.1uF, T_A =25°C, unless otherwise specified)

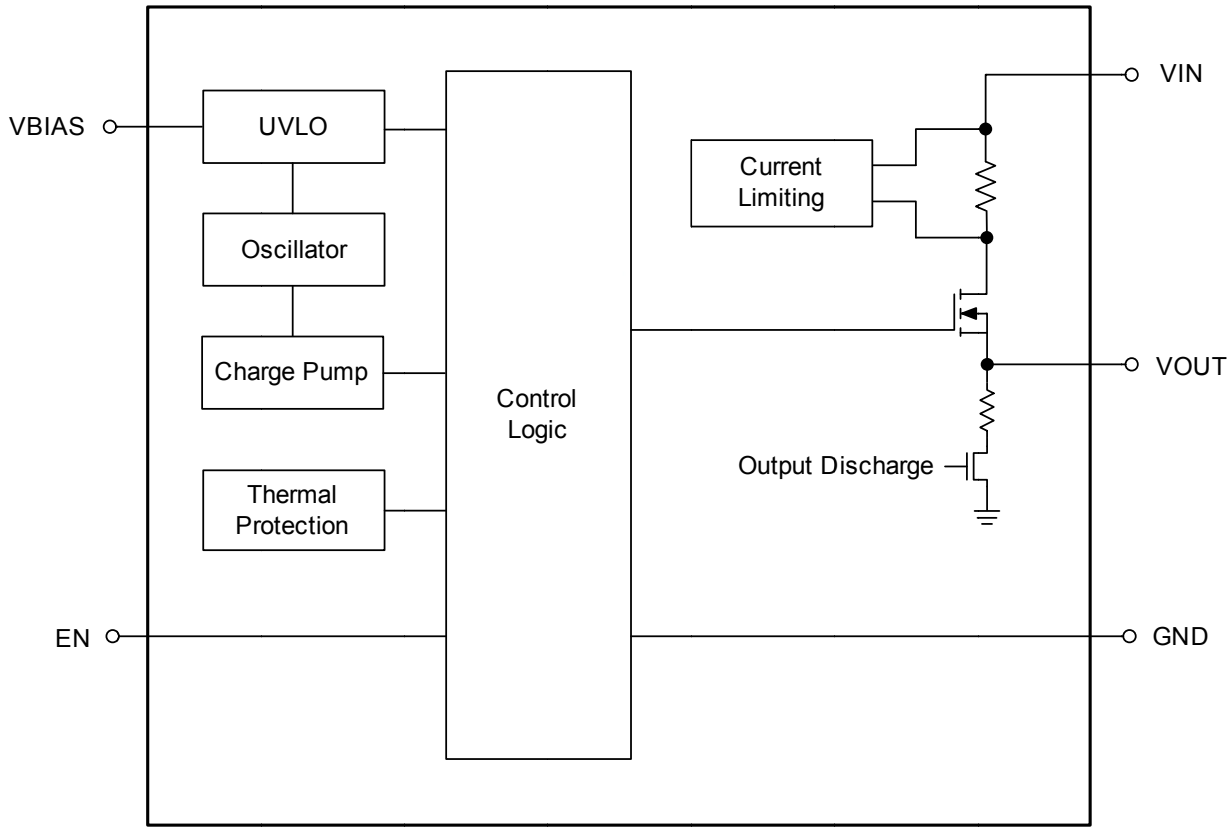
PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNIT
Quiescent Current	I_{BIAS}	V_{BIAS}=V_{EN}=12V, I_{OUT}=0A		50	80	uA
Shutdown Current	I_{SD}	V_{EN}=GND			1	uA
Under-Voltage Lockout	V_{UVLO}	Threshold	3.0	3.6	4.2	V
	V_{HYS}	Hysteresis		0.4		V
Switch ON Resistance	R_{ON}	V_{IN}=V_{BIAS}=12V, I_{OUT}=200mA		21	26	mΩ
Current Limit Threshold	I_{LM}		3.5		7	A
VOUT Rise Time	t_{SS}	V_{IN}=12V		4		ms
Output Pull-Down Resistance	R_{OPD}	V_{IN}=12V, V_{EN}=0V		330	400	Ω
EN Input Leakage Current	I_{EN}	V_{EN}=5V or GND			1	uA
EN Threshold	V_{IH}	on	1.6			V
	V_{IL}	off			0.6	V
Thermal Shutdown Threshold (Note1)	T_{SD}			140		°C
				30		°C

Note1: Guarantee by design, not production tested.

PIN DESCRIPTIONS

PIN No.	PIN SYMBOL	PIN DESCRIPTION
1	VBIAS	Bias Voltage.
2	EN	Switch control input, active high. Do not leave floating.
3,4,5,6	VOUT	Switch output.
7	NC	No connect.
8	GND	Ground.
Exposed pad	VIN	Input Power Supply.

BLOCK DIAGRAM



TYPICAL PERFORMANCE CHARACTERISTICS

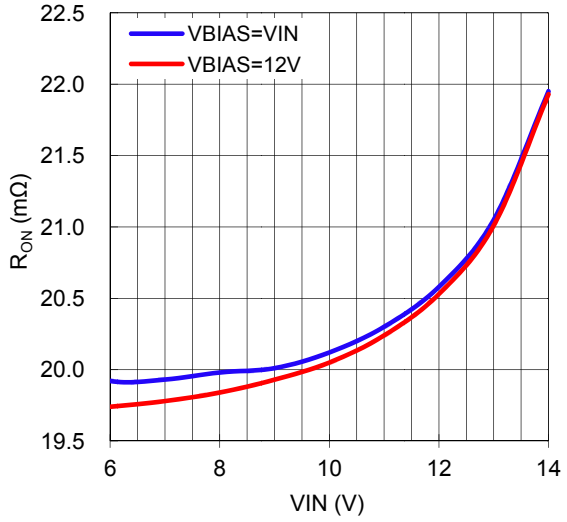


Fig.1 R_{ON} vs. V_{IN}

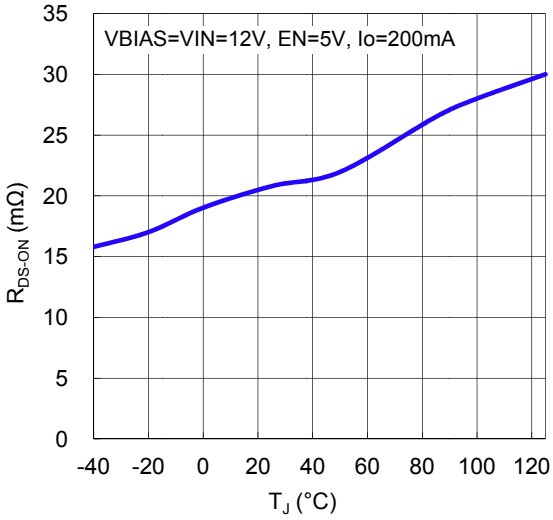


Fig.2 R_{ON} vs. Temperature

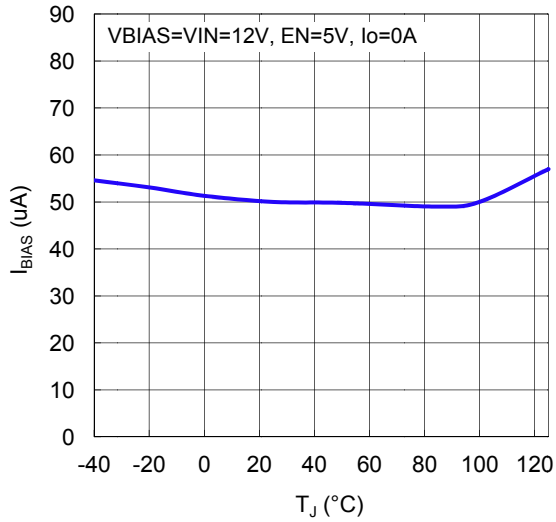


Fig.3 VBIAS Current vs. Temperature

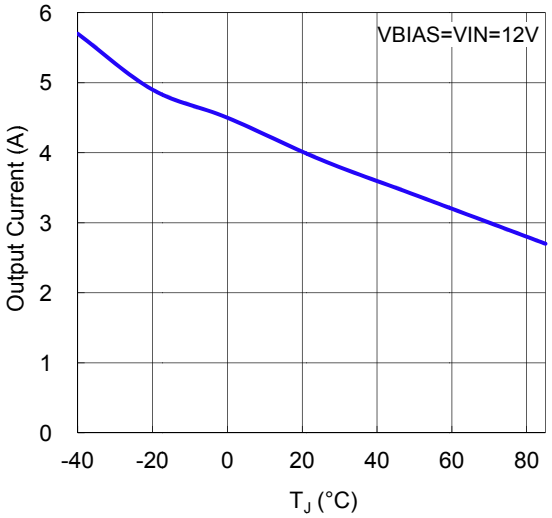


Fig.4 Current Limit vs. Temperature

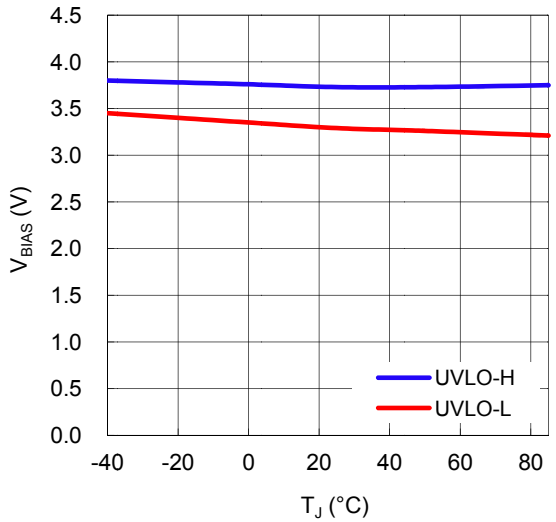


Fig.5 UVLO Threshold vs. Temperature

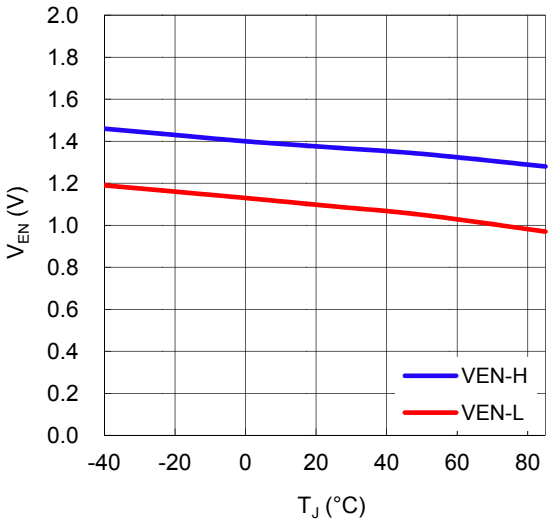


Fig.6 EN Threshold vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

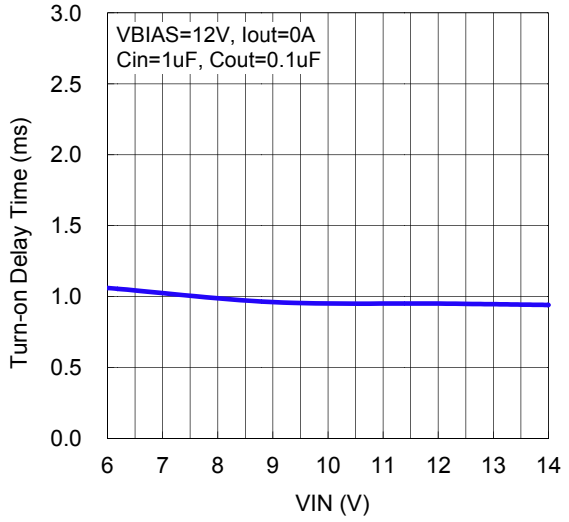


Fig.7 VOUT Turn-On Delay Time

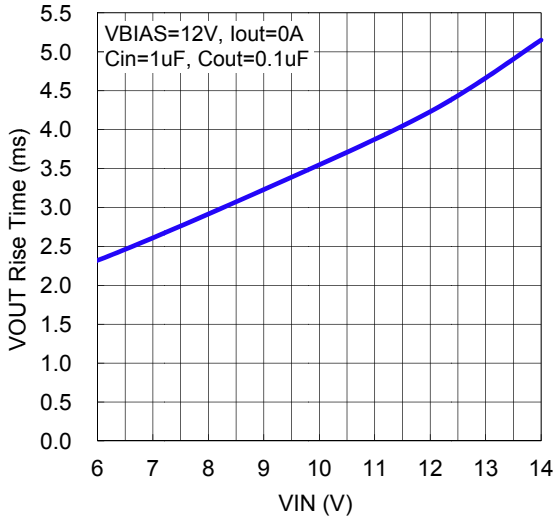


Fig.8 VOUT Rise Time

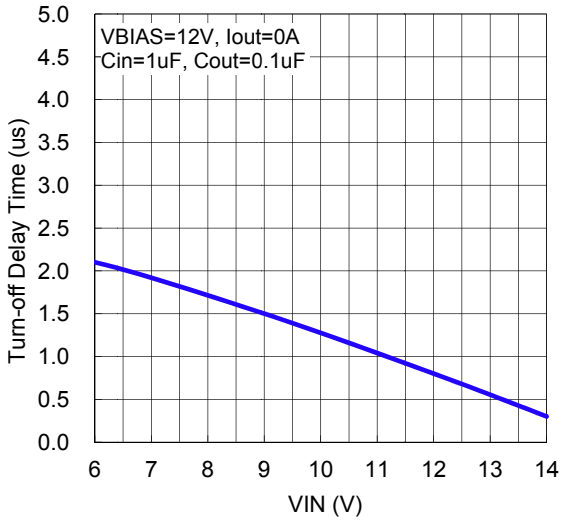


Fig.9 VOUT Turn-Off Delay Time

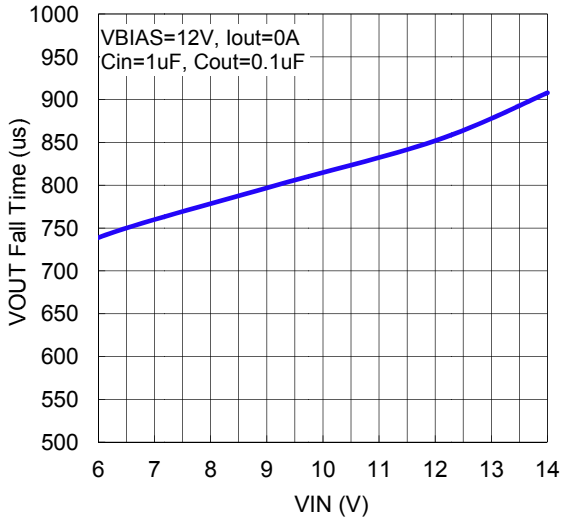


Fig.10 VOUT Fall Time

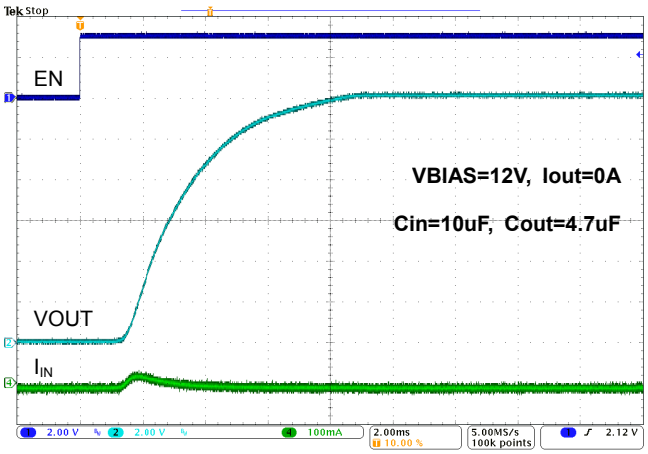


Fig.11 Enable Waveform, VIN=12V

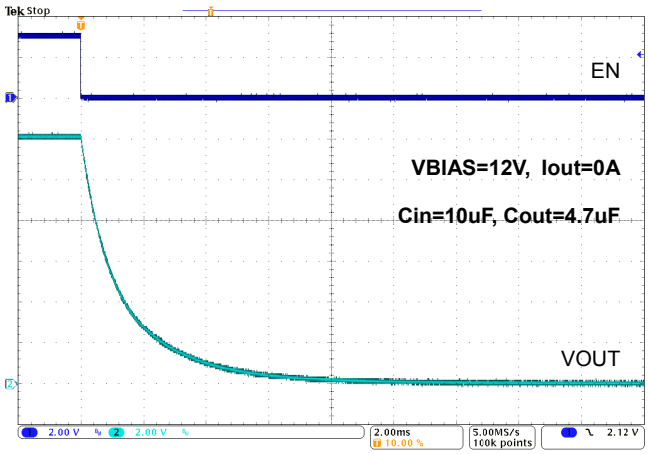


Fig.12 Disable Waveform, VIN=12V

APPLICATION INFORMATION

On/Off Control

The load switch is controlled by the EN pin. The EN pin is active high and has a low threshold making it capable of interfacing with low voltage signals. The EN pin can be used with standard 1.8V, 2.5V or 3.3V GPIO logic threshold. Do not leave the EN pin float.

The Figure13 shows the VOUT on/off definition.

t_{D-ON}: VOUT turn-on delay time

t_R: VOUT rise time

t_{D-OFF}: VOUT turn-off delay time

t_F: VOUT fall time

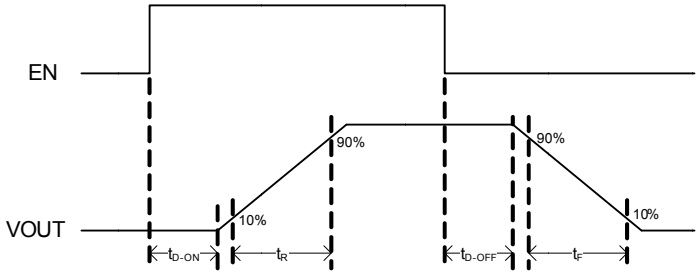


Fig.13 ON/OFF Waveform

Input Capacitor

An input capacitor is recommended to be placed between VIN and GND to limit the voltage drop on the input supply during high current application.

Output Capacitor

Setting a C_{IN} greater than the C_{OUT} is highly recommended. Since the internal body diode is in the NMOS switch, this prevents the current flows through the body diode from VOUT to VIN when the system supply is removed.

Layout Considerations

Follow the below guidelines for PCB layout to achieve stable operation. Take below figure for reference.

1. Keep the high current paths (VIN, VOUT and GND) wide and short to obtain the best effect.
2. The input and output capacitors should be close to the device as possible to minimize the parasitic trace inductances.

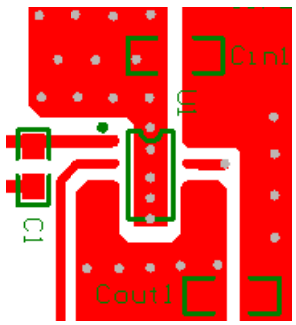


Fig.14 Reference layout

MARKING INFORMATION

ESOP-8L