

## 120V N-Channel Enhancement Mode MOSFET

### Description

The APG120N12P/T uses advanced **SGT II** technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

### General Features

$V_{DS} = 120V$   $I_D = 120A$

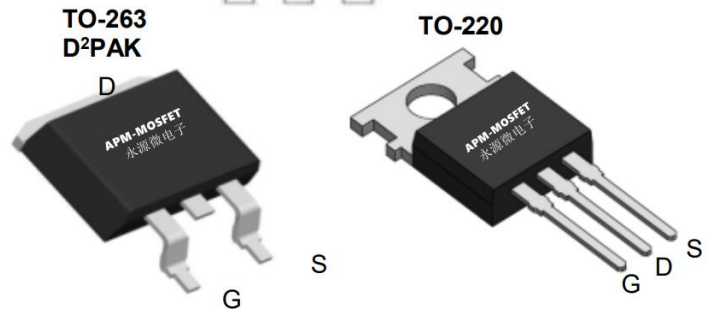
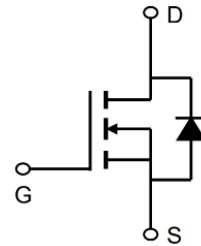
$R_{DS(ON)} < 6.8m\Omega$  @  $V_{GS}=10V$  (Type: **6.0m $\Omega$** )

### Application

Mobile phone fast charging

Brushless motor

Home appliance control board



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
APG120N12P	TO-220-3L	APG120N12P XXX YYYY	1000
APG120N12T	TO-263-3L	APG120N12T XXX YYYY	800

### Absolute Maximum Ratings ( $T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Value	Units
$V_{DS}$	Drain-to-Source Voltage	120	V
$I_D @ T_A=25^\circ C$	Continuous Drain Current <sup>1</sup>	120	A
$I_D @ T_A=100^\circ C$	Continuous Drain Current <sup>1</sup>	60	A
$IDM^{a1}$	Pulsed Drain Current	320	A
EASa2	Single pulse avalanche energy	240	mJ
IAR	Single pulse avalanche current	40	A
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$P_D$	Power Dissipation	125	W
$T_J, T_{stg}$	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ C$
$T_L$	Maximum Temperature for Soldering	300	$^\circ C$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.0	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	50	$^\circ C/W$

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### Electrical Characteristics (T<sub>J</sub>=25°C, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
VDSS	Drain to Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	120	135	--	V
IDSS	Drain to Source Leakage Current	V <sub>DS</sub> = 120V, V <sub>GS</sub> = 0V	--	--	1	μA
IGSS(F)	Gate to Source Forward Leakage	V <sub>GS</sub> =+20V	--	--	100	nA
IGSS(R)	Gate to Source Reverse Leakage	V <sub>GS</sub> =-20V	--	--	-100	nA
VGS(TH)	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> = 250μA	1.2	1.8	3.0	V
RDS(ON)1	Drain-to-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =20A	--	6.0	6.8	mΩ
RDS(ON)1	Drain-to-Source On-Resistance	V <sub>GS</sub> =4.5V, I <sub>D</sub> =10A	--	8.5	10	mΩ
gFS	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =50A		130	--	S
Ciss	Input Capacitance	V <sub>GS</sub> = 0V V <sub>DS</sub> = 50V f = 1.0MHz	--	4282	--	pF
Coss	Output Capacitance		--	429	--	pF
Crss	Reverse Transfer Capacitance		--	17	--	pF
R <sub>g</sub>	Gate resistance		--	2.5	--	Ω
td(ON)	Turn-on Delay Time	I <sub>D</sub> =20A V <sub>DS</sub> = 50V V <sub>GS</sub> = 10V R <sub>G</sub> = 5Ω	--	20	--	ns
tr	Rise Time		--	11	--	ns
td(OFF)	Turn-Off Delay Time		--	55	--	ns
tf	Fall Time		--	28	--	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> =0~10V V <sub>DS</sub> = 50V I <sub>D</sub> =20A	--	61.4	--	nC
Q <sub>gs</sub>	Gate Source Charge		--	17.4	--	nC
Q <sub>gd</sub>	Gate Drain Charge		--	14.1	--	nC
I <sub>S</sub>	Diode Forward Current	T <sub>C</sub> =25 °C	--	--	100	A
ISM	Diode Pulse Current		--	--	320	A
VSD	Diode Forward Voltage	I <sub>S</sub> =6.0A, V <sub>GS</sub> =0V	--	--	1.2	V
trr	Reverse Recovery time	I <sub>S</sub> =20A, V <sub>DD</sub> =50V dI <sub>F</sub> /dt=100A/μs	--	100	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge		--	250	--	nC

#### Note :

- 1、 The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.
- 2、 The data tested by pulsed , pulse width  $\leq$  300us , duty cycle  $\leq$  2%
- 3、 The EAS data shows Max. rating . The test condition is VDD=50V, L=0.3mH, R<sub>g</sub>=25Ω, Starting T<sub>J</sub>=25 °C
- 4、 The power dissipation is limited by 150°C junction temperature

### Typical Characteristics

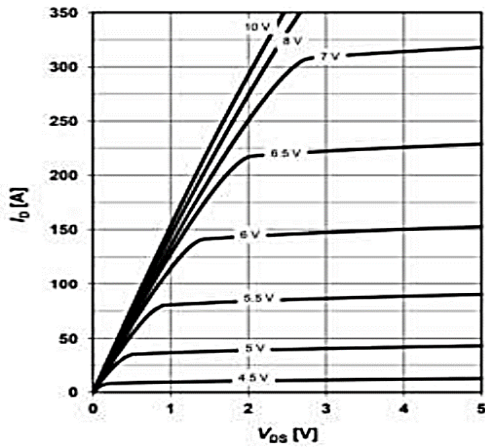


Figure1: output characteristics

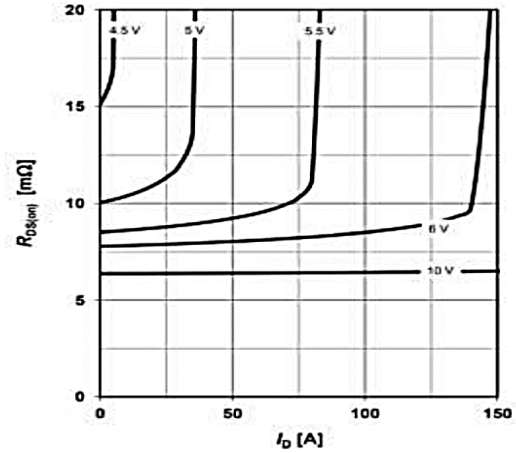


Figure2: Typical drain-source on resistance

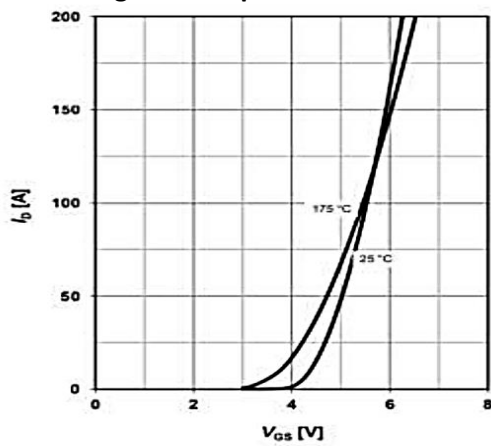


Figure3: transfer characteristics

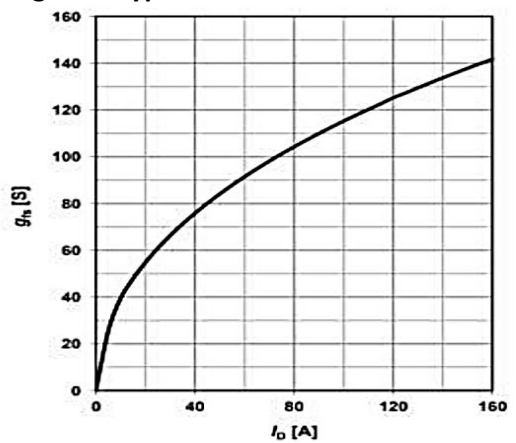


Figure4: forward transconductance

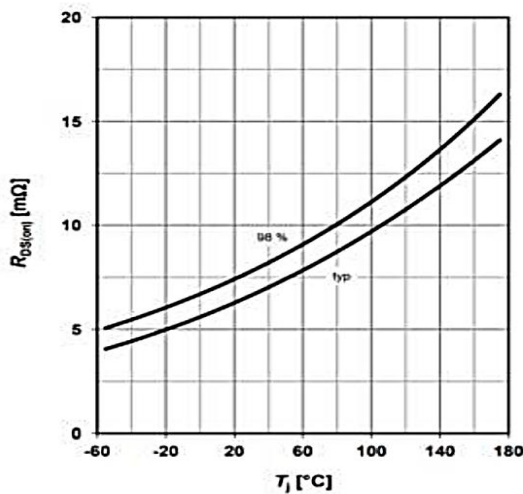


Figure5: Drain-source on-state resistance

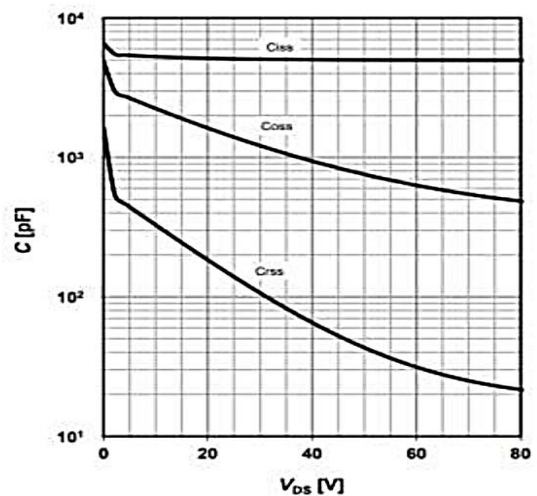


Figure6: Typ. capacitances

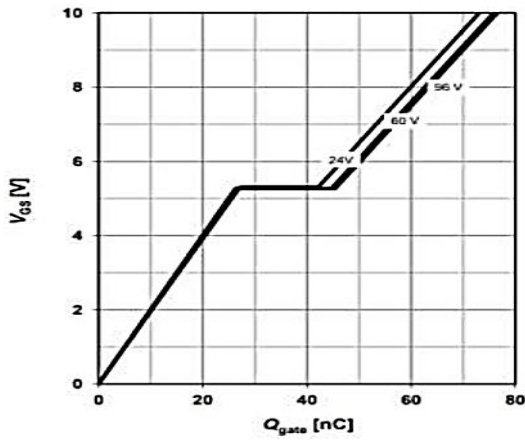


Figure7: Typ. gate charge

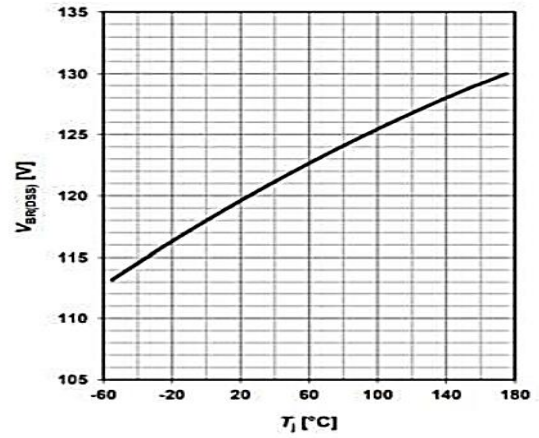


Figure8: Drain-source breakdown voltage

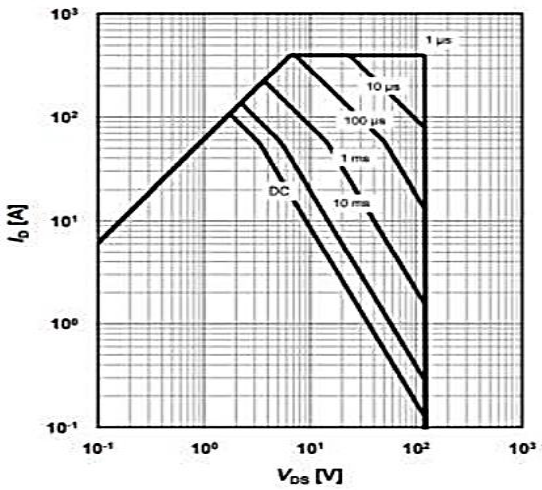


Figure9: Safe operating area

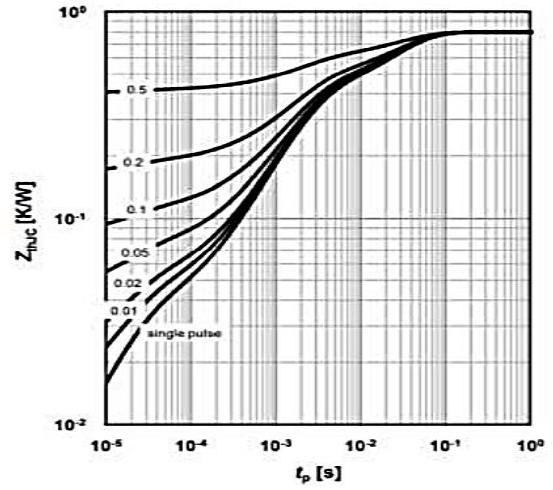
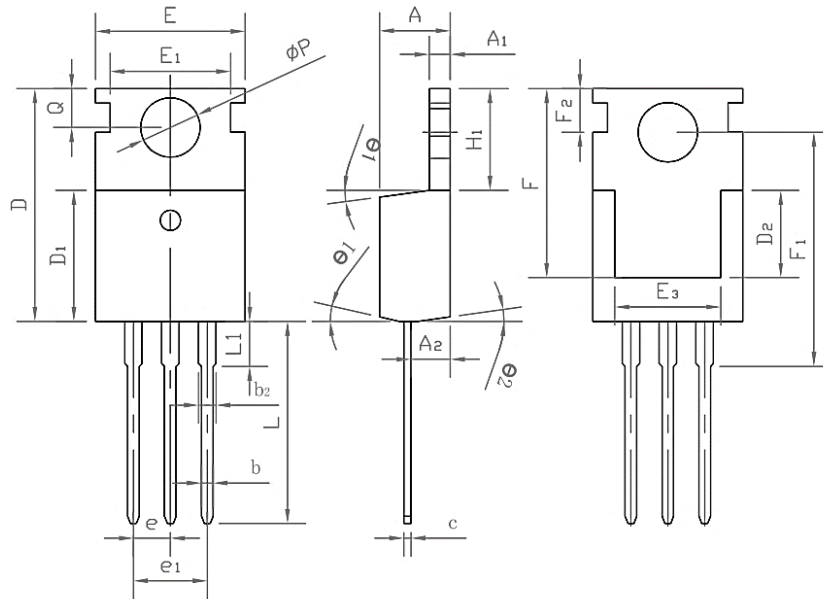


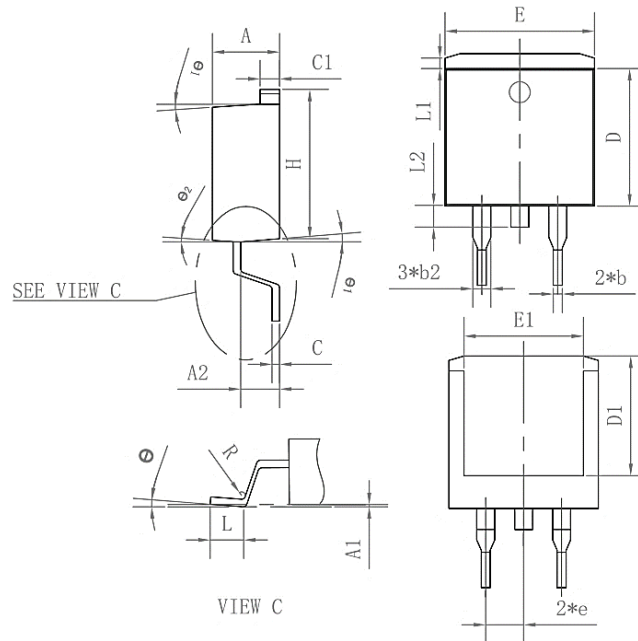
Figure10: Max. transient thermal impedance

### Package Mechanical Data-TO-220-3L-SLK



Symbol	Common		
	mm		
	Mim	Nom	Max
A	4.27	4.57	4.87
A1	1.15	1.30	1.45
A2	2.10	2.40	2.70
b	0.70	0.80	1.00
b2	1.17	1.27	1.50
D	0.40	0.50	0.65
D1	8.80	9.10	9.40
D2	5.70	6.70	7.00
E	9.70	10.00	10.30
E1	-	8.70	-
E2	9.63	10.00	10.35
E3	7.00	8.00	8.40
e		0.37	
e1		0.10	
H1	6.00	6.50	6.85
L	12.75	13.50	13.90
L1	-	3.10	3.40
Phi p	3.45	3.60	3.75
Q	2.60	2.80	3.00
theta 1	4°	7°	10°
theta 2	0°	3°	6°
F	13.30	13.50	13.70
F1	15.50	15.90	16.30
F2	2.80	3.00	3.20

### Package Mechanical Data-TO-263-3L-SLK



Symbol	Common		
	mm		
	Mim	Nom	Max
A	4.35	4.47	4.60
A1	0.09	0.10	0.11
A2	2.30	2.40	2.70
b	0.70	0.80	1.00
b2	1.25	1.36	1.50
C	0.45	0.50	0.65
C1	1.29	1.30	9.40
D	9.10	9.20	9.30
D1	7.90	8.00	8.10
E	9.85	10.00	10.20
E1	7.90	8.00	8.10
H	15.30	15.50	15.70
e	-	2.54	-
L	2.34	2.54	2.74
L1	1.00	1.10	1.20
L2	1.30	1.40	1.50
R	0.24	0.25	0.26
θ	0°	4°	8°
θ1	4°	7°	10°
θ2	0°	3°	6°

**120V N-Channel Enhancement Mode MOSFET****Attention**

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Edition	Date	Change
Rve1.0	2020/11/1	Initial release

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