

## 800V N-Channel Enhancement Mode MOSFET

### Description

The APJ28N80D is **CoolFET II** MOSFET family that is utilizing charge balance technology for extremely low on-resistance and low gate charge performance. APJ14N65F/P/T is suitable for applications which require superior power density and outstanding efficiency

### General Features

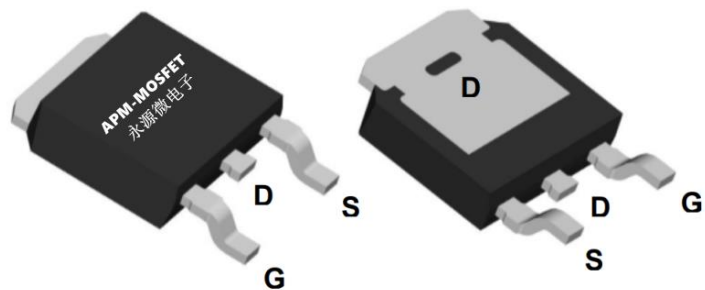
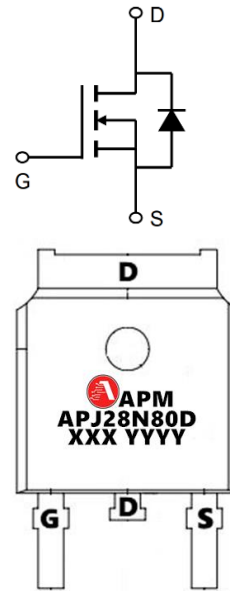
$V_{DS} = 800V$   $IDM = 36A$

$R_{DS(ON)} < 500m\Omega$  @  $V_{GS}=10V$  (**Type: 400mΩ**)

### Application

Uninterruptible Power Supply(UPS)

Power Factor Correction (PFC)



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
APJ28N80D	TO-252-3L	APJ28N80D XXX YYYY	2500

### Absolute Maximum Ratings ( $T_c=25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Value	Unit
$V_{DSS}$	Drain-Source Voltage ( $V_{GS} = 0V$ )	800	V
$I_D$	Continuous Drain Current	9	A
$I_{DM}$	Pulsed Drain Current (note1)	28	A
$V_{GS}$	Gate-Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulse Avalanche Energy (note2)	270	mJ
$P_D$	Power Dissipation ( $T_c = 25^{\circ}C$ )	52	W
$T_J, T_{stg}$	Operating Junction and Storage Temperature Range	$-55 \sim +150$	$^{\circ}C$
$R_{thJC}$	Thermal Resistance, Junction-to-Case	2.4	$^{\circ}C/W$
$R_{thJA}$	Thermal Resistance, Junction-to-Ambient	62.5	$^{\circ}C/W$



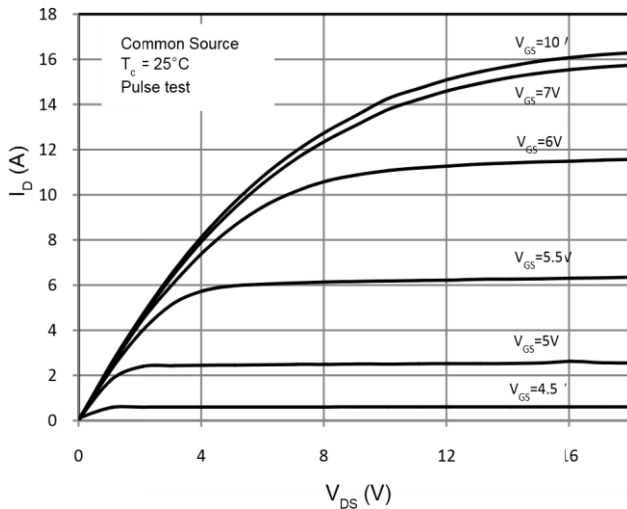
**800V N-Channel Enhancement Mode MOSFET**
**Electrical Characteristics (T<sub>J</sub>=25°C, unless otherwise noted)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain to source breakdown voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	800	880	--	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown voltage temperature coefficient	I <sub>D</sub> =250uA, referenced to 25°C	--	0.7	--	V/°C
IDSS	Drain to source leakage current	V <sub>DS</sub> =800V, V <sub>GS</sub> =0V	--	--	1	uA
		V <sub>DS</sub> =640V, T <sub>C</sub> =125°C	--	--	10	uA
IGSS	Gate to source leakage current, forward	V <sub>GS</sub> =30V, V <sub>DS</sub> =0V	--	--	100	nA
	Gate to source leakage current, reverse	V <sub>GS</sub> =-30V, V <sub>DS</sub> =0V	--	--	-100	nA
VGS(TH)	Gate threshold voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	2.5	3.5	4.5	V
RDS(ON)	Drain to source on state resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =4.5A	--	400	500	mΩ
Gfs	Forward Transconductance	V <sub>DS</sub> =10V, I <sub>D</sub> =4.5A	--	10.4	--	S
Ciss	Input capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =100V, f=1MHz	--	1099	--	pF
Coss	Output capacitance		--	52	--	
Crss	Reverse transfer capacitance		--	1	--	
td(on)	Turn on delay time	V <sub>DS</sub> =400V, I <sub>D</sub> =9A, R <sub>G</sub> =25Ω, V <sub>GS</sub> =10V	--	28	--	ns
tr	Rising time		--	34.4	--	
td(off)	Turn off delay time		--	100	--	
tf	Fall time		--	28	--	
Q <sub>g</sub>	Total gate charge	V <sub>DS</sub> =400V, V <sub>GS</sub> =10V, I <sub>D</sub> =9A	--	24.6	--	nC
Q <sub>gs</sub>	Gate-source charge		--	5.6	--	
Q <sub>gd</sub>	Gate-drain charge		--	9	--	
Rg	Gate Resistance	V <sub>DS</sub> =0V, Scan F mode	--	11	--	Ω
IS	Continuous source current	Integral reverse p-n Junction diode in the MOSFET	--	--	9	A
ISM	Pulsed source current		--	--	27	A
VSD	Diode forward voltage drop.	I <sub>S</sub> =9A, V <sub>GS</sub> =0V	--	0.9	1.3	V
T <sub>rr</sub>	Reverse recovery time	I <sub>S</sub> =9A, V <sub>GS</sub> =0V, dI <sub>F</sub> /dt=100A/us	--	258	--	ns
Qrr	Reverse recovery Charge		--	3.15	--	uC

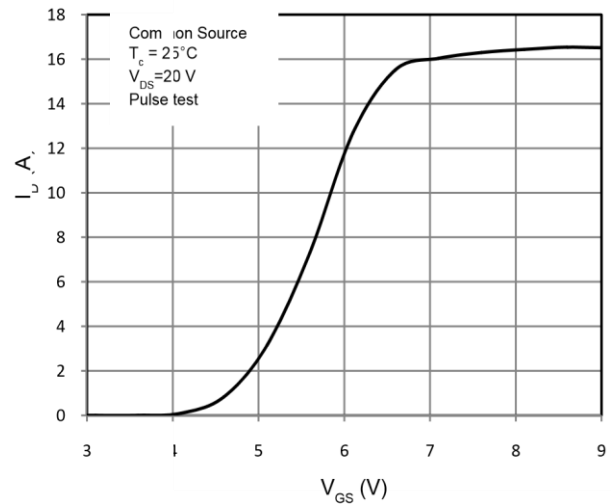
**Note :**

- 1、The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 20Z copper.
- 2、The EAS data shows Max. rating . L=60mH, I<sub>AS</sub>=3A, V<sub>DD</sub>=50V, R<sub>G</sub>=25Ω
- 3、The test condition is Pulse Test: I<sub>SD</sub> ≤ I<sub>D</sub>, di/dt = 100A/us, V<sub>DD</sub> ≤ BVDSS, Starting at T<sub>J</sub> = 25°C
- 4、The power dissipation is limited by 150°C junction temperature
- 5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

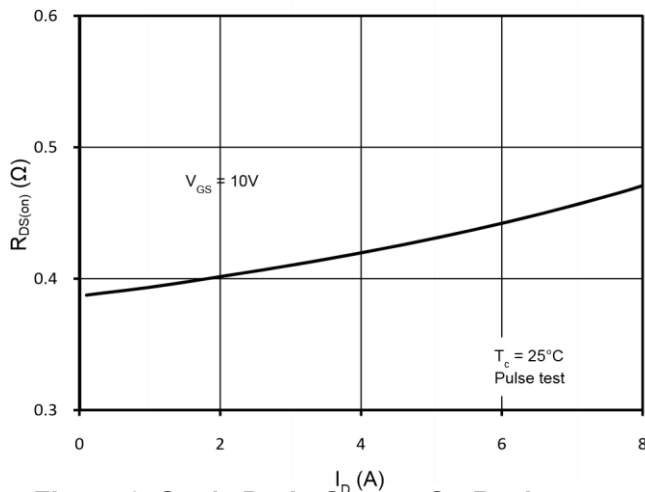
**Typical Characteristics**



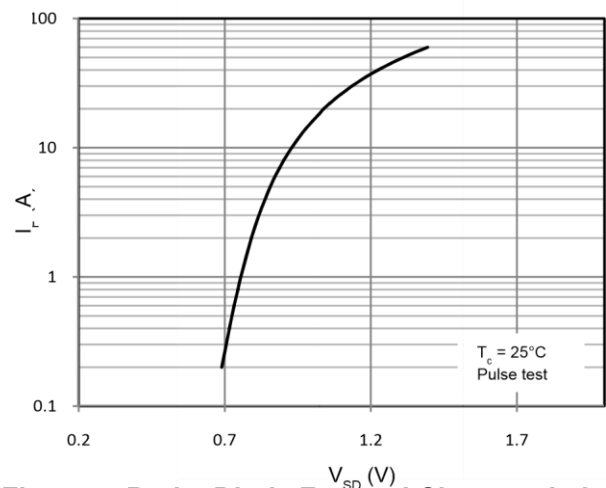
**Figure1: Output characteristics**



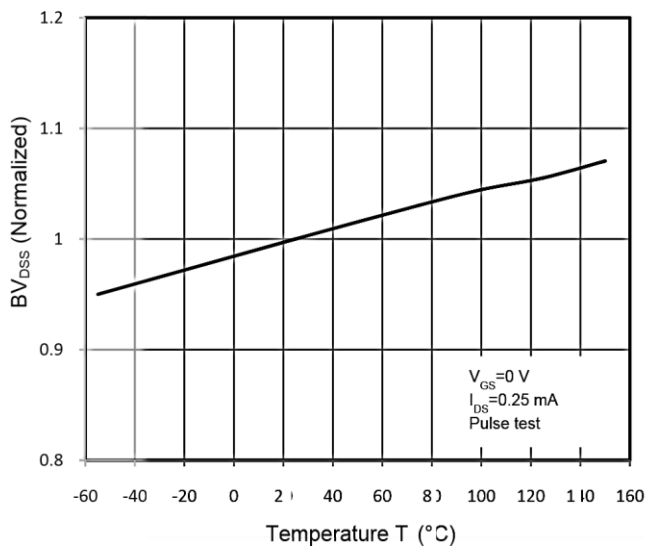
**Figure2: Transfer Characteristics**



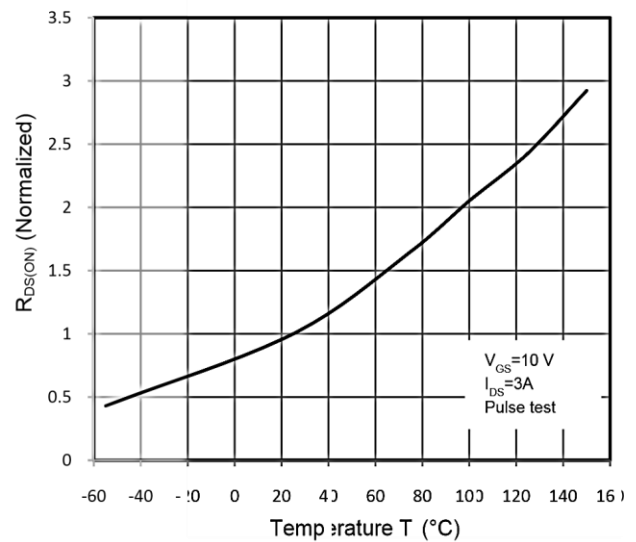
**Figure 3. Static Drain-Source On Resistance**



**Figure 4. Body-Diode Forward Characteristics**



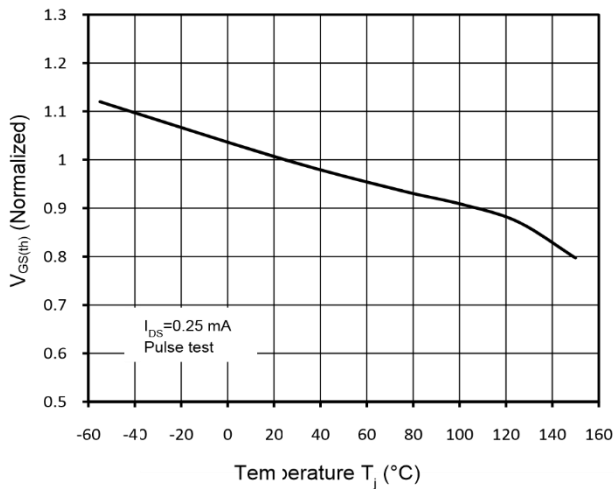
**Figure 5. Normalized  $BV_{DSS}$  vs. Temperature**



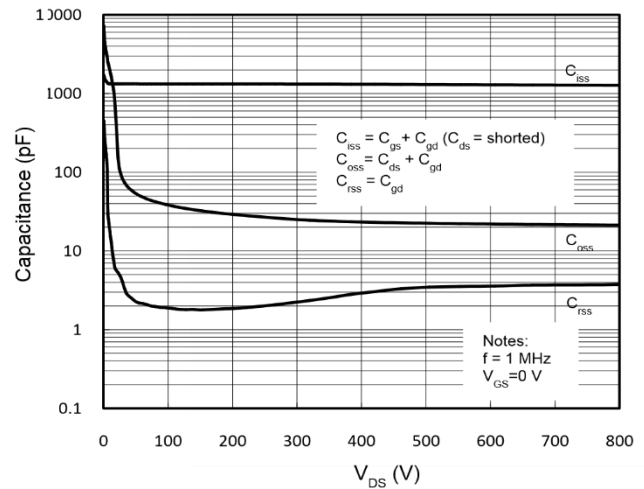
**Figure 6. Normalized  $R_{DS(on)}$  vs. Temperature**



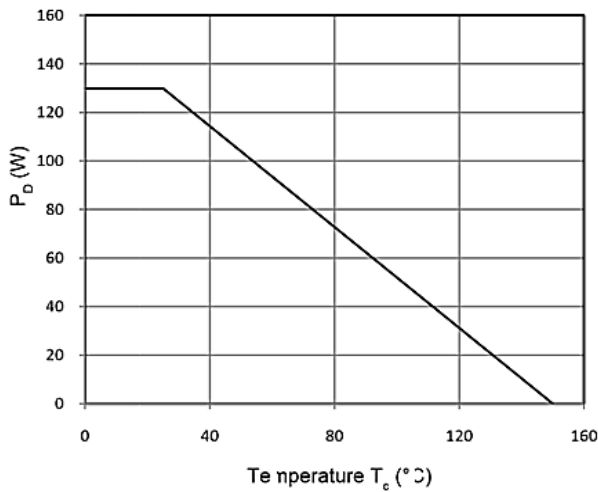
**800V N-Channel Enhancement Mode MOSFET**



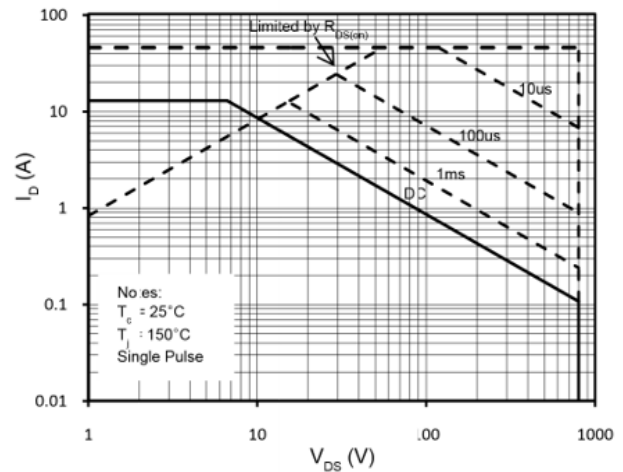
**Figure 7. Threshold Voltage vs. Temperature**



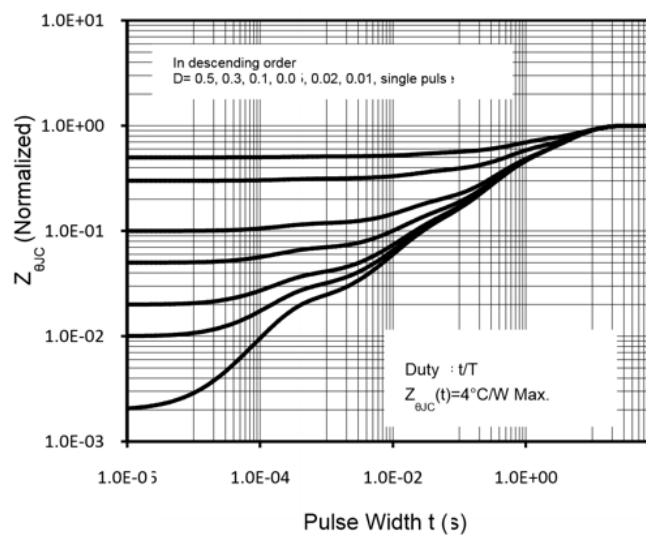
**Figure 8. Capacitance Characteristics**



**Figure9: VGS (th) vs junction temperature**

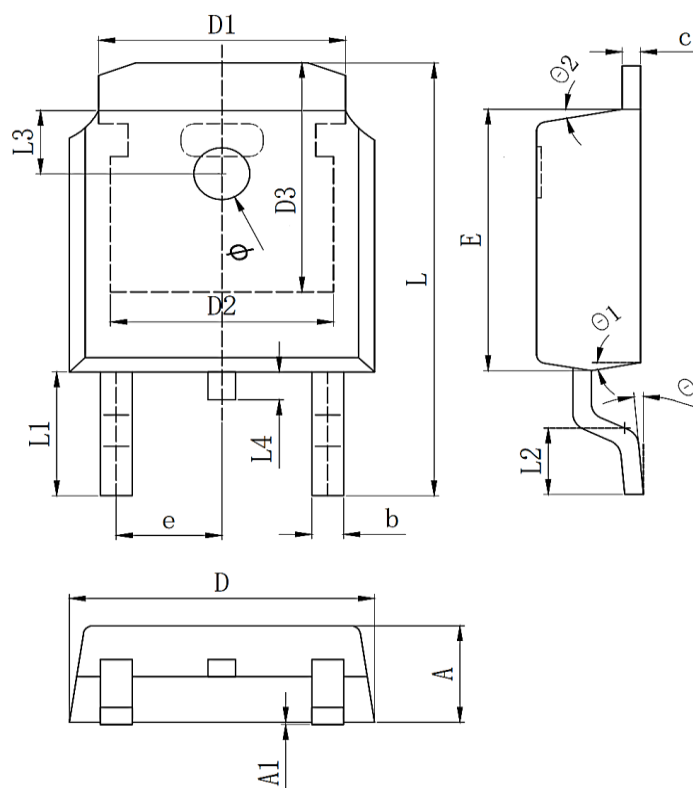


**Figure10: Safe operating area**



**Figure11: Transient thermal impedance**

**Package Mechanical Data:TO-252-3L**



Symbol	Dim in mm		
	Min	Typ	Max
A	2.1	2.3	2.5
A1	0	0.064	0.128
b	0.64	0.75	0.86
c	0.45	0.52	0.6
D	6.4	6.6	6.8
D1	5.33REF		
D2	4.83REF		
D3	5.25REF		
E	5.9	6.1	6.3
e	2.286TYP		
L	9.8	10.1	10.4
L1	2.888REF		
L2	1.4	1.5	1.7
L3	1.65REF		
L4	0.6	0.8	1
φ	1.1	1.2	1.3
θ	0°		10°
θ1	5°		10°
θ2	5°		10°

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Edition	Date	Change
REV1.0	2024/1/1	Initial release

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