

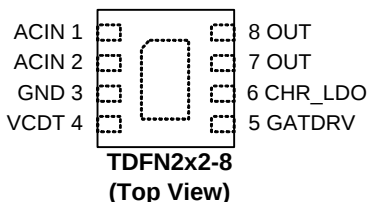
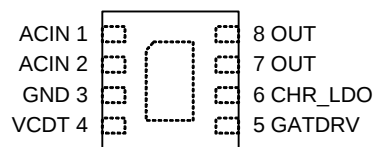
### Features

- Provide OUT Pin 5V Voltage Clamping Protection
- Thermal Charging Regulation Protection
- Provide Input Over-voltage Protection
- Provide Input Over-current Protection
- Provide Over Temperature Protection
- Provide Reverse Current Blocking
- High Immunity of False Triggering
- High Accuracy Protection Threshold
- Low On Resistance 0.3W Typ.
- Compact TDFN2x2-8 and DFN3x3-8 Packages
- Lead Free and Green Devices Available (RoHS Compliant)

### Applications

- Cell Phones

### Pin Configuration



 = Exposed Pad (connected to ground plane for better heat dissipation)

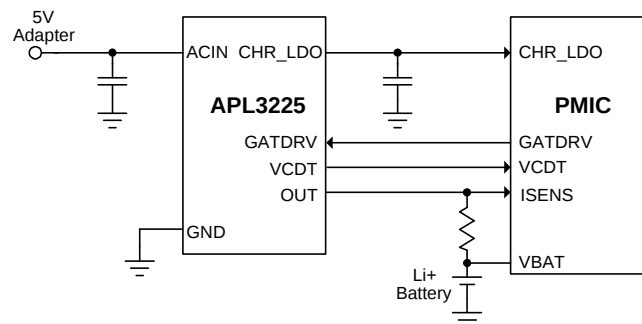
### General Description

The APL3225 provides complete Li+ charger protection against input over-voltage, input over-current and over-temperature. When any of the monitored parameters is over the threshold, the IC turns off the charging current. All protections also have deglitch time against false triggering due to voltage spikes or current transients.

The APL3225 integrates a 5.5V LDO to prevent ACIN overshoot reaching CHR\_LDO and OUT. When any transient peak voltage above 5.5V presenting in ACIN pin, but below OVP threshold, the internal LDO will clamp its output at 5.5V. When ACIN voltage exceeds OVP threshold, the device will turn off charging current. The charging current is controlled by the GATDRV pin. When sourcing a current from the GATDRV pin, the OUT pin delivers the charging current which is 200-fold magnified in amplitude based on GATDRV's current.

Other features include accurate  $V_{VCDT}/V_{ACIN}$  voltage divider, reverse current blocking from OUT to ACIN and OTP protection. The APL3225 provides complete Li+ charger protections, and saves the external MOSFET and Schottky diode for the charger of cell phone's PMIC. The above features and small package make the APL3225 an ideal part for cell phones applications.

### Simplified Application Circuit



ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

## Ordering and Marking Information

|                                                                                                                                                                                         |                                                                                                                                                                                                                                                                                              |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <div> <div>APL3225</div> <div> <div>□□□-□□□</div> <div> <div>Assembly Material</div> <div>Handling Code</div> <div>Temperature Range</div> <div>Package Code</div> </div> </div> </div> | <div> <div>Package Code</div> <div>QB : TDFN2x2-8    QA : DFN3x3-8</div> <div>Operating Ambient Temperature Range</div> <div>I : -40 to 85 °C</div> <div>Handling Code</div> <div>TR : Tape &amp; Reel</div> <div>Assembly Material</div> <div>G : Halogen and Lead Free Device</div> </div> |
| <div> <div>APL3225 QB:</div> <div> <div>L25</div> <div>• X</div> </div> </div>                                                                                                          | <div>X - Date Code</div>                                                                                                                                                                                                                                                                     |
| <div> <div>APL3225 QA:</div> <div> <div>APL</div> <div>3225</div> <div>• XXXXX</div> </div> </div>                                                                                      | <div>X - Date Code</div>                                                                                                                                                                                                                                                                     |

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

## Absolute Maximum Ratings (Note 1)

| Symbol         | Parameter                                       | Rating                | Unit |
|----------------|-------------------------------------------------|-----------------------|------|
| $V_{ACIN}$     | ACIN Input Voltage (ACIN to GND)                | -0.3 ~ 28             | V    |
| $V_{CHR\_LDO}$ | CHR_LDO to GND Voltage                          | -0.3 ~ 7              | V    |
| $V_{GATDRV}$   | GATDRV to GND Voltage                           | -0.3 ~ $V_{CHR\_LDO}$ | V    |
| $V_{CDT}$      | VCDT to GND Voltage                             | -0.3 ~ 7              | V    |
| $V_{OUT}$      | OUT to GND Voltage                              | -0.3 ~ 7              | V    |
| $I_{OUT}$      | Output Current (OUT to GND)                     | 2                     | A    |
| $T_J$          | Maximum Junction Temperature                    | 150                   | °C   |
| $T_{STG}$      | Storage Temperature                             | -65 ~ 150             | °C   |
| $T_{SDR}$      | Maximum Lead Soldering Temperature (10 Seconds) | 260                   | °C   |

Note 1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect vice reliability.

## Thermal Characteristic

| Symbol        | Parameter                                                                    | Typical Value | Unit |
|---------------|------------------------------------------------------------------------------|---------------|------|
| $\theta_{JA}$ | TDFN2x2-8 Junction-to-Ambient Resistance in free air <small>(Note 2)</small> | 75            | °C/W |
| $\theta_{JA}$ | DFN3x3-8 Junction-to-Ambient Resistance in free air <small>(Note 2)</small>  | 65            | °C/W |

Note 2:  $\theta_{JA}$  is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of TDFN2x2-8 is soldered directly on the PCB.

## Recommended Operating Conditions (Note 3)

| Symbol         | Parameter                | Range     | Unit |
|----------------|--------------------------|-----------|------|
| $V_{ACIN}$     | ACIN Input Voltage       | 4.5 ~ 6.5 | V    |
| $I_{OUT}$      | Output Current           | 0 ~ 1     | A    |
| $T_A$          | Ambient Temperature      | -40 ~ 85  | °C   |
| $T_J$          | Junction Temperature     | -40 ~ 125 | °C   |
| $C_{CHR\_LDO}$ | CHR_LDO Output Capacitor | 1         | μF   |

Note 3: Refer to the typical application circuit

## Electrical Characteristics

Unless otherwise specified, these specifications apply over  $V_{ACIN}=5V$ ,  $T_A = -40 \sim 85$  °C. Typical values are at  $T_A=25$ °C.

| Symbol                                      | Parameter                    | Test Conditions                                                                |                                                         | APL3225 |        |        | Unit |
|---------------------------------------------|------------------------------|--------------------------------------------------------------------------------|---------------------------------------------------------|---------|--------|--------|------|
|                                             |                              |                                                                                |                                                         | Min.    | Typ.   | Max.   |      |
| ACIN INPUT CURRENT and POWER-ON-RESET (POR) |                              |                                                                                |                                                         |         |        |        |      |
| I <sub>ACIN</sub>                           | ACIN Supply Current          | I <sub>OUT</sub> =0A, I <sub>CHR_LDO</sub> =0A                                 |                                                         | -       | 350    | 600    | μA   |
|                                             |                              | In OTP                                                                         |                                                         | -       | -      | 550    | μA   |
|                                             |                              | V <sub>ACIN</sub> >V <sub>OVP</sub>                                            |                                                         | -       | -      | 550    | μA   |
| V <sub>POR</sub>                            | ACIN POR Threshold           | V <sub>ACIN</sub> rising                                                       |                                                         | 2.4     | 2.6    | 2.8    | V    |
|                                             | ACIN POR Hysteresis          |                                                                                |                                                         | -       | 250    | -      | mV   |
| T <sub>B(ACIN)</sub>                        | ACIN Power-On Blanking Time  |                                                                                |                                                         | -       | 8      | -      | ms   |
| INTERNAL SWITCH ON RESISTANCE               |                              |                                                                                |                                                         |         |        |        |      |
|                                             | ACIN to OUT On Resistance    | I <sub>OUT</sub> = 1A                                                          |                                                         | -       | 0.3    | 0.35   | Ω    |
|                                             | CHR_LDO Discharge Resistnace | V <sub>ACIN</sub> = 12V , V <sub>CHR_LDO</sub> = 2V                            |                                                         | -       | 500    | -      | Ω    |
| INPUT OVER-VOLTAGE PROTECTION (OVP)         |                              |                                                                                |                                                         |         |        |        |      |
| V <sub>REG</sub>                            | Internal LDO Output Voltage  | V <sub>ACIN</sub> = 6V, I <sub>OUT</sub> = 10mA, T <sub>J</sub> = -40 ~ 125 °C |                                                         | 5.265   | 5.5    | 5.735  | V    |
|                                             | LDO Output Series Resistance |                                                                                |                                                         | 2.4     | 3      | 3.6    | kΩ   |
| V <sub>OVP</sub>                            | Input OVP Threshold          | APL3225                                                                        | V <sub>ACIN</sub> rising, T <sub>J</sub> = -40 ~ 125 °C | 6.6     | 6.8    | 7      | V    |
|                                             | Input OVP Hysteresis         |                                                                                |                                                         | 150     | 200    | 250    | mV   |
| T <sub>OVP</sub>                            | Input OVP Propagation Delay  |                                                                                |                                                         | -       | -      | 1      | μs   |
| T <sub>ON(OVP)</sub>                        | Input OVP recovery time      |                                                                                |                                                         | -       | 1      | -      | ms   |
| OVER-CURRENT PROTECTION (OCP)               |                              |                                                                                |                                                         |         |        |        |      |
| I <sub>OC</sub>                             | Over-Current Trip Threshold  | T <sub>J</sub> = 25 °C, T <sub>J</sub> = -40 ~ 25 °C                           |                                                         | 1.5     | -      | -      | A    |
| I <sub>CL</sub>                             | Current Limit Level          | T <sub>J</sub> = 25 °C, T <sub>J</sub> = -40 ~ 25 °C                           |                                                         | 1.2     | -      | -      | A    |
| VCDT INTERNAL DIVIDER                       |                              |                                                                                |                                                         |         |        |        |      |
|                                             | Divider Ratio                | V <sub>VCDT</sub> /V <sub>ACIN</sub>                                           |                                                         | 0.1035  | 0.1056 | 0.1078 | V/V  |
| CHARGE CURRENT CONTROL                      |                              |                                                                                |                                                         |         |        |        |      |
|                                             | Current Mirror Gain          | I <sub>OUT</sub> = 0.6A, I <sub>OUT</sub> /I <sub>GATDRV</sub>                 |                                                         | 100     | 200    | 300    | A/A  |

## Electrical Characteristics (Cont.)

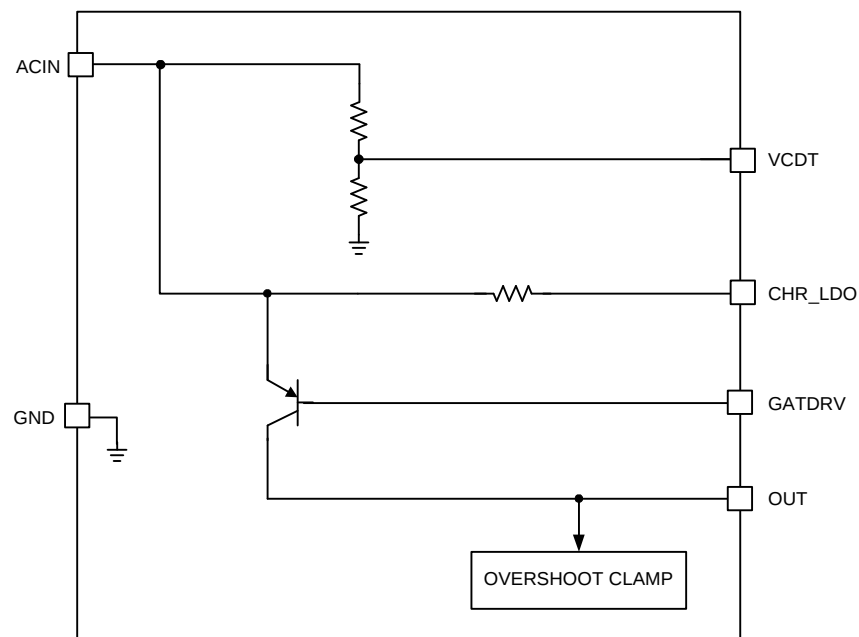
Unless otherwise specified, these specifications apply over  $V_{ACIN}=5V$ ,  $T_A = -40 \sim 85^\circ C$ . Typical values are at  $T_A=25^\circ C$ .

| Symbol                      | Parameter                                    | Test Conditions                                                          | APL3225 |      |      | Unit |
|-----------------------------|----------------------------------------------|--------------------------------------------------------------------------|---------|------|------|------|
|                             |                                              |                                                                          | Min.    | Typ. | Max. |      |
| REVERSE CURRENT BLOCKING    |                                              |                                                                          |         |      |      |      |
|                             | PMOS Lockout Threshold                       |                                                                          | -       | 20   | -    | mV   |
|                             | PMOS Lockout Release Threshold               |                                                                          | -       | 150  | -    | mV   |
|                             | OUT Input Current (Reverse Current Blocking) | V <sub>ACIN</sub> = 0V, V <sub>OUT</sub> = 4.2V, V <sub>GATDRV</sub> =0V | -       | -    | 1    | μA   |
| VOUT OVERSHOOT CLAMP        |                                              |                                                                          |         |      |      |      |
| V <sub>CCAMP</sub>          | Overshoot Clamp Rising Threshold             | V <sub>OUT</sub> rising slew rate > 0.2V/μs                              | 4.6     | 4.8  | 5.0  | V    |
|                             | Overshoot Clamp Pull Low Resistance          | V <sub>OUT</sub> rising slew rate > 0.2V/μs                              | -       | 3    | -    | Ω    |
|                             | Overshoot Clamp Active Time                  | From Overshoot Clamp Threshold being surpassed                           | -       | 150  | -    | μs   |
| Thermal Shutdown Protection |                                              |                                                                          |         |      |      |      |
| T <sub>OTP</sub>            | Thermal Shutdown Threshold                   | T <sub>J</sub> rising                                                    | -       | 160  | -    | °C   |
|                             | Thermal Shutdown Hysteresis                  |                                                                          | -       | 40   | -    | °C   |

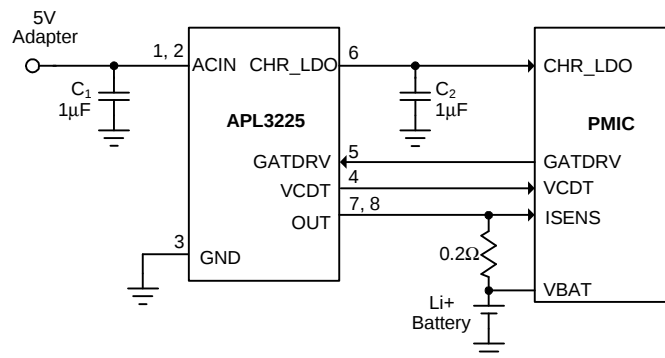
## Pin Description

| PIN         |         | FUNCTION                                                                                                                                                |
|-------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| NO          | NAME    |                                                                                                                                                         |
| 1           | ACIN    | Power Supply Input. Connect this pin to external DC supply. Bypass to GND with a 1 $\mu$ F (minimum) ceramic capacitor.                                 |
| 2           |         |                                                                                                                                                         |
| 3           | GND     | Ground terminal.                                                                                                                                        |
| 4           | VCDT    | Provide an interval voltage divider. This pin divides ACIN voltage into 39/369 ratio.                                                                   |
| 5           | GATDRV  | Charging current control pin. When sourcing a current from this pin, the OUT pin will source out a current whose magnitude is $200 \times I_{GATDRV}$ . |
| 6           | CHR_LDO | Output Pin. The pin provides supply voltage to the PMIC input. Bypass to GND with a 1 $\mu$ F (minimum) ceramic capacitor.                              |
| 7           | OUT     | Output Pins. The pin provides supply source current in series with a resistor to battery.                                                               |
| 8           |         | This pin possesses the overshoot clamp function to limit peak voltage.                                                                                  |
| Exposed Pad | -       | Exposed Thermal Pad. Must be electrically connected to the GND pin.                                                                                     |

## Block Diagram



## Typical Application Circuit



| Designation          | Description                                      |
|----------------------|--------------------------------------------------|
| C <sub>ACIN</sub>    | 1μF, 25V, X5R, 0603<br>Murata GRM188R61E105K     |
|                      | 1μF, 16V, X5R, 0603<br>Murata GRM188R61C105K     |
| C <sub>CHR_LDO</sub> | 1μF, 6.3V, X5R, 0603<br>Murata GRM185R60J225KE26 |

## Function Description

### ACIN Power-On-Reset (POR)

The APL3225 is built-in a power-on-reset circuit to keep the output shut off until internal circuitry is operating properly. The POR circuit has hysteresis and a de-glitch feature so that it will typically ignore undershoot transients on the input. When input voltage exceeds the POR threshold and after 8ms blanking time, the output voltage starts a soft-start to reduce the inrush current.

### ACIN Over-Voltage Protection (OVP) and LDO Mode Operation

The CHR\_LDO output of the IC operates similar to a linear regulator. When the ACIN input voltage is less than  $V_{REG}$ , and above the ACIN POR  $V_{ACIN}$ , the internal LDO output voltage tracks the input voltage with a voltage drop caused by  $R_{DS(on)}$  of MOSFET Q1. When the ACIN input voltage is greater than  $V_{REG}$  plus the  $R_{DS(on)}$  drop of Q1, and less than  $V_{OVP}$ , the internal LDO output voltage is regulated to  $V_{REG}$ , and this is also referred as LDO mode operation. If the input voltage rises above  $V_{OVP}$ , the internal FET Q1 and Q2 will be turned off within 1 $\mu$ s to protect connected system on OUT pin. When the input voltage returns below the input OVP threshold minus the hysteresis, the FETs are turned on again after 1ms recovery time. The input OVP circuit has a 200mV hysteresis and a recovery time of  $T_{ON(OVP)}$  to provide noise immunity against transient conditions.

### Charging Current Control

The charging current is controlled by the GATDRV pin. When sourcing a current from the GATDRV pin, the OUT pin delivers the charging current which is 200-fold magnified in amplitude based on GATDRV's current. The  $I_{OUT}$  current can be calculated by this following equation:

$$I_{OUT} = 200 \times I_{GATDRV}$$

where

The  $I_{OUT}$  is the current flowing out from OUT pin.

The  $I_{GATDRV}$  is the current flowing out from GATDRV pin.

### Current Limit

The output current is monitored by the internal current limit circuit. When the output current reaches the current limit threshold, the device limits the output current at current limit threshold. The current limit level decreases as the junction temperature increases. When the Junction temperature increases, the internal current limit circuit reduces the current limit level, allowing the device's Junction temperature to cool down.

### Internal P-MOSFET and Reverse Current Blocking

The APL3225 integrates a P-channel MOSFET with the body diode reverse protection to replace the external PNP transistor and Schottky diode for cell phone's PMIC. The body diode reverse protection prevents battery voltage supplies to CHR\_LDO and ACIN pin. When the P-channel MOSFET's negative  $V_{SD}$  voltage is detected, the internal bulk selection circuitry will switch the body diode of the P-channel MOSFET forward biased from source to drain, meanwhile the P-channel is turned off regardless of GATDRV's current. This after the detection of negative  $V_{SD}$ , the P-channel MOSFET is in lockout state to prevent battery discharging from ACIN and CHR\_LDO to external circuitry. The P-channel MOSFET lockout will be released when positive  $V_{SD}$  is detected.

### OUT Overshoot Clamp

This OUT pin possesses the overshoot clamp function to limit peak voltage. Since the clamping function needs a low resistance path between OUT pin and external high voltage source (in abnormal condition), please connect this OUT pin directly to outside circuit to let clamping work.

## Application Information

### Capacitor Selection

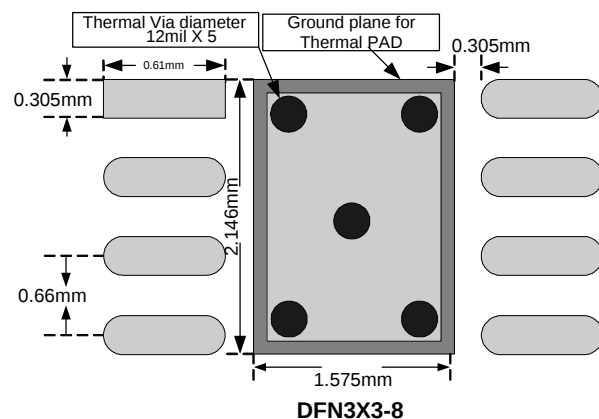
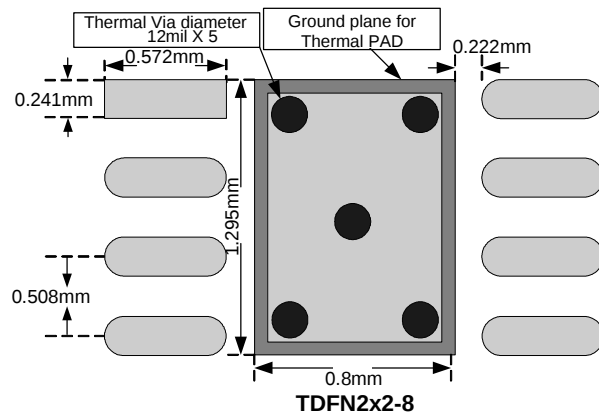
The input capacitor is for decoupling and prevents the input voltage from overshooting to dangerous levels. In the AC adapter hot plug-in applications or load current step-down transient, the input voltage has a transient spike due to the parasitic inductance of the input cable. A 25V, X5R, dielectric ceramic capacitor with a value between  $1\mu\text{F}$  and  $4.7\mu\text{F}$  placed close to the ACIN pin is recommended.

The output capacitor of CHR\_LDO is for CHR\_LDO voltage decoupling. And also can be as the input capacitor of the charging circuit. At least, a  $1\mu\text{F}$ , 10V, X5R capacitor is recommended.

### Layout Consideration

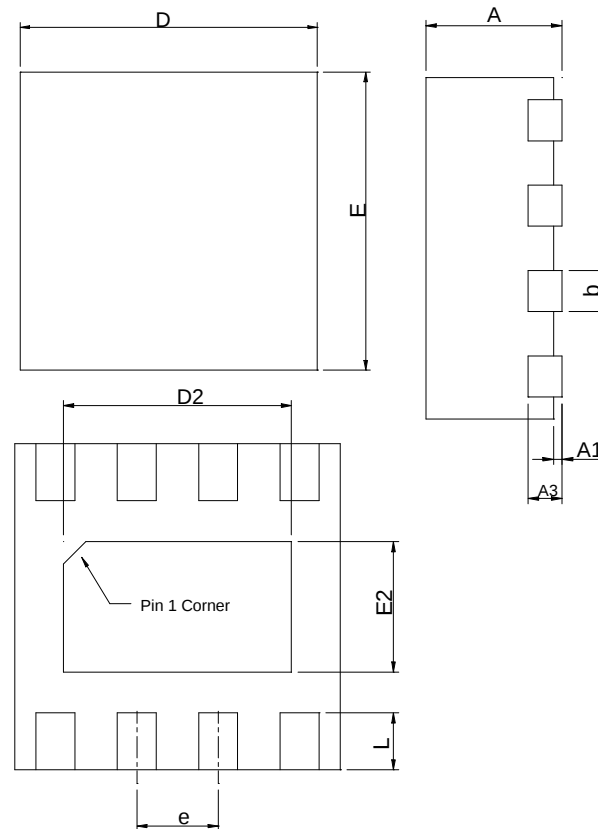
In some failure modes, a high voltage may be applied to the device. Make sure the clearance constraint of the PCB layout must satisfy the design rule for high voltage. The exposed pad of the TDFN2x2-8 and DFN3x3-8 performs the function of channeling heat away. It is recommended that connect the exposed pad to a large copper ground plane on the backside of the circuit board through several thermal vias to improve heat dissipation. The input and output capacitors should be placed close to the IC. The high current traces like input trace and output trace must be wide and short.

### Recommended Minimum Footprint



## Package Information

TDFN2x2-8

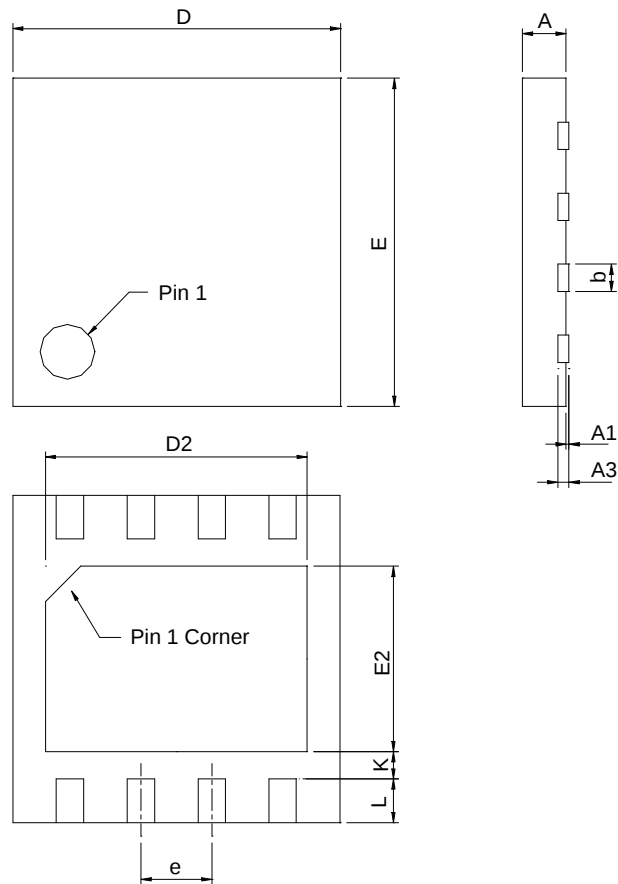


| SYMBOL | TDFN2x2-8   |      |           |       |
|--------|-------------|------|-----------|-------|
|        | MILLIMETERS |      | INCHES    |       |
|        | MIN.        | MAX. | MIN.      | MAX.  |
| A      | 0.70        | 0.80 | 0.028     | 0.031 |
| A1     | 0.00        | 0.05 | 0.000     | 0.002 |
| A3     | 0.20 REF    |      | 0.008 REF |       |
| b      | 0.18        | 0.30 | 0.007     | 0.012 |
| D      | 1.90        | 2.10 | 0.075     | 0.083 |
| D2     | 1.00        | 1.60 | 0.039     | 0.063 |
| E      | 1.90        | 2.10 | 0.075     | 0.083 |
| E2     | 0.60        | 1.00 | 0.024     | 0.039 |
| e      | 0.50 BSC    |      | 0.020 BSC |       |
| L      | 0.30        | 0.45 | 0.012     | 0.018 |

Note : 1. Follow from JEDEC MO-229 WCCD-3.

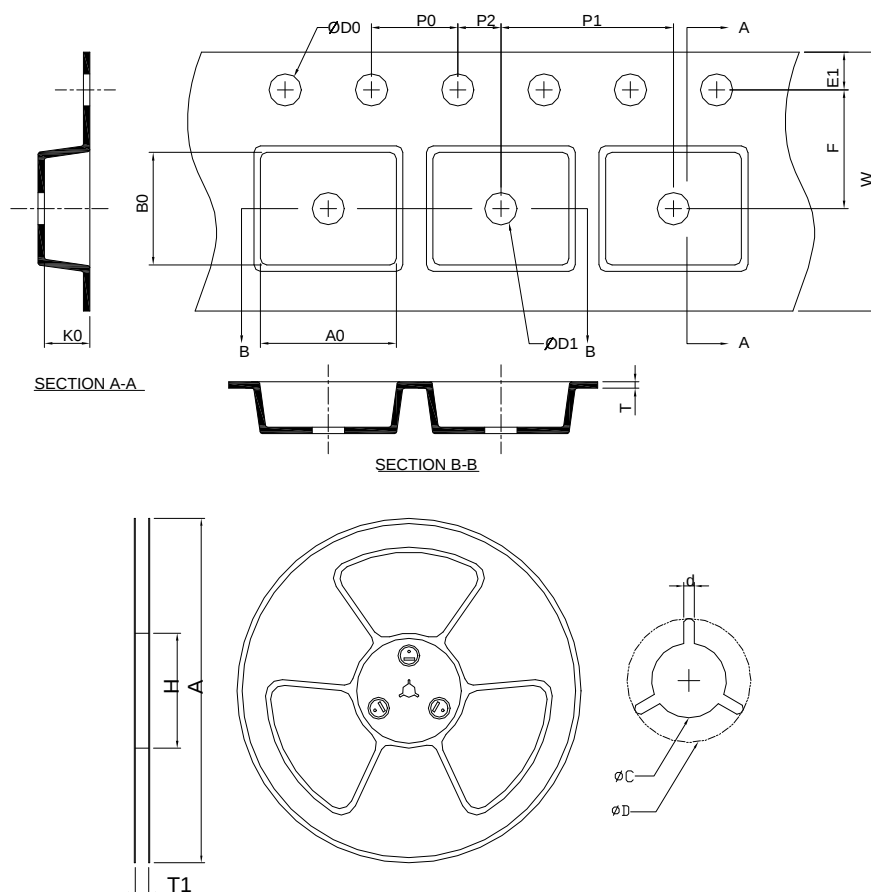
## Package Information

DFN3x3-8



| SYMBOL | DFN3x3-8    |      |           |       |
|--------|-------------|------|-----------|-------|
|        | MILLIMETERS |      | INCHES    |       |
|        | MIN.        | MAX. | MIN.      | MAX.  |
| A      | 0.80        | 1.00 | 0.031     | 0.039 |
| A1     | 0.00        | 0.05 | 0.000     | 0.002 |
| A3     | 0.20 REF    |      | 0.008 REF |       |
| b      | 0.25        | 0.35 | 0.010     | 0.014 |
| D      | 2.90        | 3.10 | 0.114     | 0.122 |
| D2     | 1.90        | 2.40 | 0.075     | 0.094 |
| E      | 2.90        | 3.10 | 0.114     | 0.122 |
| E2     | 1.40        | 1.75 | 0.055     | 0.069 |
| e      | 0.65 BSC    |      | 0.026 BSC |       |
| L      | 0.30        | 0.50 | 0.012     | 0.020 |
| K      | 0.20        |      | 0.008     |       |

## Carrier Tape & Reel Dimensions



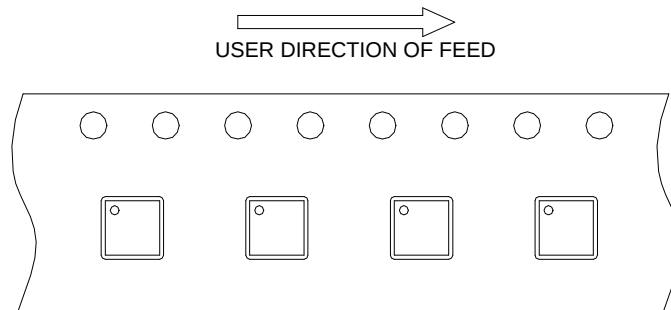
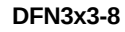
| Application | A           | H         | T1                 | C                  | d        | D                 | W          | E1         | F          |
|-------------|-------------|-----------|--------------------|--------------------|----------|-------------------|------------|------------|------------|
| TDFN2x2-8   | 178.0 ±0.00 | 50 MIN.   | 8.4+2.00<br>-0.00  | 13.0+0.50<br>-0.20 | 1.5 MIN. | 20.2 MIN.         | 8.0 ±0.20  | 1.75 ±0.10 | 3.50 ±0.05 |
|             | P0          | P1        | P2                 | D0                 | D1       | T                 | A0         | B0         | K0         |
|             | 4.0 ±0.10   | 4.0 ±0.10 | 2.0 ±0.05          | 1.5+0.10<br>-0.00  | 1.5 MIN. | 0.6+0.00<br>-0.4  | 2.35 MIN   | 2.35 MIN   | 1.00 ±0.20 |
| Application | A           | H         | T1                 | C                  | d        | D                 | W          | E1         | F          |
| DFN3x3-8    | 178.0 ±0.00 | 50 MIN.   | 12.4+2.00<br>-0.00 | 13.0+0.50<br>-0.20 | 1.5 MIN. | 20.2 MIN.         | 12.0 ±0.30 | 1.75 ±0.10 | 5.5 ±0.05  |
|             | P0          | P1        | P2                 | D0                 | D1       | T                 | A0         | B0         | K0         |
|             | 4.0 ±0.10   | 8.0 ±0.10 | 2.0 ±0.05          | 1.5+0.10<br>-0.00  | 1.5 MIN. | 0.6+0.00<br>-0.40 | 3.30 ±0.20 | 3.30 ±0.20 | 1.30 ±0.20 |

(mm)

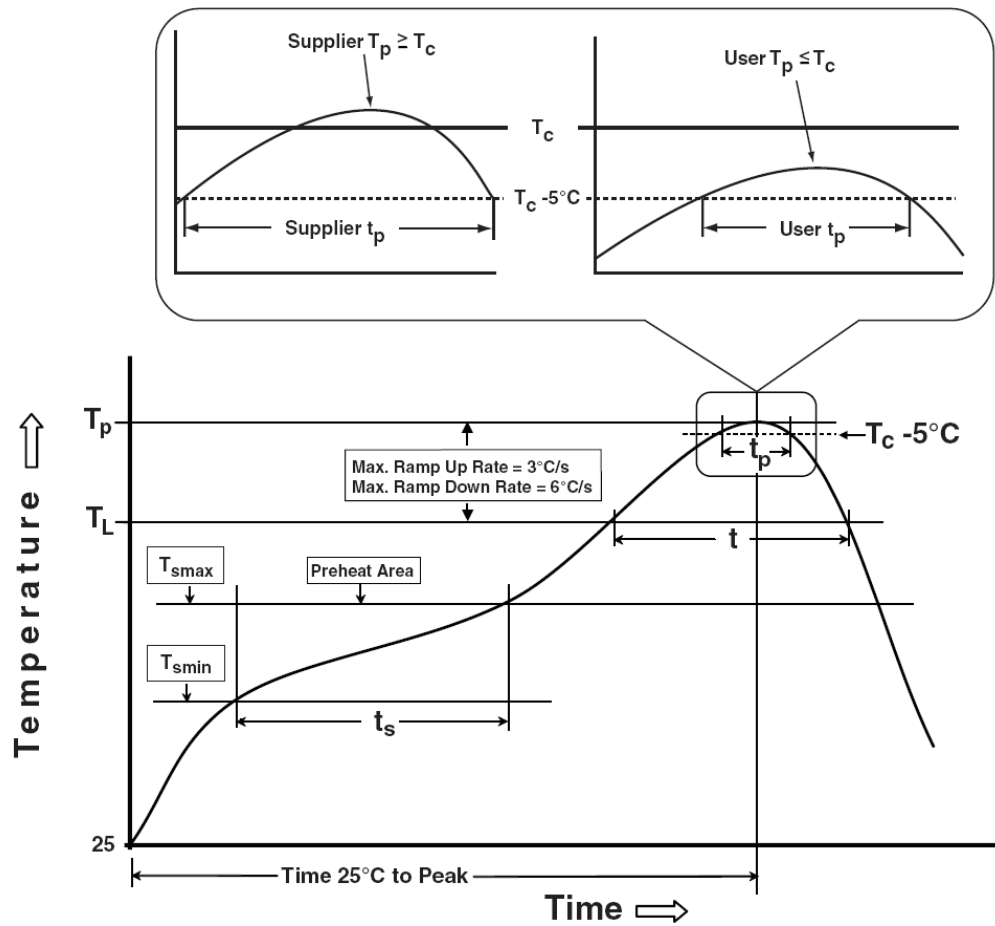
## Devices Per Unit

| Package Type | Unit        | Quantity |
|--------------|-------------|----------|
| TDFN2x2-8    | Tape & Reel | 3000     |
| DFN3x3-8     | Tape & Reel | 3000     |

**TDFN2x2-8**



## Classification Profile



## Classification Reflow Profiles

| Profile Feature                                                                                                                                                                                                             | Sn-Pb Eutectic Assembly            | Pb-Free Assembly                   |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------|------------------------------------|
| <b>Preheat &amp; Soak</b><br>Temperature min ( $T_{smin}$ )<br>Temperature max ( $T_{smax}$ )<br>Time ( $T_{smin}$ to $T_{smax}$ ) ( $t_s$ )                                                                                | 100 °C<br>150 °C<br>60-120 seconds | 150 °C<br>200 °C<br>60-120 seconds |
| Average ramp-up rate ( $T_{smax}$ to $T_p$ )                                                                                                                                                                                | 3 °C/second max.                   | 3°C/second max.                    |
| Liquidous temperature ( $T_L$ )<br>Time at liquidous ( $t_L$ )                                                                                                                                                              | 183 °C<br>60-150 seconds           | 217 °C<br>60-150 seconds           |
| Peak package body Temperature ( $T_p$ )*                                                                                                                                                                                    | See Classification Temp in table 1 | See Classification Temp in table 2 |
| Time ( $t_p$ )** within 5°C of the specified classification temperature ( $T_c$ )                                                                                                                                           | 20** seconds                       | 30** seconds                       |
| Average ramp-down rate ( $T_p$ to $T_{smax}$ )                                                                                                                                                                              | 6 °C/second max.                   | 6 °C/second max.                   |
| Time 25°C to peak temperature                                                                                                                                                                                               | 6 minutes max.                     | 8 minutes max.                     |
| * Tolerance for peak profile Temperature ( $T_p$ ) is defined as a supplier minimum and a user maximum.<br>** Tolerance for time at peak profile temperature ( $t_p$ ) is defined as a supplier minimum and a user maximum. |                                    |                                    |

Table 1. SnPb Eutectic Process – Classification Temperatures ( $T_c$ )

| Package Thickness | Volume mm <sup>3</sup><br><350 | Volume mm <sup>3</sup><br>≥350 |
|-------------------|--------------------------------|--------------------------------|
| <2.5 mm           | 235 °C                         | 220 °C                         |
| ≥2.5 mm           | 220 °C                         | 220 °C                         |

Table 2. Pb-free Process – Classification Temperatures ( $T_c$ )

| Package Thickness | Volume mm <sup>3</sup><br><350 | Volume mm <sup>3</sup><br>350-2000 | Volume mm <sup>3</sup><br>>2000 |
|-------------------|--------------------------------|------------------------------------|---------------------------------|
| <1.6 mm           | 260 °C                         | 260 °C                             | 260 °C                          |
| 1.6 mm – 2.5 mm   | 260 °C                         | 250 °C                             | 245 °C                          |
| ≥2.5 mm           | 250 °C                         | 245 °C                             | 245 °C                          |

## Reliability Test Program

| Test item     | Method             | Description                              |
|---------------|--------------------|------------------------------------------|
| SOLDERABILITY | JESD-22, B102      | 5 Sec, 245°C                             |
| HOLT          | JESD-22, A108      | 1000 Hrs, Bias @ $T_j=125^\circ\text{C}$ |
| PCT           | JESD-22, A102      | 168 Hrs, 100%RH, 2atm, 121°C             |
| TCT           | JESD-22, A104      | 500 Cycles, -65°C~150°C                  |
| HBM           | MIL-STD-883-3015.7 | VHBM 2KV                                 |
| MM            | JESD-22, A115      | VMM 200V                                 |
| Latch-Up      | JESD 78            | 10ms, 1 <sub>tr</sub> 100mA              |

## Customer Service

### **Anpec Electronics Corp.**

#### Head Office :

No.6, Dusing 1st Road, SBIP,  
Hsin-Chu, Taiwan, R.O.C.  
Tel : 886-3-5642000  
Fax : 886-3-5642050

#### Taipei Branch :

2F, No. 11, Lane 218, Sec 2 Jhongsing Rd.,  
Sindian City, Taipei County 23146, Taiwan  
Tel : 886-2-2910-3838  
Fax : 886-2-2917-3838