USB Charging Port Power Switch and Controller

Features

- Meets Battery Charging Specification BC1.2 for DCP and CDP
- Meets Chinese Telecommunications Industry Standard YD/T 1591-2009
- Support Non-BC1.2 Charging Mode by Automatic Detection:
  - Divider 1, 2 Supports Most Available Apple Device
  - 1.2V Mode Pull High Supports Samsung device
  - Automatic SDP/CDP Swapping for BC1.2 non-compatible Devices That do not Recognize CDP Ports
- Supports Sleep Mode Charging and LS & HS HID (Mouse/Keyboard) Wake Up
- Load Detection for both Power Supply Control in S4/S5 Charging and Port Power Management in all Charge Modes
- 62mΩ Power Switch Meets USB2.0 & USB3.0 Power Switch Requirement
- VIN Operating Range: 4.5 ~ 5.5V
- Low Quiescent Current:
  - <240μA When Device Enabled
  - <2μA When Device Disabled
- High Bandwidth Data Switch Supports USB 2.0
- Adjustable Current Limit Up to 3.0A (typical)
- Output Discharge
- UL Approved-File No.E328191
- UL-CB Scheme IEC/EN62368-1 Certified
- TUV IEC/EN62368-1 Certified
- Lead Free and Green Devices (RoHS Compliant)

General Description

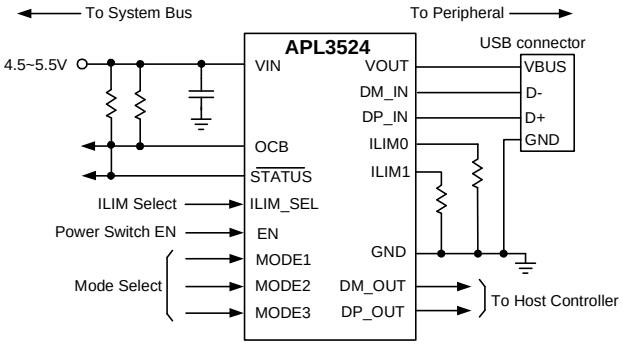
The APL3524 is an USB charging port controller which integrates USB 2.0 high-speed data line (D+/D-) switches and a power switch. The charging schemes comply with battery charging BC1.2 and Chinese Telecommunications Industry Standard YD/T 1591-2009.

The APL3524 also implements some dedicated charging schemes to support non-BC1.2 compatible device, such as divider1, divider2 mode or 1.2V shorted mode. The APL3524 features power wake and port power management (PPM) via STATUS pin in supporting power management. Power wake allows for power supply control in S4/S5 charging and PPM the ability to manage port power in a multi-port application. Furthermore, the APL3524 supports mouse/keyboard wake up from S3. The 62mΩ power switch with current limit and short circuit protections supports load current up to 2.5A. Two current limit thresholds set by two programming pin provide flexibility in current limit and load detection settings.

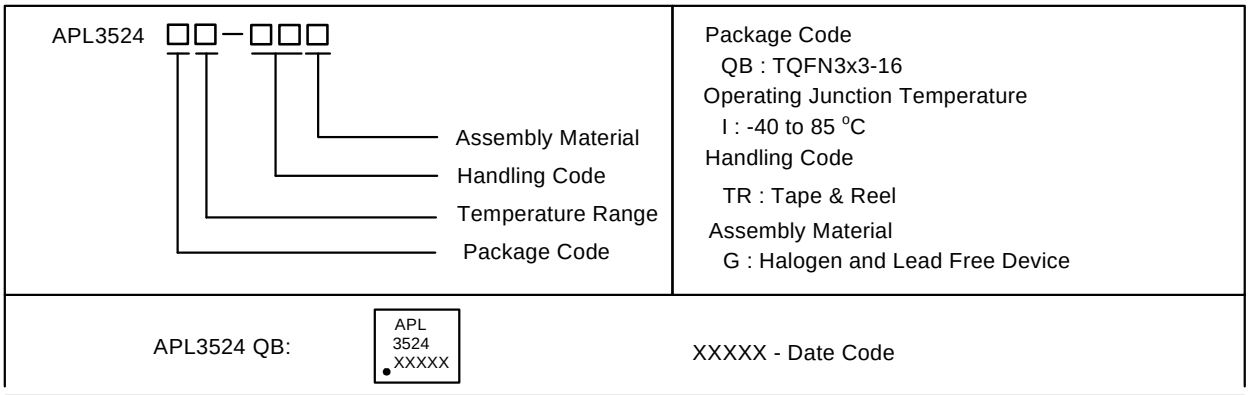
Applications

- NB
- AIO PC
- USB Ports
- Universal Wall Charging Adapters

Simplified Application Circuit

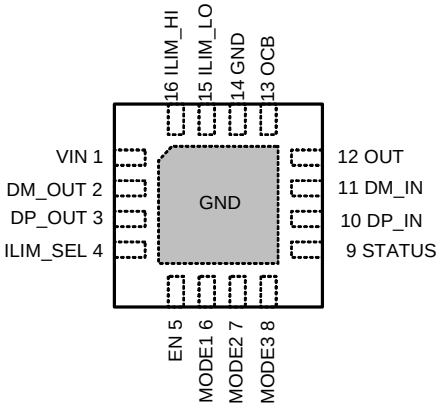


Ordering and Marking Information



Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Pin Configuration



TQFN3x3-16
(Top View)

=Exposed Pad. Connect this pad to large copper area for better heat dissipation.

Absolute Maximum Ratings (Note 1)

Symbol	Parameter		Rating	Unit
V_{VIN}	VIN Input Voltage (VIN to GND)		-0.3~7	V
V_{EN}, V_{ILIM_LO}, V_{ILIM_HI}, V_{ILIM_SEL}, V_{MODE1}, V_{MODE2}, V_{MODE3}	EN, ILIM_LO, ILIM_HI, ILIM_SEL, MODE1, MODE2, MODE3 to GND Voltage		-0.3~7	V
V_{VOUT}, V_{OCB}	VOUT, OCB, $\overline{STATUS}$ to GND Voltage		-0.3~7	V
$V_{VIN-VOUT}$	VIN to VOUT Voltage		-7~7	V
V_{DP_IN}, V_{DM_IN}, V_{DP_OUT}, V_{DM_OUT}	DP_IN, DM_IN, DP_OUT, DM_OUT to GND Voltage		-0.3~5.7	V
I_{DP_IN}, I_{DM_IN}, I_{DP_OUT}, I_{DM_OUT}	DP_IN, DM_IN, DP_OUT, DM_OUT Input Clamp Current		-20~20	mA
$I_{DP\_IN-DP\_OUT}$, $I_{DM\_IN-DM\_OUT}$	DP_IN to DP_OUT, DM_IN to DM_OUT Continuous Current In SDP or CDP Mode		-100~100	mA
$I_{DP\_IN-DM\_IN}$	DP_IN to DM_IN Current In BC1.2 DCP Mode		-35~35	mA
I_{OUT}	Continuous Output Current		Internally Limited	
I_{OCB}	OCB Continuous Sink Current		25	mA
I_{ILIM_LO}, I_{ILIM_HI}	ILIM_LO, ILIM_HI Continuous Source Current		1	mA
P_D	Continuous Total Power Dissipation		Internally Limited	
HMB	ESD Rating, Human Body Model	VIN, EN, ILIM_LO, ILIM_HI, ILIM_SEL, MODE1, MODE2, MODE3, OUT, OCB, N/C	2	kV
		DP_IN, DM_IN, DP_OUT, DM_OUT	8	
CDM	ESD Rating, Charged Device Model		500	V
T_J	Junction Temperature		Internally Limited	°C
T_{STG}	Storage Temperature		-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature(10 Seconds)		260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air.	55	°C/W
θ_{JC}	Junction-to-Caset Resistance in free air.	10	°C/W

Note 2: 2 layered 5 in2 printed circuit boards with 2oz trace and copper through several thermal vias. The thermal pad is soldered on the PCB.

Note 3: The case temperature is measured at the center of the exposed pad on the underside of the TQFN3x3-16 packages.

Recommended Operating Conditions (Note 4)

Symbol	Parameter	Range	Unit
V_{VIN}	VIN Input Voltage (VIN to GND)	4.5 ~ 5.5	V
V_{EN}, V_{ILIM_SEL}, V_{MODE1}, V_{MODE2}, V_{MODE3}	EN, ILIM_SEL, MODE1, MODE2, MODE3 to GND Input Voltage	0 ~ 5.5	V
V_{DP_IN}, V_{DM_IN}, V_{DP_OUT}, V_{DM_OUT}	DP_IN, DM_IN, DP_OUT, DM_OUT to GND Input Voltage	0 ~ 5.5	V
$I_{DP\_IN-DP\_OUT}$, $I_{DM\_IN-DM\_OUT}$	DP_IN to DP_OUT, DM_IN to DM_OUT Continuous Current In SDP or CDP Mode	-30 ~ 30	mA
$I_{DP\_IN-DM\_IN}$	DP_IN to DM_IN Current In BC1.2 DCP Mode	-10 ~ 10	mA
I_{OUT}	Continuous Output Current	0 ~ 2.5	A
R_{ILIM_LO}, R_{ILIM_HI}	ILIM_HI, ILIM_LO Set Resistors (ILIM_LO, ILIM_HI to GND)	16.9 ~ 750	kΩ
T_J	Operating Virtual Junction Temperature	-40 ~ 125	°C

Note 4: Refer to the typical application circuit.

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=V_{EN}=5V, R_{OCB}=10kΩ, R_{IILIM_LO}=210kΩ, R_{IILIM_HI}=20kΩ, MODE1=MODE2=low, MODE3=high, and T_A= -40 to 85°C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APL3524			Unit
			Min	Typ	Max	
SUPPLY CURRENT						
I_{VIN}	VIN Supply Current	V_{EN}=5V, T_A=25 °C	-	180	240	μA
I_{VIN_SD}	VIN Shutdown Supply Current	V_{EN}=0V, T_A=25 °C	-	0.1	2.0	μA
UNDER-VOLTAGE LOCKOUT						
V_{UVLO}	VIN UVLO Threshold Voltage	V_{IN} rising	3.9	4.1	4.3	V
V_{UVLO_HYS}	VIN UVLO Threshold Voltage Hysteresis	V_{IN} falling	-	100	-	mV
POWER SWITCH						
$R_{DS(on)}$	Static Drain-Source On-state Resistance	I_{OUT}=2A, ILIM_SEL=high, T_A= -40 to 85 °C	-	62	78	mΩ
		I_{OUT}=2A, ILIM_SEL=low, T_A= 25 °C	-	62	72	mΩ
	VOUT Rise Time	C_{OUT}=1μF, R_{OUT}=100Ω (V_{OUT} 10-90%)	0.7	1	1.6	ms
	VOUT Fall Time	C_{OUT}=1μF, R_{OUT}=100Ω (V_{OUT} 90-10%)	0.2	-	0.5	ms
	Leakage Current	V_{IN}=5.5V, V_{EN}=0V, T_J=25°C, VOUT tied to GND	-	-	1	μA
	Reverse Leakage Current	V_{OUT}=5.5V, V_{EN}=0V, T_J=25°C, VIN tied to GND	-	-	1	μA

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=V_{EN}=5V, R_{OCB}=10kΩ, R_{IILIM_LO}=210kΩ, R_{IILIM_HI}=20kΩ, MODE1=MODE2=MODE3=high, and T_A= -40 to 85°C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions		APL3524			Unit
				Min	Typ	Max	
CURRENT LIMIT							
	ILIM_SEL Logic Input Threshold	V_{ILIM_SEL} rising		1.1	1.3	1.85	V
	ILIM_SEL Logic Threshold Hysteresis	V_{ILIM_SEL} falling		-	200	-	mV
	ILIM_SEL Input Current	V_{ILIM_SEL}=0V or 5.5V		-0.5	-	0.5	µA
I_{LIM}	Current Limit Threshold	ILIM_SEL=low, VOUT short to ground.	R_{ILIM_LO}=210kΩ	205	240	275	mA
			R_{ILIM_LO}=80.6kΩ	575	625	680	
			R_{ILIM_LO}=22.1kΩ	2120	2275	2430	
		ILIM_SEL=high, VOUT short to ground.	R_{ILIM_HI}=20kΩ	2340	2510	2685	
			R_{ILIM_HI}=16.9kΩ	2770	2970	3170	
	Response Time to Short Circuit	I_{OUT} slew rate=20A/µs	R_{ILIM_XX}=20kΩ	-	-	1	µs
ENABLE, OUTPUT DISCHARGE							
V_{EN_TH}	EN Logic Input Threshold			1.1	1.3	1.85	V
	EN Logic Input Threshold Hysteresis			-	200	-	mV
	EN Input Current	V_{EN}=0 or 5.5V		-0.5	-	0.5	µA
	Turn-on Time	C_{OUT}=1µF, R_{OUT}=100Ω, V_{EN} rising edge to 90% V_{OUT}		-	-	11	ms
	Turn-off Time	C_{OUT}=1µF, R_{OUT}=100Ω, V_{EN} fallng edge to 10% V_{OUT}		-	1.7	3	ms
	VOUT Discharge Resistance	V_{OUT}=4V, V_{EN}=0V		400	500	630	Ω
t_{DCHG}	VOUT Discharge Hold Time	Time start to count when V_{OUT} falls below 0.8V during DCH mode		1.3	2	2.9	s
OCB							
	OCB Output Low Voltage	I_{OCB}=1mA		-	-	100	mV
	Off-state Leakage			-	-	1	µA
$t_{D(OCB)}$	OCB Deglitch Time			5	8.2	12	ms
MODE1, MODE2, MODE3 Inputs							
V_{MODE_TH}	MODEx Logic Input Threshold	V_{MODEx} rising		1.1	1.3	1.85	V
	MODEx Logic Input Threshold Hysteresis	V_{MODEx} falling		-	200	-	mV
	MODEx Input Current	V_{MODEx}=0 or 5.5V		-0.5	-	0.5	µA

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=V_{EN}=5V, R_{OCB}=10kΩ, R_{IILIM_LO}=210kΩ, R_{IILIM_HI}=20kΩ, MODE1=MODE2=low, MODE3=high, and T_A= -40 to 85°C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APL3524			Unit
			Min	Typ	Max	
THERMAL SHUTDOWN						
	Thermal Shutdown Threshold		130	140	150	°C
	Thermal Shutdown Threshold Hysteresis		-	20	-	°C
HIGH BANDWIDTH ANALOG SWITCH						
R_{HS_ON}	DP, DM High Speed Switch On Resistance	V_{DP/DM_OUT}=0V, I_{DP/DM_OUT}=+30mA	-	2	4	Ω
		V_{DP/DM_OUT}=2.4V, I_{DP/DM_OUT}=-15mA	-	3	6	Ω
	On Resistance Match Between Channels DP/DM Switch	V_{DP/DM_OUT}=0V, I_{DP/DM_OUT}=+30mA	-	0.05	0.15	Ω
		V_{DP/DM_OUT}=0V, I_{DP/DM_OUT}=+30mA	-	0.05	0.15	Ω
	DM/DP Off State Capacitance	V_{EN}=0V, V_{DP/DM_IN}=0.3V, V_{AC}=0.6V_{PK-PK}, f=1MHz	-	3	-	pF
	DM/DP On State Capacitance	V_{DP/DM_IN}=0.3V, V_{AC}=0.6V_{PK-PK}, f=1MHz,	-	5.4	-	pF
	Off State Isolation	V_{EN}=0V, R_L=50Ω, f=250MHz, T_A= -40 to 125 °C	-	33	-	dB
	On State Cross Channel Isolation	R_L=50Ω, f=250MHz, T_A= -40 to 125 °C	-	52	-	dB
	Off State Leakage	V_{EN}=0V, V_{DM_IN}=V_{DP_IN}=3.6V, V_{DM_OUT}=V_{DP_OUT}=0V, measure I_{DM_OUT} and I_{DP_OUT}	-	0.1	1.5	μA
	Bandwidth (-3dB)	R_L=50Ω	-	2.6	-	GHz
	Propagation Delay		-	0.25	-	ns
	Skew Between Opposite Transitions Of The Same Port (t_{PHL}-t_{PLH})		-	0.1	-	
DCP SHORTED MODE CHARGER INTERFACE						
R_{DPM_SHORT}	DP_IN/DM_IN Shorting Resistance	MODEx configured for DCP BC1.2	-	125	200	Ω
DIVIDER MODE CHARGER INTERFACE						
V_{DP_AM}	DP_IN Output Voltage in Divider 1	MODEx configured for divider mode	1.9	2	2.1	V
	DP_IN Output Voltage in Divider 2		2.57	2.7	2.84	V
V_{DM_AM}	DM_IN Output Voltage Divider 1		2.57	2.7	2.84	V
	DM_IN Output Voltage Divider 2		1.9	2	2.1	V
Z_{OUT_DP}	DP_IN Output Impedance		8	10.5	12.5	kΩ
Z_{OUT_DM}	DM_IN Output Impedance		8	10.5	12.5	kΩ
1.2V Mode						
	DP_IN/DM_IN Output Voltage		1.19	1.25	1.31	V
	DP_IN/DM_IN Output Impedance		60	75	94	kΩ

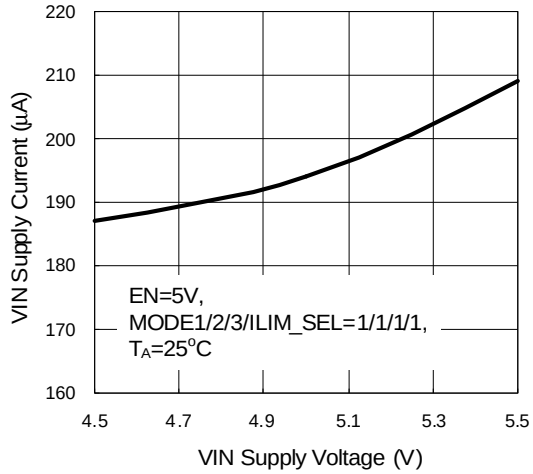
Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=V_{EN}=5V, R_{OCB}=10kΩ, R_{IILIM_LO}=210kΩ, R_{IILIM_HI}=20kΩ, MODE1=MODE2=low, MODE3=high, and T_A= -40 to 85°C. Typical values are at T_A=25°C.

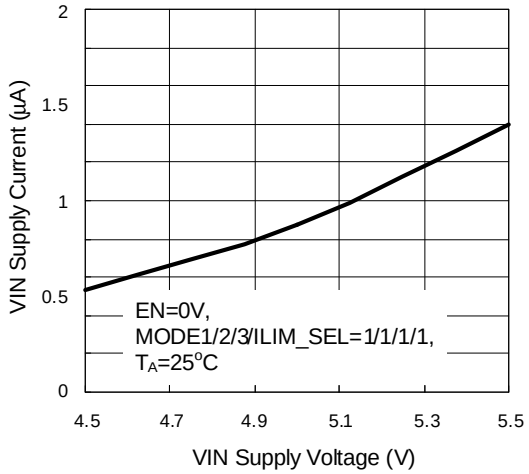
Symbol	Parameter	Test Conditions	APL3524			Unit
			Min	Typ	Max	
CDP Interface						
V_{DM_SRC}	Voltage Source On DM_IN for CDP Detect	V_{DP_IN}=0.6V, MODEx configured for CDP	0.5	0.6	0.7	V
V_{DAT_REF}	DP_IN Rising Voltage Threshold To Activate V_{DM_SRC}	V_{DP_IN}=0.6V, MODEx configured for CDP	0.25	-	0.4	V
	V_{DAT_REF} Hysteresis			50		mV
V_{LGC_SRC}	DP_IN Rising Voltage Threshold To Deactivate V_{DM_SRC}		0.8	-	1	V
	V_{LGC_SRC} Hysteresis		-	100	-	mV
I_{DP_SINK}	DP_IN Sink Current	V_{DP_IN}=0.4~0.8V,	40	70	100	uA
LOAD DETECTION- PORT POWER MANAGEMENT						
	I_{OUT} Rising Load Detection Current Threshold		-	I_{ILIM_LO}+60	-	mA
	I_{OUT} rising load detection current threshold Hyeteresis		-	50	-	mA
	Load Detection Set Time		140	200	275	ms
	Load Detection Reset Time		1.9	3	4.2	s
LOAD DETECTION- POWER WAKE						
	Power Wale Short Circuit Current Limit		-	55	-	mA
	I_{OUT} Falling Power Wake Reset Current Detection Threshold		23	45	67	mA
	Power Wake Reset Time		10.7	15	20.6	s

Typical Operating Characteristics

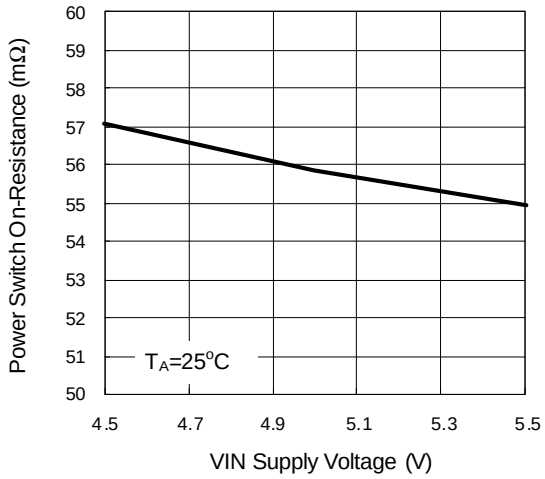
VIN Supply Current vs. Supply Voltage



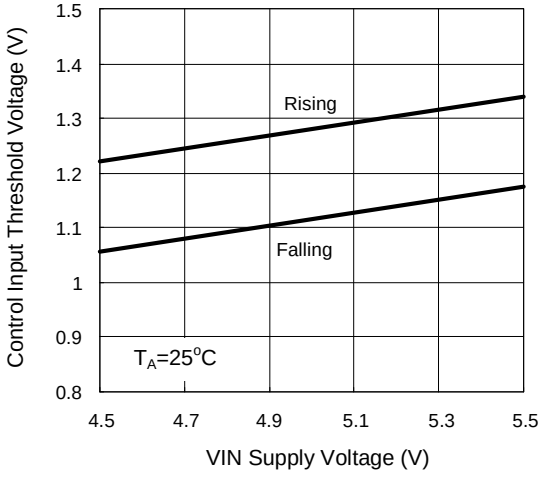
VIN Supply Current vs. Supply Voltage



Power Switch On-Resistance vs. VIN Supply Voltage



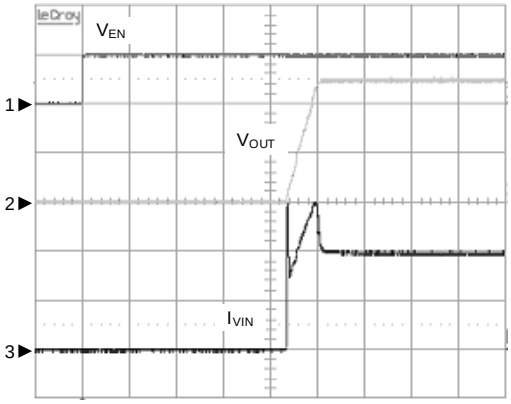
Control Logic Input Threshold Voltage vs. VIN Supply Voltage



Operating Waveforms

The test condition is V_{IN}=5V, T_A= 25°C unless otherwise specified.

Turn On Response



V_{IN}=5V, R_{LOAD}=5Ω, C_{IN}=4.7uF/MLCC, C_{OUT} =150µF/Electrolytic,

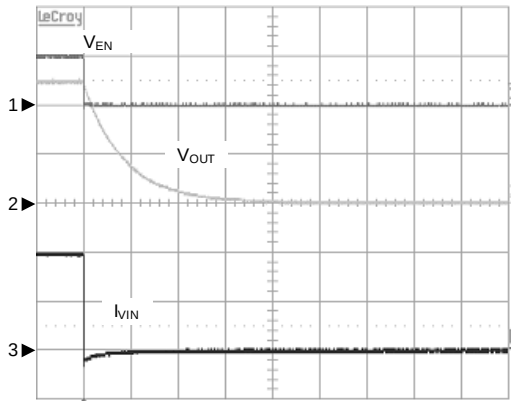
CH1: V_{EN}, 5V/Div, DC

CH2: V_{OUT}, 2V/Div, DC

CH3: I_{VIN}, 500mA/Div, DC

TIME: 2ms/Div

Turn Off Response



V_{IN}=5V, R_{LOAD}=5Ω, C_{IN}=4.7uF/MLCC, C_{OUT} =150µF/Electrolytic,

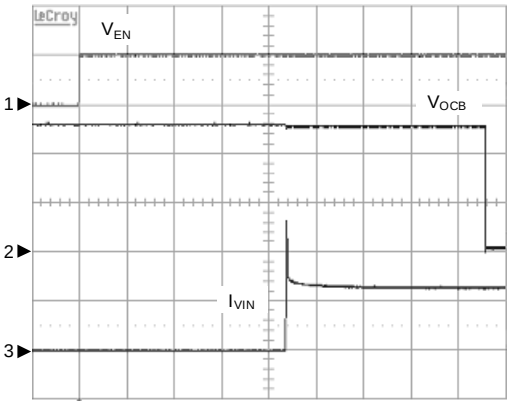
CH1: V_{EN}, 5V/Div, DC

CH2: V_{OUT}, 2V/Div, DC

CH3: I_{VIN}, 500mA/Div, DC

TIME: 1ms/Div

Device Enabled into Short Circuit



V_{IN}=5V, OUT short to ground, MODE1=1, MODE2=1, MODE3=1, ILIM_SEL=0, R_{ILIM_LO}=80.6kΩ

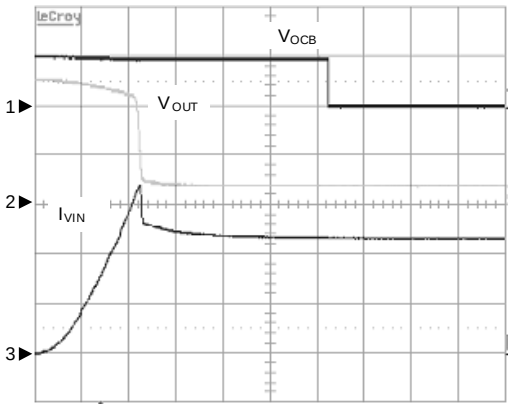
CH1: V_{EN}, 5V/Div, DC

CH2: V_{OCB}, 2V/Div, DC

CH3: I_{VIN}, 0.5A/Div, DC

TIME:2ms/Div

OCB Response with Ramped Load



V_{IN}=5V, MODE1=1, MODE2=1, MODE3=1, ILIM_SEL=1, R_{ILIM_LO}=20kΩ

CH1: V_{OCB}, 5V/Div, DC

CH2: V_{OUT}, 2V/Div, DC

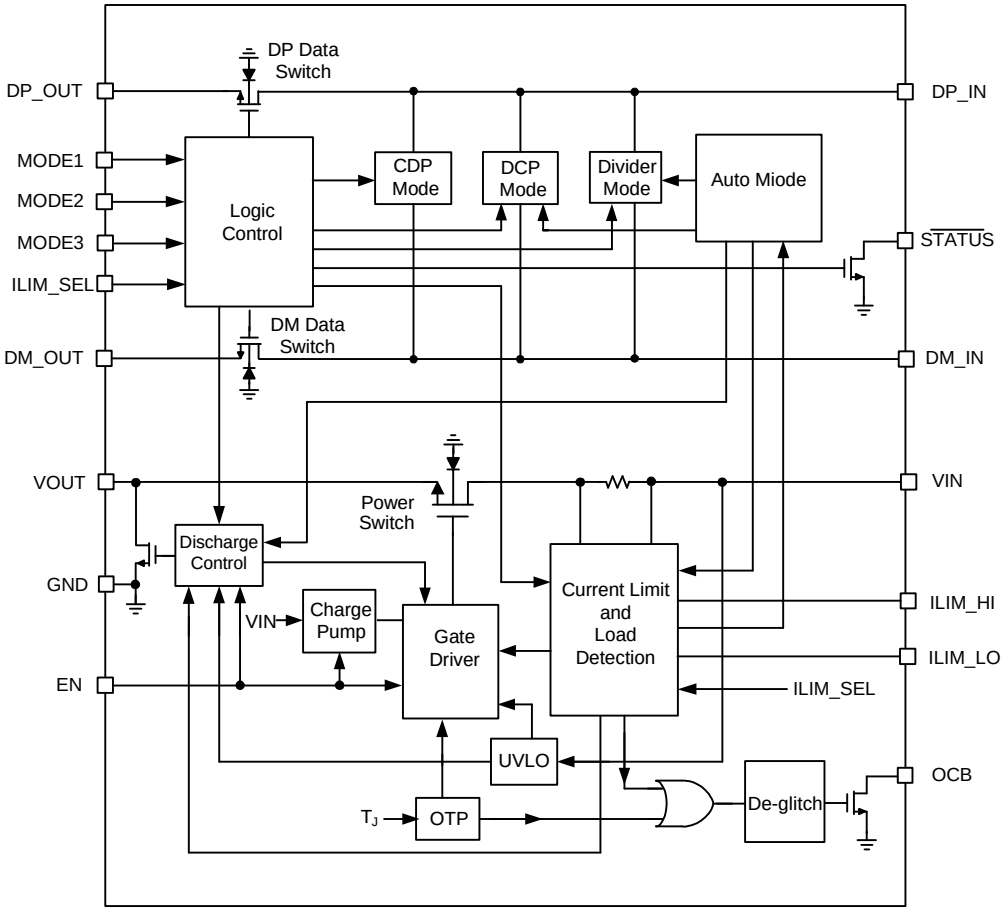
CH3: I_{VIN}, 1A/Div, DC

TIME:2ms/Div

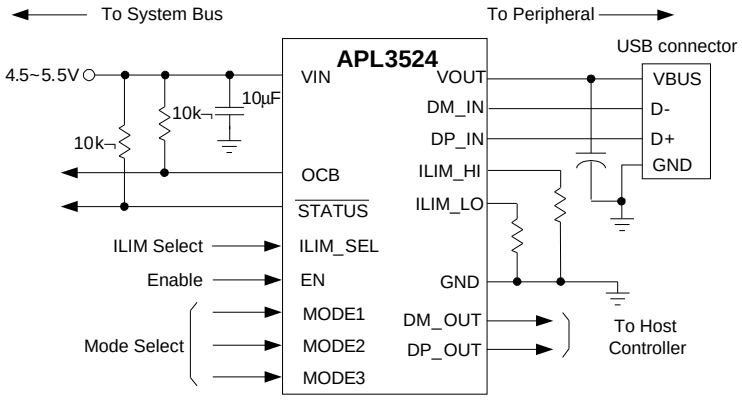
Pin Description

PIN		FUNCTION
NO.	NAME	
1	VIN	Input Voltage. Connect a 0.1μF or greater ceramic capacitor from VIN to GND as close to the device as possible
2	DM_OUT	D- data line output. Connect this pin to USB host controller.
3	DP_OUT	D+ data line output. Connect this pin to USB host controller.
4	ILIM_SEL	Logic-level input signal used to dynamically charge power switch current limit threshold; logic low selects ILIM0, logic high selects ILIM1.
5	EN	Logic-level control input for turning the power switch and the signal switches on/off. When EN is low, the device is disabled, the signal and power switches are off.
6	MODE1	Logic-level control inputs for controlling the charging mode and signal switches.
7	MODE2	
8	MODE3	
9	$\overline{\text{STATUS}}$	Active-low open drain output, asserted in load detection conditions.
10	DP_IN	D+ data line input. Connect this pin to USB peripheral.
11	DM_IN	D- data line input. Connect this pin to USB peripheral.
12	OUT	Power switch output.
13	OCB	An active-low open-drain output for over current events indication, asserted during over-temperature or current limit conditions.
14	GND	Ground.
15	ILIM_LO	An external resistor from this pin to ground sets the current limit threshold, recommended 16.9kΩ≦R_{ILIM}≦750kΩ.
16	ILIM_HI	An external resistor from this pin to ground sets the current limit threshold; recommended 16.9kΩ≦R_{ILIM}≦750kΩ.

Block Diagram



Typical Application Circuit



Function Description

Overview

As the USB ports on PC become popular for exchanging data between host and portable peripherals they become convenient places for replenishing portable devices'batteries. Many of these portable devices are with high ampere-hour batteries and thus need higher charging rate for recharging. However, not every USB port can support sufficient current for charging. In a traditional USB2.0 port, the current from it is not allowed to exceed 500mA after being enumerated. The USB3.0 port raises its supporting current to 900mA to downstream device after being enumerated. A mere 500mA or 900mA may not be adequate for charging batteries of many portable devices of nowadays. The success of USB has made the mini-USB a popular choice for wall adapter cables. A wall adapter can support current higher than 500mA/900mA. Since the USB2.0/3.0 constrains the USB port supporting current, some standards such as Battery Charging Specification Revision 1.2 (BC1.2) and Chinese Telecommunications Industry Standard YD/T 1591-2009 define some hand-shaking protocols that permit hosts and peripherals to draw current exceeding 500mA/900mA in charging. Some portable device maker such as Apple or Samsung has its own proprietary charging schemes to break the current barrier that USB2.0/3.0 has defined. The APL3524 are compliant with BC1.2 and YD/T 1591-2009 while supports most of the devices from Samsung and Apple. BC1.2 lists three different port types as listed below:

1. Standard Downstream Port
2. Charging Downstream Port
3. Dedicated Charging Port

BC1.2 defines a charging port as a downstream facing USB port that provides power for charging portable equipment, under this definition CDP and DCP are defined as charging ports

Standard Downstream Port

A Standard Downstream Port (SDP) is a traditional USB port that complies with the USB2.0/3.0 definition of a host or hub. An SDP expects a downstream device with a good battery to draw current up to 500mA/900mA (USB2.0/USB3.0) per port. In a SDP, USB traffic is allowed while battery charging can be in progress. The APL3524 supports SDP mode when control pins (MODE1~MODE3) are configured in SDP mode.

Charging Downstream Port

A Charging Downstream Port (CDP) is defined by USB BC1.2 and is USB 2.0/3.0 complied except that it shall support charging current up to 1.5A per port. The difference between CDP and SDP is the hand-shaking logic that follows BC1.2. The handshaking of CDP is done in two steps. During the step one the DM_IN outputs a voltage of V_{DM_SRC} when DP_IN senses a voltage from peripheral greater than V_{DAT_REF} but less that V_{LGC_SRC}. When the step one is done. The peripheral concludes it is connected to a CDP or DCP port rather than SDP and goes for step two. In the step two, the peripheral determines if it is connected to a CDP or DCP by outputting a nominal 0.6V voltage on DM_IN. The peripheral concludes it is a CDP port if it receives the voltage on DP_IN is less than the nominal 0.3V and a DCP port if it receives the voltage on DP_IN is greater than the nominal 0.3V. The APL3524 supports CDP mode when control pins (MODE1~MODE3) are configured in CDP mode.

Function Description

Dedicated Charging Port

A Dedicated Charging Port (DCP) is as its name's implication that provides power for battery charging but does not support USB data communication to an upstream port. The APL3524 emulates a DCP in some charging modes: DCP Shorted, DCP Divider1 and DCP Auto. In DCP Shorted mode, the APL3524 short the DP_IN with DM_IN via a shorting resistor 125Ω which meets BC1.2 and Chinese Telecommunications Industry Standard YD/T 1591-2009. In DCP Divider1, the APL3524 outputs 2V and 2.7V respectively on the DP_IN pin and DM_IN pin. The DCP Divider1 is compliant with Apple device such as iPod and iPhone. In DCP Auto mode, the APL3524 conditionally switches modes between DCP shorted, DCP Divider1, DCP Divider2 and 1.2V mode, to support non-BC1.2 devices. When MODE1~MODE3 are configured in DCP Auto mode, it starts in Divider1 mode, however if a BC1.2/ YD/T 1591-2009 compliant is attached, the APL3524 responds by discharging OUT, turning back on the power switch and operating in 1.2V mode for a fixed period and then moving to DCP Shorted mode, it then stays in that mode until the device releases the data line, in which case it goes back to Divider1 mode. When a Divider1 compliant device is attached in DCP Auto mode, the APL3524 will stay in Divider1 mode. When a Divider2 compliant device is attached in DCP Auto mode, the APL3524 will transfer to Divider2 mode until the attached device is unattached. In Divider2, the APL3524 outputs 2.7V and 2V respectively on the DP_IN pin and DM_IN pin.

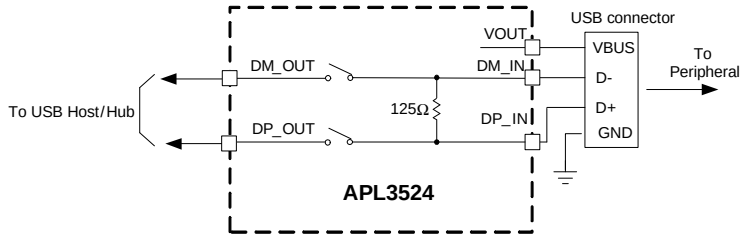


Figure 1. DCP Shorted mode

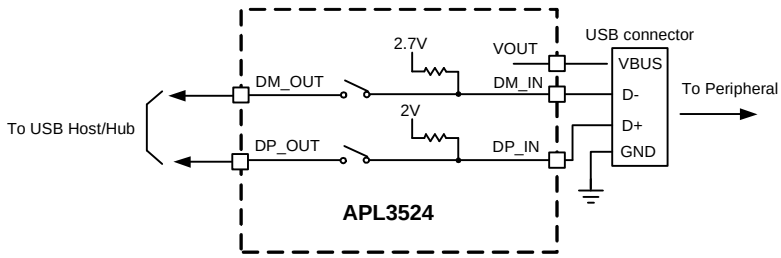


Figure 2. Divider1 mode

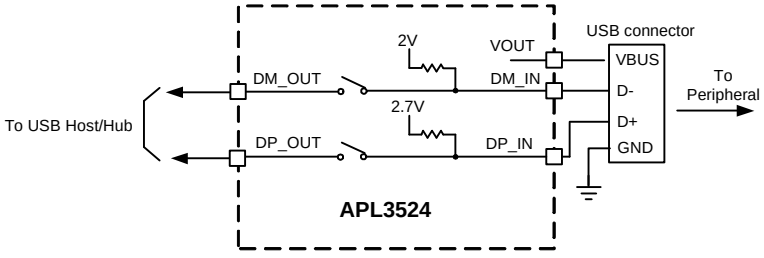


Figure 3. Divider2 mode

Function Description

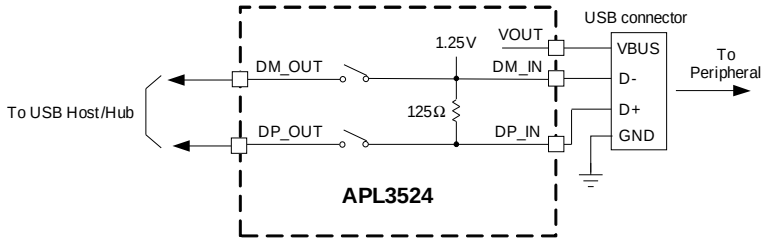


Figure 4. 1.2V mode

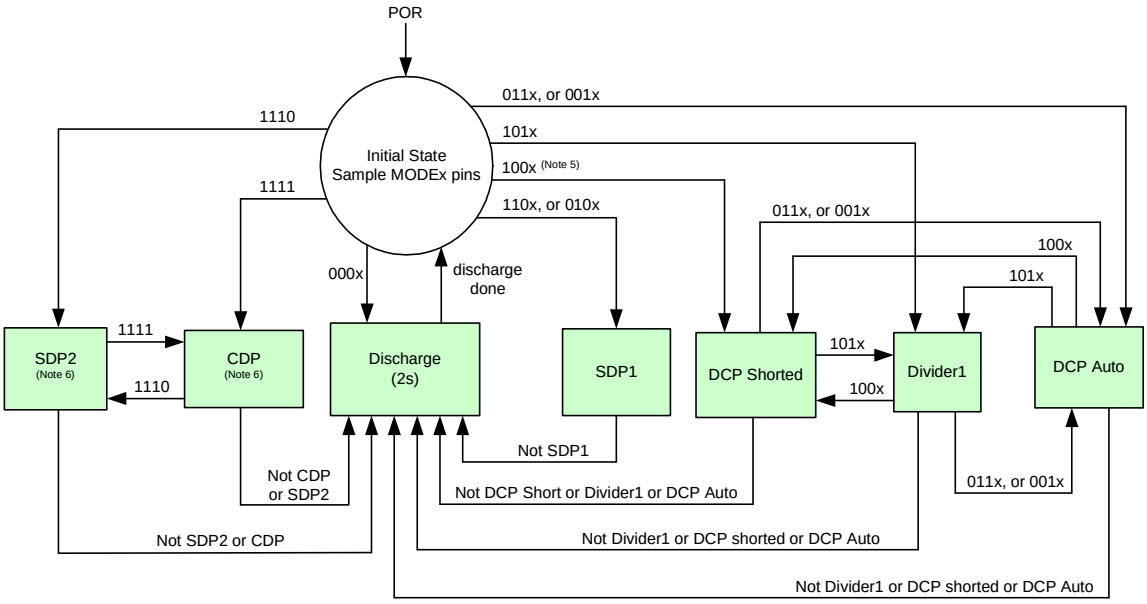
High Bandwidth Data Line Switches

The APL3524 integrates D+ and D- data lines switches for passing through data between host and peripherals without corrupting signal integrity in CDP or SDP mode. The data line switches support USB2.0 communication only. In the case of USB3.0 bus, please connect the data line directly between host and USB connector without passing through the APL3524. The data line switches operate based on these following criteria:

1. In any of SDP or CDP mode, the data switches are ON.
2. The data switches are OFF when EN or MODE1~ MODE3 are held low.
3. If current limit occurs in power switch, the data switches are still ON.
4. Data switches are OFF when power switch is in discharge state.

Charging Mode Flow Diagram

Below is a diagram that depicts how the APL3524 transfer charging states. Following a POR, the APL3524 enters initial state and will change state depending on the status of MODE1~ MODE3 and ILIM_SEL pins.



Note 5: The numbers on each flow line represent the status of MODE1~ MODE 3 and ILIM_SEL accordingly. Having "100x" for example, the first position "1" means MODE1=1, the second position "0" means MODE2=0, likewise, the third position "0" means the MODE3=0, and the forth position "x" means ILIMSEL=don't care. Please see below table for each flow line condition corresponding to charging mode.

Note 6: No OUT discharge when changing between 1111 and 1110.

Function Description

Flow Line Condition				Charging Mode
MODE1	MODE2	MODE3	ILIM_SEL	
0	0	0	x	Discharge
1	1	1	1	CDP
1	1	1	0	SDP2 (no discharge from/to CDP)
1	1	0	x	SDP1 (discharge from/to any charging mode including CDP)
0	1	0	x	
1	0	0	x	DCP Shorted
1	0	1	x	Divider1
0	1	1	x	DCP Auto
0	0	1	x	

Wake on USB

When system is placed in sleeping mode, or S3 mode, the data line switches are presumably put into OFF state while APL3524 is in DCP_Auto mode. However, Wake on USB function requires data lines to be connected to the host for conveying wake-up signals from a low or full speed HID (human interface device like mouse/keyboard). When MODEx pins are configured in CDP or SDP the APL3524 monitors both DM_IN and DP_IN pin for detecting LS or FS HID device attachment. If a LS or FS HID device is attached while one of the following MODEx changes occurs, the data line switches will be continuously connected even in DCP Auto mode until they are used to wake the system. When a FS device is used for wakeup function, there is a 60 seconds requirement that must be met. (Note 7) The following MODEx changes support Wake on USB when you are using LS or FS HID device.

1. MODE1/2/3=1/1/1 (CDP/SDP2, while system in S0) to 0/1/1 (DCP Auto, while system in S3)
2. MODE1/2/3=0/1/0 (SDP1, while system in S0) to 0/1/1 (DCP Auto, while system in S3)

Nowadays a high-speed(HS) mouse/keyboard is developed for gaming usage. Please note that the APL3524 will not support such a high speed USB device for wakeup function when the above mentioned MODEx changes are used. However, the wakeup function by using HS mouse/keyboard can be still supported If you configure APL3524 in SDP, SDP2 or CDP mode while system is in S3/S5 state. Wakeup from SDP, SDP2 or CDP mode when system in S3/S5 state does not require the regulation of 60-second.
The following MODEx changes support Wake on USB when you are using LS ,FS or HS HID device.

3. MODE1/2/3=1/1/1 (CDP/SDP2, while system in S0) to 1/1/1 (CDP/SDP2, while system in S3)
4. MODE1/2/3=0/1/0 (SDP1, while system in S0) to 0/1/0 (SDP1, while system in S3)

Note 7: If system is placed in sleep mode earlier than the 60 second window, a FS device may not get recognized and hence could fail to wake system from S3. This requirement does not apply for LS device.

Function Description

Truth Table

The Truth Table lists all combinations for all control pins MODEx and ILIM_SEL and their corresponding charging mode. Note that the current limit setting governed by the resistor on ILIM_LO or ILIM_HI or by the internal load detection threshold may change as mode changes. The column “System globe power state” provides suggestions to system designers on how to configure charging modes per system global power states(S0~S5). The power states listed in below table are suggestions rather than restrictions. System designer may have any match of charging mode and system power state. Since the APL3524 is unconscious of system global power states, the match with power state relies on system designer by routing MODEx and ILIM_SEL with system power state control signals. For example when system is in S0 state then set MODEx and ILIM_SEL to correspond to SDP or CDP mode. If charging is desired when system is in S3 or S4 state then system designer must set MODEx and ILIM_SEL to correspond to DCP Auto per below table and so on.

MODE1	MODE2	MODE3	ILIM_SEL	Mode	Current limit setting refers to	STATUS Output (Active Low)	Comment	System global power state
0	0	0	0	Discharge	N/A	High	OUT held low	N/A
0	0	0	1	Discharge	N/A	High		N/A
0	0	1	0	DCP Auto	ILIM_HI	High	Data lines disconnected	S3/S4/S5
0	0	1	1	DCP Auto	I_{OS_PW} & ILIM_HI (Note 8)	DCP load preset, held low (Note 9)	Data lines disconnected and Power Wake function active	S4/S5
0	1	0	0	SDP1	ILIM_LO	High	Data lines connected	S3
0	1	0	1	SDP1	ILIM_HI	High		S3
0	1	1	0	DCP Auto	ILIM_HI	High	Data lines disconnected	S3
0	1	1	1	DCP Auto	ILIM_HI	DCP load preset, held low (Note 10)	Data lines disconnected, Port Power Management function active	S3
1	0	0	0	DCP Shorted	ILIM_LO	High	Device forced to stay in BC1.2 shorted mode	N/A
1	0	0	1	DCP Shorted	ILIM_HI	High		N/A
1	0	1	0	Divider1	ILIM_LO	High	Device forced to stay in Divider1 mode	N/A
1	0	1	1	Divider1	ILIM_HI	High		N/A
1	1	0	0	SDP1	ILIM_LO	High	Data lines connected	S0
1	1	0	1	SDP1	ILIM_HI	High		S0
1	1	1	0	SDP2	ILIM_LO	High		S0
1	1	1	1	CDP	ILMI_HI	CDP load preset (Note 11)	Data lines connected and load detect active	S0

Note 8: The current limit setting is automatically switched between IOS_PW and the resister value on ILIM_HI according to the Power Wake functionality(for more details see Power Wake).

Note 9: DCP load present governed by the “Load Detection-Power Wake” limits.

Note 10: DCP load present governed by the “Load Detection-Port Power Management”.

Note 11: CDP load present governed by the “Load Detection-Port Power Management” and BC1.2 primary detection.

Function Description

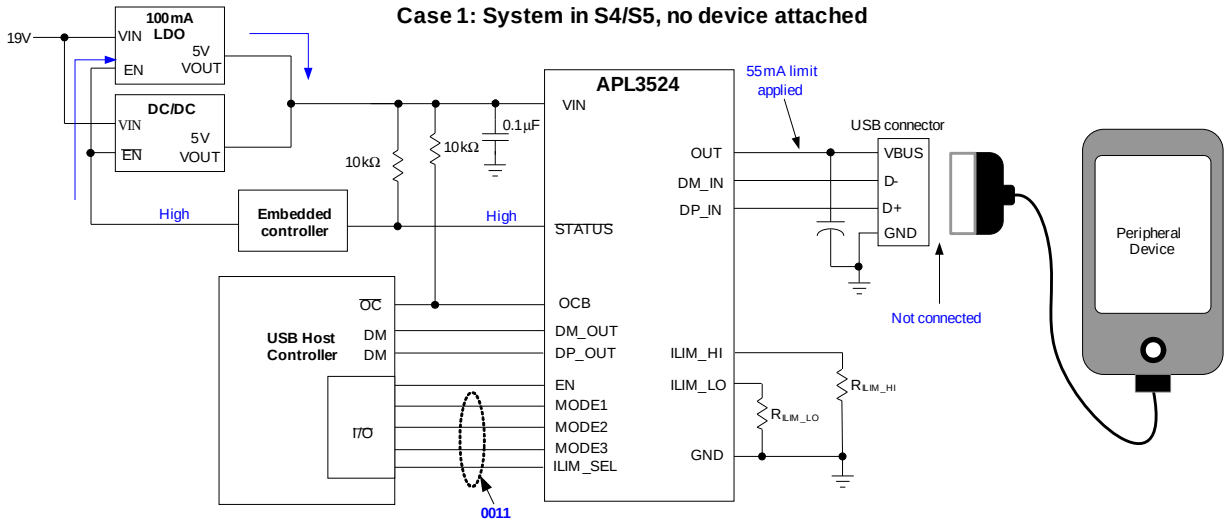
Load Detection

The APL3524 implements 2 schemes for power management via /STATUS pin by monitoring load current at OUT pin. The 2 schemes are:

1. Power Wake.
2. Port Power Management.

Power Wake

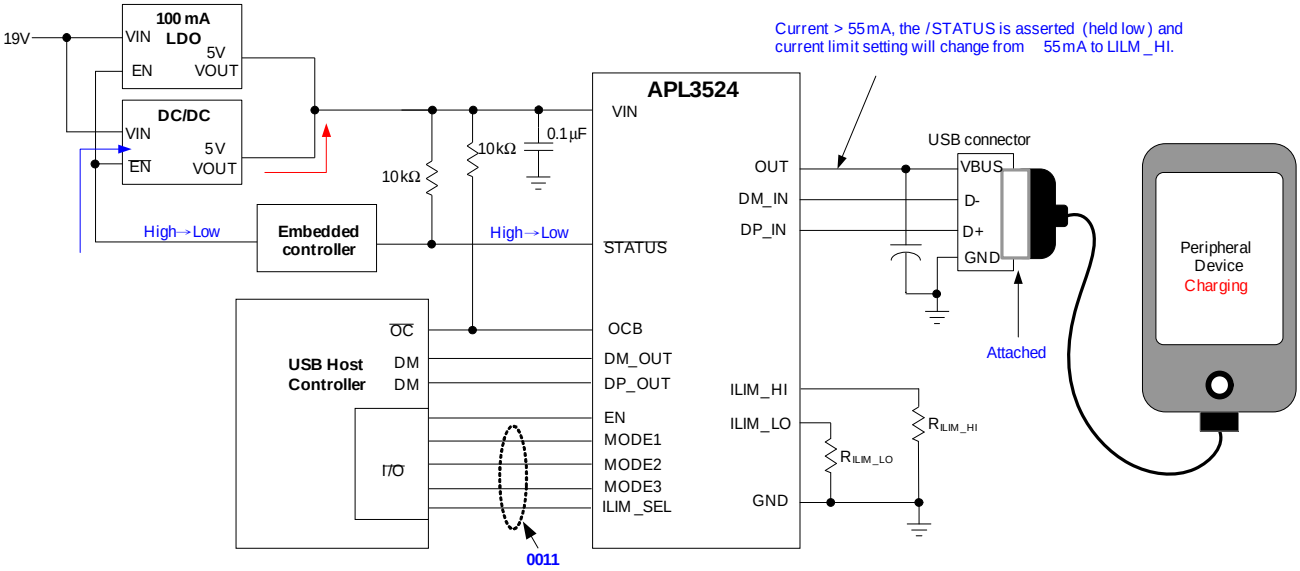
Power Wake function aims to save power for the system when system is in deep sleep state (S4/S5). In general Power Wake function is used mainly in mobile systems like a notebook where it is imperative to save battery power, and therefore battery run time is extended. When the control pins of APL3524 are configured at 0011 (see Truth Table), the Power Wake function is active. The APL3524 will monitor load current at OUT pin and provide /STATUS pin for power path control. As shown in below Case 1 diagram when system is in S4/S5 state and no device is connected to the USB port system is powered by a 100mA LDO (low IQ, high efficiency). In this state the current limit setting of APL3524 is internally fixed at 55mA regardless of ILIM_HI and ILIM_LO settings.



Function Description

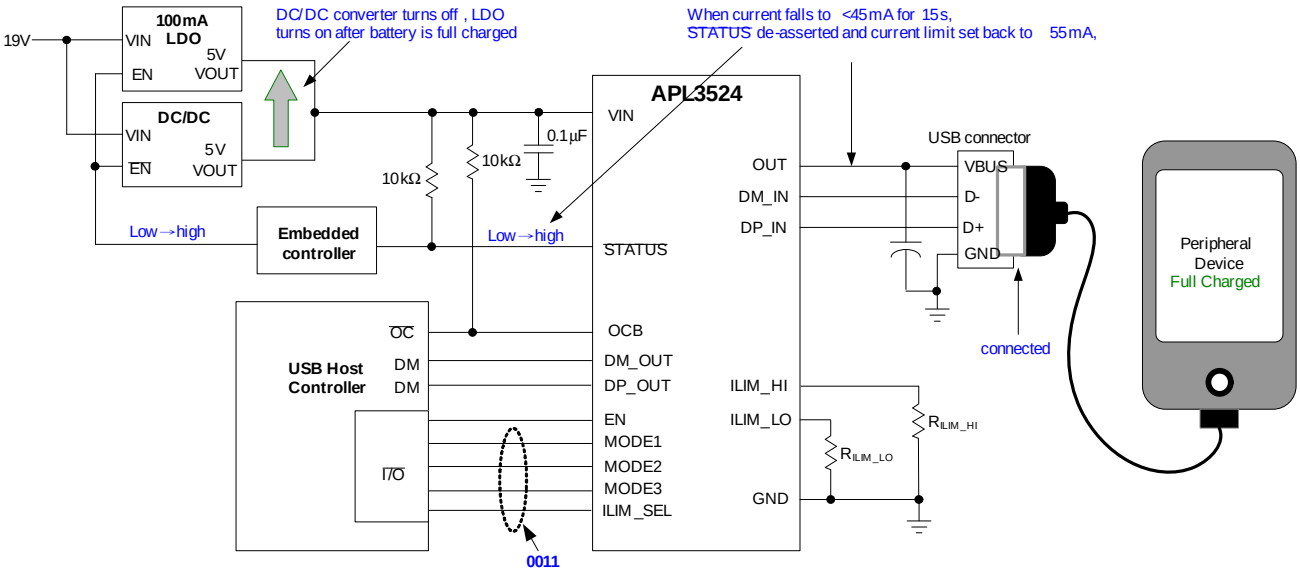
When a device is attached, as shown in below Case 2 diagram, and current drawn from OUT exceeds 55mA limitation the APL3524 will assert /STATUS to turn on the main power supply (DC/DC) and discharge VBUS for 2s(typ.). After the discharge the APL3524 will turn back on and then set the current limit at ILIM_HI. Afterward the DC/DC converter provides the power to the system and charging current to the peripheral.

Case 2: System in S4/S5 device attached and charging



In Case 3, APL3524 will monitor the load current at OUT pin while the peripheral device is in charging state. When the charging current drops below 45mA for a continuous period of 15s, the APL3524 assumes the peripheral device is fully charged and then de-asserts /STATUS and sets the current limit back to 55mA.

Case 3: System in S4/S5 device attached and charging completed



Function Description

Port Power Management

Port Power Management is for systems that deploy multiple charging ports but have load budget that forbids the ports simultaneously to draw high current. The Port Power Management functionality is active when control pins of MODEx, ILIM_SEL are configured at 0111 or 1111(see Truth Table). When current at OUT exceeds the Port Power Management threshold, or ILIM_LO+60mA, the /STATUS will be asserted to notify system that high current is present. When the maximum allowed number of ports assert /STATUS, the remaining ports are toggled to a non-charging port. Non-charging port are SDP ports with current limit set by ILIM_LO. The APL3524 allows a system to toggle between charging and non-charging ports either with or without VBUS discharge. For example when a port is in SDP2 mode (1110) and its ILIM_SEL pin is toggled to 1 due to another port releasing its high current requirements. The SDP2 port will automatically revert to CDP mode (1111) without a discharge event. This is desirable if this port was connected to a media device where it was syncing data from the SDP2 port; a discharge event would mess-up the syncing activity on the port and cause user confusion.

Figure 5 below is an example of an implementation of Port Power management. The example has two charging ports, each port with its own APL3524. Both ports are all configured at 0111(in S3 state) or 1111(in S0 state) initially, and current limit are all set by ILIM_HI that can support 1.5A each. In the implement the system's 5V can only support 2.5A maximum, so the current drawn from each port can not reach 1.5A simultaneously. When the load in one of the two ports, in this case the port #1, exceeds ILIM_LO+60mA for 200ms its /STATUS will be asserted and be received by the port #2. The port #2 receives /STATUS from neighborhood will then be configured in SDP mode and the current limit is set by ILIM_LO that only supports 0.9A in this case. After the port #1 de-asserts its /STATUS (ex, HDD has been pulled out of port #1), the port #2 will be set back to a charging port. Note that the Port Power Management threshold, ILIM_LO+60mA, is a threshold used to notify the system when the high power is present but not a current limit threshold. With the implement of Port Power Management in a system the power supply can be designed for a reasonable charging load while providing all ports the high charging capability.

Function Description

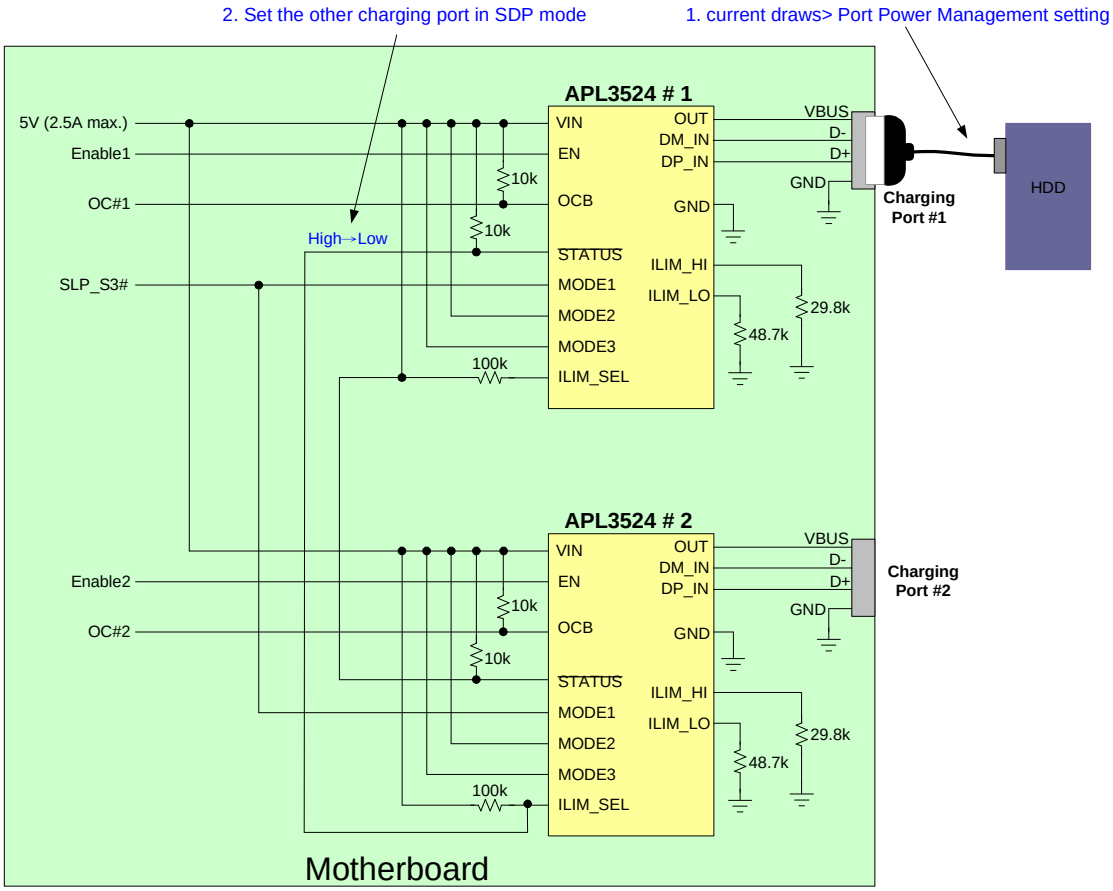


Figure 5. Implement of Port Power Management

OCB Output

The APL3524 provides an open-drain output to indicate that a fault has occurred.
When any of current-limit or over-temperature protection occurs for a deglitch time of $t_{D(OCB)}$, the OCB goes low. The OCB keeps in low until the fault has been removed. Since the OCB pin is an open-drain output, connecting a resistor to a pull high voltage is necessary.

Enable/Disable

The APL3524 provides an EN input pin for enable/disable control. Pulling the EN pin logic low disables the device. When IC is disabled, the power switch and data switches are all in OFF state, the OUT in discharge and the VIN supply current is educed to less than 2μA. The enable input is compatible with both TTL and CMOS logic levels. The EN pin cannot be left floating.

Function Description

Power Switch

The power switch is an N-channel MOSFET with a low RDS(ON). The internal power MOSFET does not have the body diode. When IC is off, the MOSFET prevents a current flowing from the VOUT back to VIN and VIN to VOUT.

VIN Under-Voltage Lockout (UVLO)

The APL3524 has a built-in under-voltage lockout circuit to keep the output shutting off until internal circuitry is operating properly. The UVLO circuit has hysteresis and a de-glitch feature so that it will typically ignore undershoot transients on the input. When input voltage exceeds the UVLO threshold, the output voltage starts a soft-start to reduce the inrush current.

Current-Limits and Settings

The APL3524 has current limit function to limit load current at current limit threshold in over-load conditions. When device operates in current limiting, the output current is limited and the output voltage is reduced accordingly. At the instant the overload occurs, high currents may flow for microseconds before the current-limit circuit can react. The device has two independent current limit setting pins ILIM_HI and ILIM_LO.

Each pin with a resistor to ground sets a current limit threshold. At a time, only one current limit threshold is valid. The ILIM_SEL input pin is used to choose either ILIM_HI or ILIN_LO the candidate of current limit setting. Both settings have the same relation between the current limit and the programming resistor. The following equation programs the typical current limit:

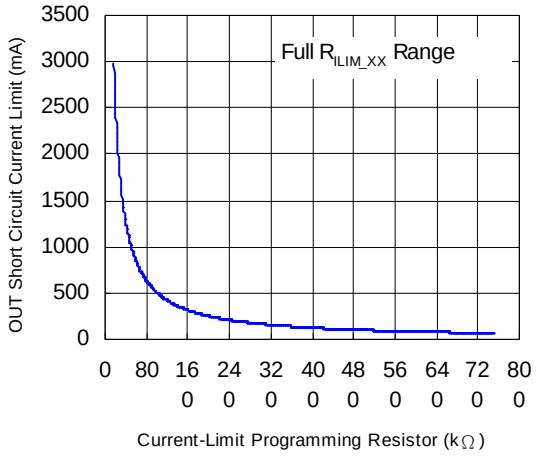
I_{CL}(mA) typ.=50250/R_{ILIM_XX}(kΩ)

R_{ILIM_XX} corresponds to either R_{ILIM_HI} or R_{ILIM_LO} as ILIM_SEL sets. Please consult the Truth Table to see how ILIM_SEL relates to ILIM_HI and ILIM_LO.

R_{ILIM_LO} is optional and the ILIM_LO pin may be left unconnected if the following conditions are met:

1. ILIM_SEL is always set high
2. Load Detection - Port Power Management is not used

Typical Current Limit Setting vs. Programming Resistor



Function Description

Over-Temperature Protection

When the junction temperature exceeds 140°C, the internal thermal sense circuit turns off the power FET and allows the device to cool down. When the device's junction temperature cools by 20°C, the internal thermal sense circuit will enable the device, resulting in a pulsedoutput during continuous thermal protection. Thermal protection is designed to protect the IC in the event ofover temperature conditions. For normal operation, the junction temperature cannot exceed T_J=+125°C.

Application Information

Input Capacitor

A 1µF or higher ceramic bypass capacitor from VIN to GND, located near the APL3524, is strongly recommended to suppress the ringing during short circuit fault event. When the load current trips the SCP threshold in an over load condition such as a short circuit, hot plug-in or heavy load transient the IC immediately turns off the internal power switch that will cause V_{IN} ringing due to the inductance between power source and VIN. Without the bypass capacitor, the output short may cause sufficient ringing on the input to damage internal control circuitry.
Input capacitor is especially important to prevent V_{IN} from ringing too high in some applications where the inductance between power source to VIN is large (ex, an extra bead is added between power source line to VIN for EMI reduction), additional input capacitance may be needed on the input to reduce voltage overshoot from exceeding the absolute maximum voltage of the device during over load conditions.

Output Capacitor

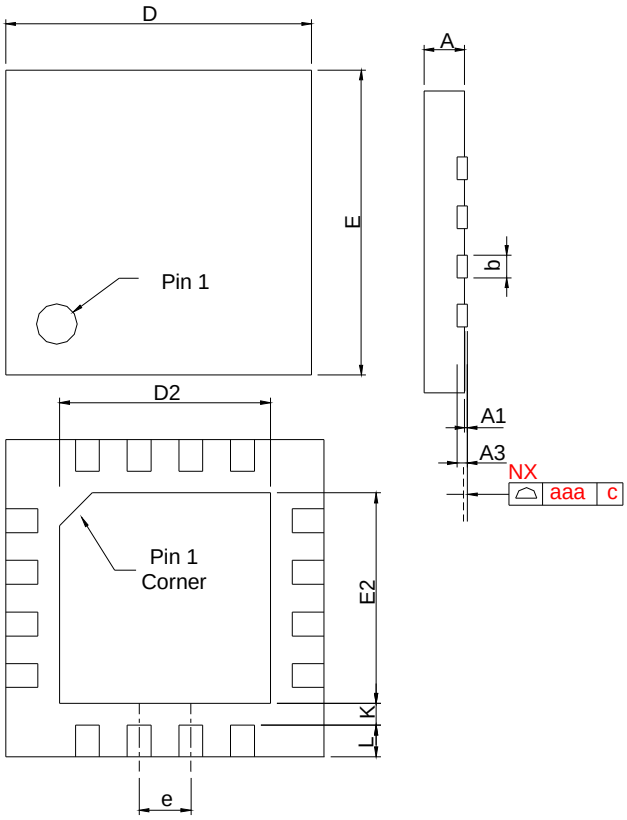
A low-ESR 150µF aluminum electrolytic or tantalum between VOUT and GND is strongly recommended to reduce the voltage droop during hot-attachment of downstream peripheral. (Per USB 2.0, output ports must have a minimum 120µF of low-ESR bulk capacitance per hub). Higher-value output capacitor is better when the output load is heavy. Additionally, bypassing the output with a 0.1µF ceramic capacitor improves the immunity of the device to short-circuit transients.

Layout Consideration

The PCB layout should be carefully performed to maximize thermal dissipation and to minimize voltage drop, droop and EMI. The following guidelines must be considered:
1. Please place the input capacitors near the VIN pin as close as possible.
2. Output decoupling capacitors for load must be placed near the load as close as possible for decoupling high frequency
ripples.
3. Locate APL3524 and output capacitors near the load to reduce parasitic resistance and inductance for excellent load transient performance.
4. The traces routing the R_{ILIM_XX} resistors should be a sufficiently low resistance as to not affect the current-limit accuracy.
5. The negative pins of the input and output capacitors and the GND pin must be connected to the ground plane of the load.
6. Keep VIN and VOUT traces as wide and short as possible.

Package Information

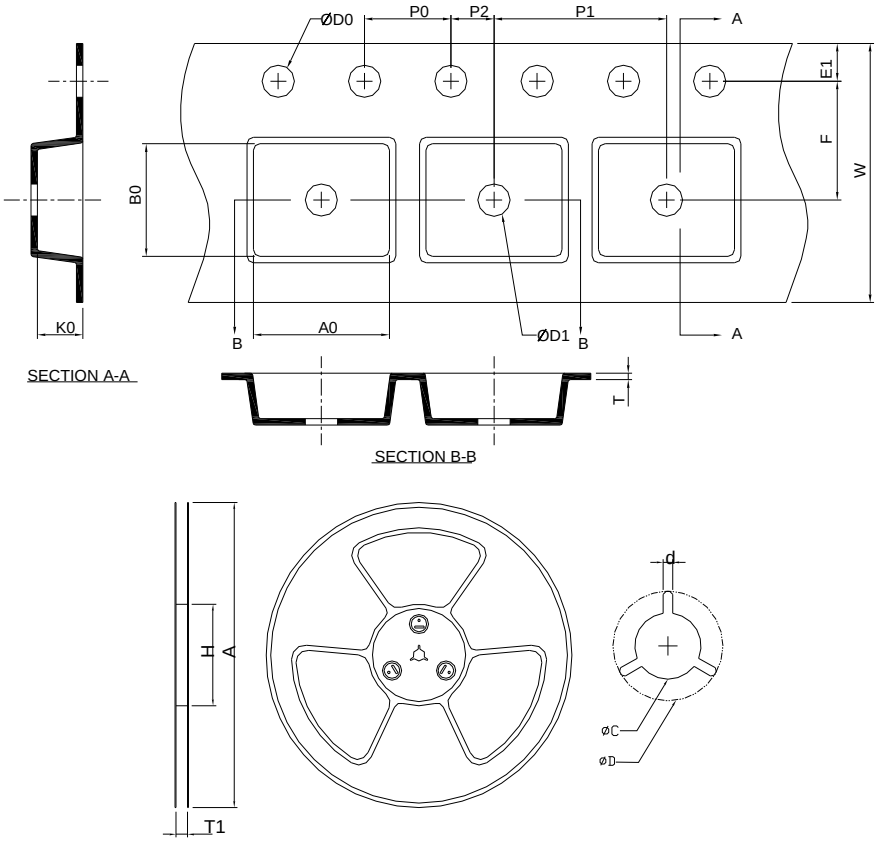
TQFN3x3-16



SYMBOL	TQFN3*3-16			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	2.90	3.10	0.114	0.122
D2	1.50	1.80	0.059	0.071
E	2.90	3.10	0.114	0.122
E2	1.50	1.80	0.059	0.071
e	0.50 BSC		0.020 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	
aaa	0.08		0.003	

Note : Follow JEDEC MO-220 WEED-4.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFN3x3-16	330±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.00±0.20

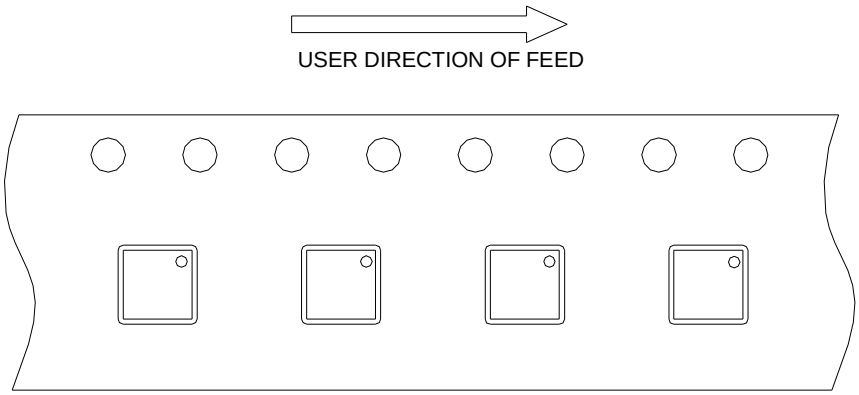
(mm)

Devices Per Unit

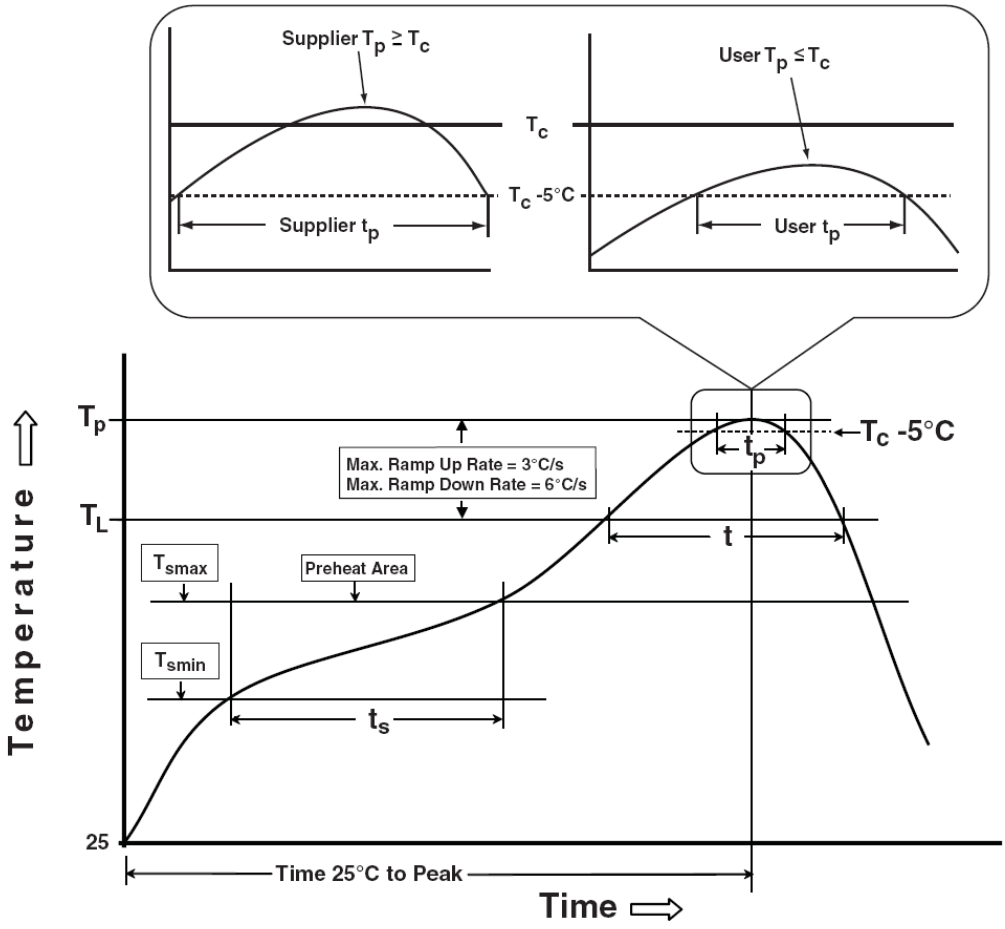
Package Type	Unit	Quantity
TQFN3x3-16	Tape & Reel	3000

Taping Direction Information

TQFN3x3-16



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 3350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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