Ultra-Low On-Resistance, 6A Dual Load Switch with Soft Start

Features

- **Ultra-Low On-Resistance**
  -APL3538A/B: 20mΩ (Max.)
  -APL3538C/D: 35mΩ (Max.)
- **Low Quiescent Current: 30μA(max)**
- **Soft Start Time Programmable by External Capacitor**
- **Wide Input Voltage Range (VIN): 0.8V to 5.5V**
- **Supply Voltage Range (VDD): 3V to 5.5V**
- **Over-Current Protection (OCP)**
- **Enable Control Function**
- **Output Discharge when Switch Disabled**
- **Reverse Current Blocking when Switch Disabled**
- **Over-Temperature Protection with Hysteresis**
- **Tiny small TQFN2x2-14 Package**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Gereral Description

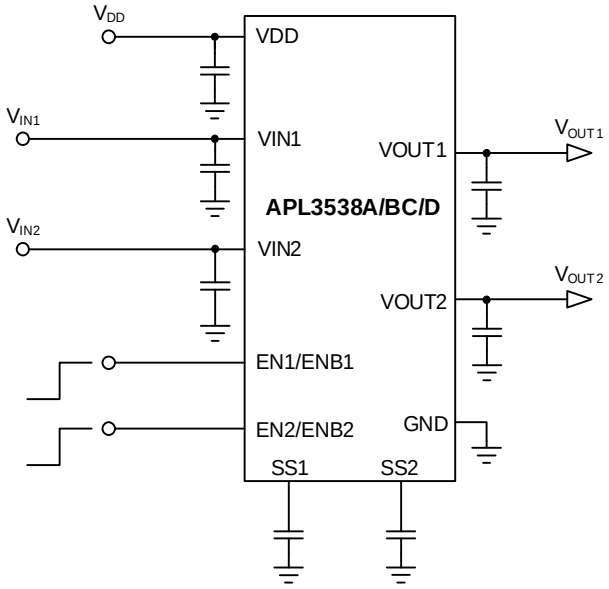
The APL3538 is an ultra-low On-resistance, dual power-distribution switch with external soft start control. It integrates two N-channel MOSFETs that can deliver 6A continuous load current each. The APL3538 can be enabled by other power systems. Pulling and holding the voltage of EN pin (APL3538A) below 0.4V shuts off the output. Pulling and holding the voltage of ENB pin (APL3538B) below 0.4V enable the output. The device integrates some protection features, including Over-Current Protection (OCP) and Over-Temperature Protection (OTP). The OCP can protect the device against current over-loads or short-circuit events. The OTP function shuts down the N-channel MOSFET power switch when the junction temperature rises beyond 150°C and will automatically turns on the power switch when the temperature drops by 30°C.

The device is available in lead free TQFN2x2-14 package.

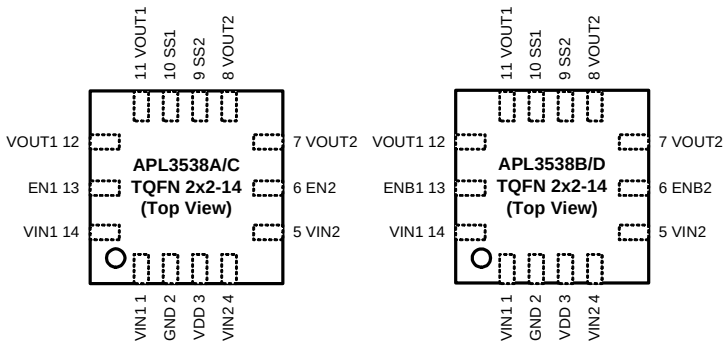
Applications

- **Notebooks**
- **Tablet PC**
- **AIO PC**

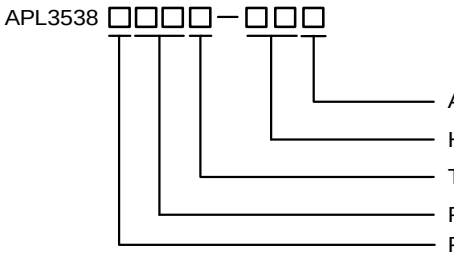
Simplified Application Circuit



Pin Configurations



Ordering and Marking Information



Product Code (Enable Function / $R_{DS(ON)}$)
A : Active High / 16mΩ (Typ.)
B : Active Low / 16mΩ (Typ.)
C : Active High / 25mΩ (Typ.)
D : Active Low / 25mΩ (Typ.)
Package Code
QB : TQFN2x2-14
Operating Ambient Temperature Range
I : -40 to 85°C
Handling Code
TR : Tape & Reel
Assembly Material
G : Halogen and Lead Free Device

APL3538A QB:	L38A • X	X - Date Code
APL3538B QB:	L38B • X	X - Date Code
APL3538C QB:	L38C • X	X - Date Code
APL3538D QB:	L38D • X	X - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter		Rating	Unit
V_{DD}	VDD to GND Voltage		-0.3 ~ 6	V
V_{INx}	VINx to GND Voltage		-0.3 ~ 6	V
V_{OUTx}	VOUTx to GND Voltage	>10μ sec pulse width	-0.3 ~ 6	V
		<10μ sec pulse width	-1.4 ~ 6	V
V_{DSx}	VINx to VOUTx Voltage	<100n sec pulse width	8	V
V_{ENx}	ENx to GND Voltage		-0.3 ~ 6	V
V_{ENBx}	ENBx to GND Voltage		-0.3 ~ 6	V
I_{OUTx}	Continuous Output Current, IOUTx		Internally Limited	A
T_J	Maximum Junction Temperature		-40 ~ 150	°C
T_{STG}	Storage Temperature		-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)		260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance in free air (Note 2) TQFN2x2-14	70	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{DD}	VDD Input Voltage ($V_{DD} \geq V_{IN}$)	3.0 ~ 5.5	V
V_{INx}	VINx Input Voltage	0.8 ~ 5.5	V
I_{OUTx}	VOUTx Output Current (Single Channel)	0 ~ 6	A
	Maximum Pulse Current, Pulse<300μs, 1% Duty Cycle (Single Channel)	8	A
V_{IHx}	ENx/ENBx Logic High Input Voltage	1 ~ 5.5	V
V_{ILx}	ENx/ENBx Logic Low Input Voltage	0 ~ 0.4	V
C_{SSx}	SSx Capacitance	0 ~ 10	nF
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3 : Refer to the typical application circuit.

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{INx}= 5V, V_{DD}=5V, V_{ENx}=5V (or V_{ENBx}=0V) and T_A=-40~85°C. Typical values are at T_A=25°C.

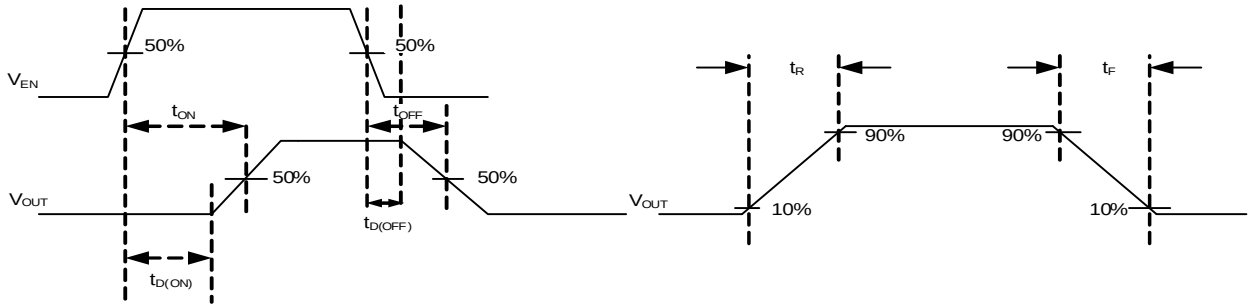
Symbol	Parameter	Test Conditions	APL3538A/B/C/D			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
	VDD Supply Current (both channels)	No load	–	20	30	μA
	VDD Supply Current (single channel)	No load	–	15	25	μA
	VDD Supply Current at Shutdown	No load, V_{DD}=5V, V_{ENx}=0V	–	–	1	μA
		No load, V_{DD}=5V, V_{ENBx}=5V	–	0.9	2	μA
	VINx Off-State Supply Current (per channel)	No load, V_{DD}=5V, V_{INx}=5V, V_{EN}=0V or V_{ENB}=5V	–	0.1	8	μA
		No load, V_{DD}=5V, V_{INx}=3.3V, V_{EN}=0V or V_{ENB}=5V	–	0.1	3	μA
		No load, V_{DD}=5V, V_{INx}=1.8V, V_{ENx}=0V or V_{ENB}=5V	–	0.1	2	μA
		No load, V_{DD}=5V, V_{INx}=0.8V, V_{ENx}=0V or V_{ENB}=5V	–	0.1	1	μA
	Reverse Leakage Current (per channel)	V_{ENx}=0V or V_{ENBx}=5V, V_{OUTx}=5.5V, V_{INx}=0V	–	0.1	16	μA
UNDER-VOLTAGE LOCKOUT (UVLO)						
	Rising VDD UVLO Threshold	V_{DD} rising, T_J=25°C	2.0	2.3	2.6	V
	VDD UVLO Hysteresis		–	0.1	–	V

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{INx}= 5V, V_{DD}=5V, V_{ENx}=5V (or V_{ENBx}=0V) and T_A=-40~85°C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APL3538A/B/C/D			Unit
			Min.	Typ.	Max.	
POWER SWITCH 1 AND POWER SWITCH 2						
$R_{DS(ON)}$	Power Switch On Resistance **(APL3538A/B)**	V_{DD}=5V, I_{OUTx}=6A, T_J=25°C	–	16	20	mΩ
		V_{DD}=3.3V, I_{OUTx}=6A, T_J=25°C	–	20	24	mΩ
	Power Switch On Resistance **(APL3538C/D)**	V_{DD}=5V, I_{OUTx}=6A, T_J=25°C	–	25	35	mΩ
		V_{DD}=3.3V, I_{OUTx}=6A, T_J=25°C	–	31	42	mΩ
OVER CURRENT PROTECTION (OCP)						
I_{OCPx}	OCP Threshold (per channel)	T_J=25°C	9	12	15	A
		T_J=-40~125°C	8	–	–	A
	OCP Response Time	VOUTx short to ground	–	–	1	µs
SOFT-START CONTROL PIN (SS1 AND SS2)						
t_R	Internal Soft-Start Time	R_{LX}=10Ω, C_{SSx}=0nF, V_{INx}=1.05V	–	12	–	µs
	SSx Discharge Resistance	V_{SSx}=6V, V_{ENx}=Low or V_{ENBx}=High, measured at SSx	–	14	–	kΩ
ENABLE INPUT PIN (EN1, EN2 OR ENB1, ENB2)						
	Input Logic HIGH		1	–	–	V
	Input Logic Low		–	–	0.4	V
	Input Current	V_{ENx}=5.5V or V_{ENBx}=5.5V	–	–	1	µA
$t_{D(ON)}$	Turn On Delay Time	C_{SSx}=0nF, R_{LX}=10Ω, From being enabled to V_{OUT} rising	–	7	–	µs
$t_{D(OFF)}$	Turn Off Delay Time	C_{SSx}=0nF, R_{LX}=10Ω	–	5	–	µs
	Output Discharge Resistance	V_{ENx}=0V or V_{ENBx}=5V, V_{OUTx} force 1V	–	100	150	Ω
OVERT-TEMPERATURE PROTECTION (OTP)						
T_{OTPX}	OTP Threshold (per channel)	T_J rising	–	150	–	°C
T_{HYS}	OTP Hysteresis		–	30	–	°C

Timing Chart



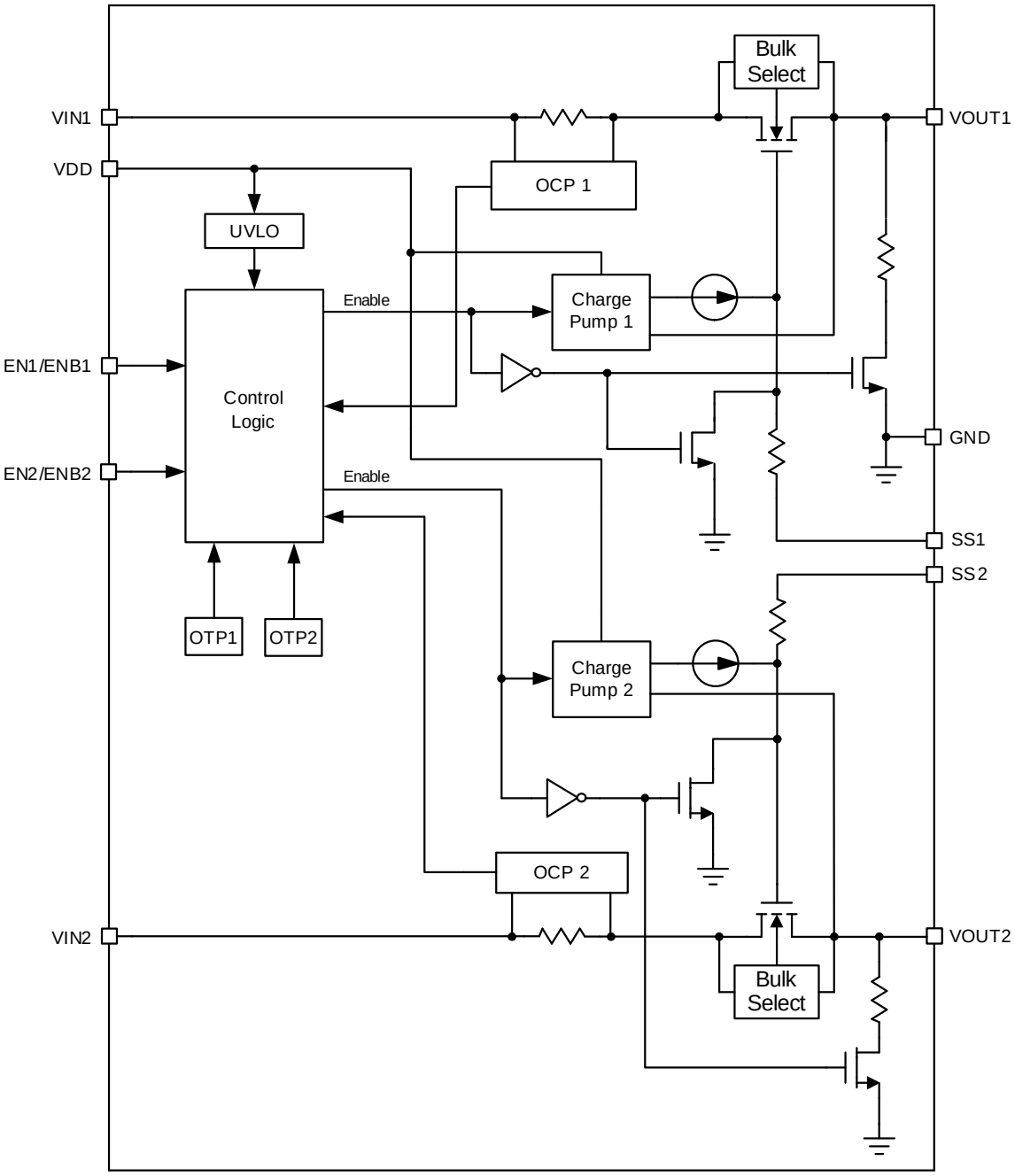
Note4: Rise and fall times of the control signal is 100ns.

Figure 1. $t_{D(ON)}/t_{D(OFF)}$, t_{ON}/t_{OFF}, t_R/t_F Waveforms

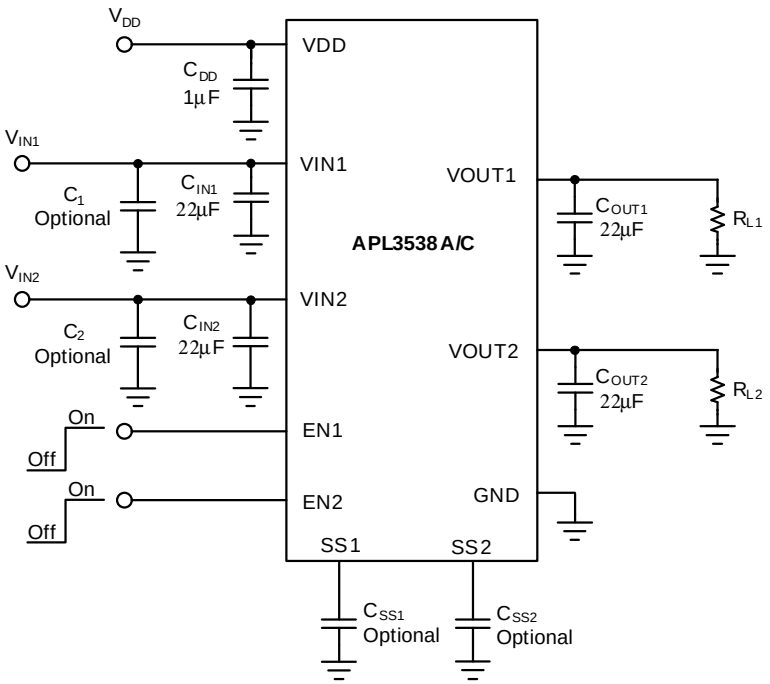
Pin Descriptions

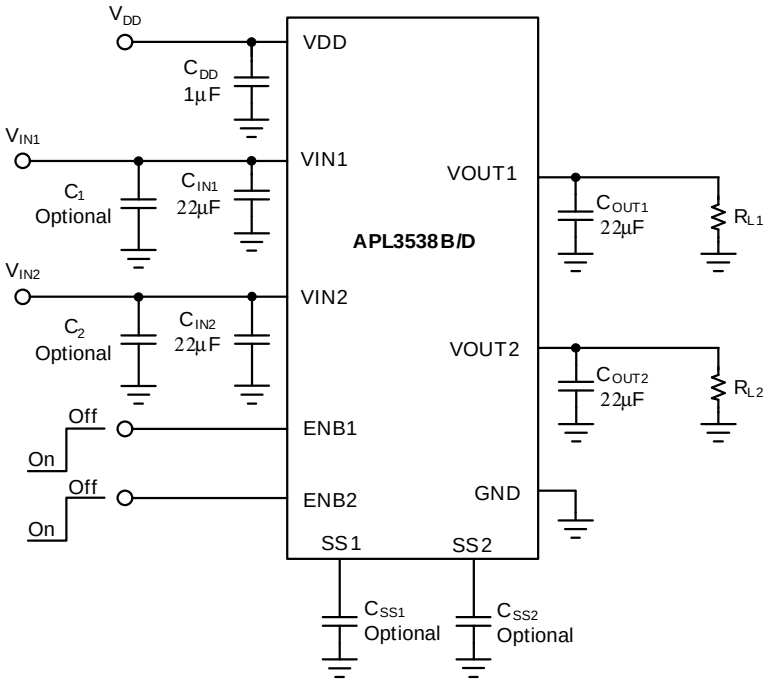
PIN		Function
NO.	NAME	
1, 14	VIN1	Power supply Input of switch 1. Connect this pin to an external DC supply.
2	GND	Power supply Input of switch. Connect this pin to an external DC supply.
3	VDD	VDD voltage input pin for internal control circuitry. Connecting this pin to a 5V or 3.3V supply voltage provides the bias for the control circuitry and charge pump.
4, 5	VIN2	Power supply Input of switch 2. Connect this pin to an external DC supply.
6	EN2	Enable input of switch 2. Logic high turns on switch. The EN2 pin cannot be left floating.
	ENB2	Enable input of switch 2. Logic low turns on switch. The ENB2 pin cannot be left floating.
7, 8	VOUT2	Output of switch 2. The output voltage follows the input voltage. When EN2 is low or ENB2 is high, the output voltage is discharged by an internal resistor.
9	SS2	Soft start control of switch 2. A capacitor from this pin to ground sets the VOUT's rise slew rate.
10	SS1	Soft start control of switch 1. A capacitor from this pin to ground sets the VOUT's rise slew rate.
11, 12	VOUT1	Output of switch 1. The output voltage follows the input voltage. When EN1 is low or ENB1 is high, the output voltage is discharged by an internal resistor.
13	EN1	Enable input of switch 1. Logic high turns on switch. The EN1 pin cannot be left floating.
	ENB1	Enable input of switch 1. Logic low turns on switch. The ENB1 pin cannot be left floating.

Block Diagram



Typical Application Circuit





Function Description

Under-voltage Lockout (UVLO)

A Under-Voltage Lockout (UVLO) circuit monitors the VDD pins voltage to prevent wrong logic controls. The UVLO function initiates a soft-start process after the VDD supply voltages exceed rising UVLO voltage threshold during powering on.

Power Switch

The power switch is an N-channel MOSFET with a ultra-low $R_{DS(ON)}$. When IC is in shutdown state ($V_{EN1,2}$=Low or $V_{ENB1,2}$=High), the MOSFET prevents a reverse current flowing from the VOUT back to VIN. When IC is in UVLO state, the internal parasitic diodes connected from VOUT to VIN will be forward biased.

Over-Current Protection (OCP)

The APL3538 power switch provides the OCP function. When the output current reaches the OCP threshold, the device is turned off and the output is latched to be floating until ENx or ENBx is toggled.

Soft-Start

The APL3538 provides an adjustable soft-start circuitry to control rise rate of the output voltage and limit the current surge ($I_{SURGE,Max}$<7.5A) during start-up. The soft-start time is set with a capacitor from the SSx pin to the ground.

Enable Control

The APL3538 has a dedicated enable pin (ENx or ENBx). A logic low/high signal applied to this pin shuts down the output. Following a shutdown, a logic high/low signal re-enables the output through initiation of a new soft-start cycle.

Over-Temperature Protection

When the junction temperature exceeds 150°C, the internal thermal sense circuit turns off the power FET and allows the device to cool down. When the device's junction temperature cools by 30°C, the internal thermal sense circuit will enable the device, resulting in a pulsed output during continuous thermal protection. Thermal protection is designed to protect the IC in the event of over temperature conditions. For normal operation, the junction temperature cannot exceed TJ=+125°C.

Application Information

Power Sequencing

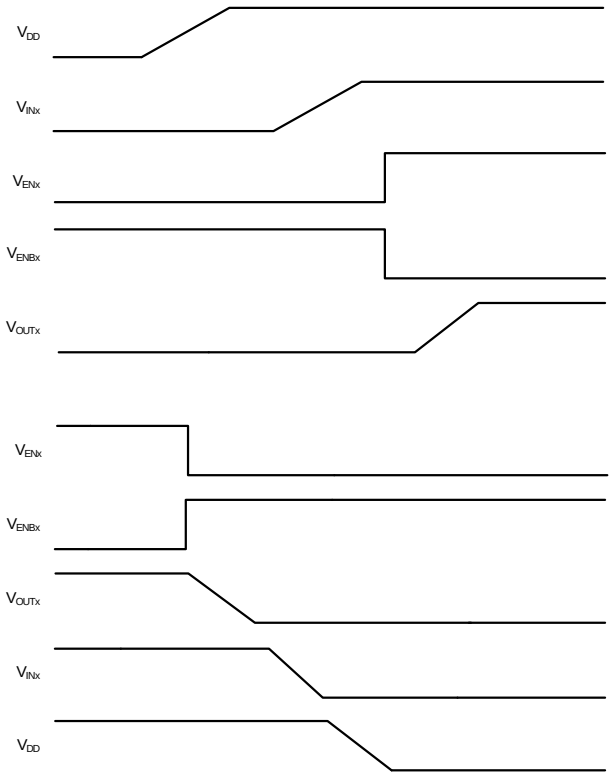


Figure 2. APL3538 Power Sequencing Diagram

The APL3538 has a built-in reverse current blocking circuit to prevent a reverse current flowing through the body diode of power switch from the VOUTx back VINx pin when power switch disabled. The reverse current blocking circuit is not active before V_{DD} is ready. When IC is in UVLO state, the internal parasitic diodes of power switch connected from VOUTx to VINx will be forward biased. Otherwise, V_{OUTx} should not be higher than V_{DD}, and V_{DD} must be higher than the voltage of any other input pin, the reason is that the internal parasitic diodes connected from VOUTx to VDD will be forward biased.

Input Capacitor Selection

The APL3538 requires proper input capacitors to supply current surge during stepping load transients to prevent the input voltage rail from dropping. Because the parasitic inductor from the voltage sources or other bulk capacitors to the VIN pin limit the slew rate of the surge currents, more parasitic inductance needs more input capacitance.

A 22µF or higher ceramic bypass capacitor from VIN to GND, located near the APL3538, is strongly. Additional input capacitance may be needed on the input to reduce voltage overshoot from exceeding the absolute maximum voltage of the device during heavy load transient or short-circuit conditions. When the load current trips the OCP threshold in an over load condition such as a short circuit, the IC immediately turns off the internal power switch that will cause V_{IN} ringing due to the parasitical inductance between power source and VIN.

Output Capacitor Selection

The APL3538 requires proper output capacitors to supply current surge during stepping load transients to prevent the output voltage rail from dropping. A 22µF ceramic bypass capacitor from VOUT to GND, located near the APL3538, is strongly. Additional output capacitance may be needed on the output to reduce voltage undershoot from exceeding the absolute maximum ratings (V_{OUTx} and V_{DSx}) of the device during OCP condition.

Thermal Consideration

The APL3538 maximum power dissipation depends on the differences of the thermal resistance and temperature between junction and ambient air. The power dissipation P_D across the device is:

$$P_D = (T_J - T_A) / \theta_{JA}$$

where (T_J-T_A) is the temperature difference between the junction and ambient air. θ_{JA} is the thermal resistance between junction and ambient air.
For normal operation, do not exceed the maximum operating junction temperature of T_J = 125°C. The calculated power dissipation should be less than:

$$P_{D(MAX)} = (125 - 25) / 70$$
$$= 1.42 \text{ (W)} \ldots\ldots T_A = 25°C$$

$$P_{D(MAX)} = (125 - 85) / 70$$
$$= 0.57\text{(W)} \ldots\ldots T_A = 85°C$$

Application Information

Thermal Consideration

To ensure proper operation, the maximum junction temperature of the APL3538 should not exceed 125°C. Several factors attribute to the junction temperate rise: load current, MOSFET on resistance, junction-to-ambient thermal resistance, and ambient temperature. The maximum load current can be determined by:

$$I_{OUT1(MAX)} + I_{OUT2(MAX)} \le \sqrt{\frac{P_{D(MAX)}}{R_{DS(ON)}} + 2 \times I_{OUT1(MAX)} \times I_{OUT2(MAX)}}$$

$$I^2_{OUT1(MAX)} + I^2_{OUT2(MAX)} \le \frac{P_{D(MAX)}}{R_{DS(ON)}}$$

$I^2_{OUT1(MAX)} + I^2_{OUT2(MAX)} \le 71$ .....V_{DD}=5V, T_A=25°C

$I^2_{OUT1(MAX)} + I^2_{OUT2(MAX)} \le 59$ .....V_{DD}=3.3V, T_A=25°C

It is noted that the maximum continuous output current (I_{OUT1} or I_{OUT2}) is 6A. Exceeding the maximum continuous output current may cause permanent damage to the device.

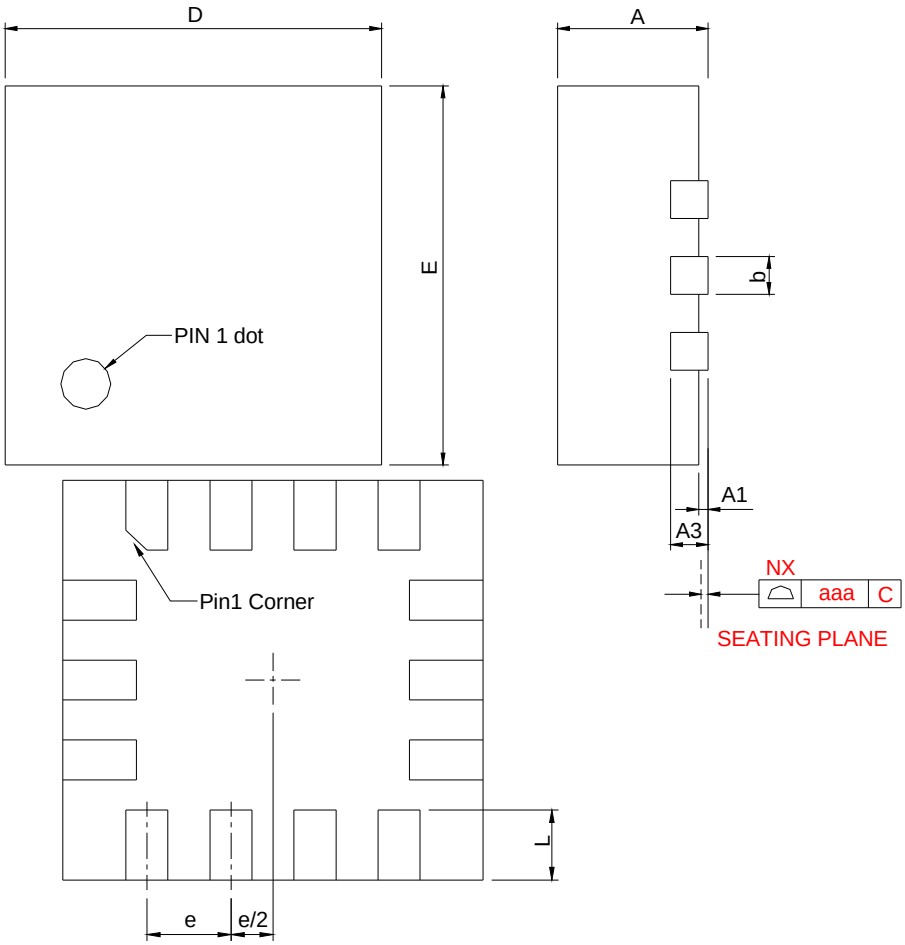
Layout Consideration

The PCB layout should be carefully performed to maximize
thermal dissipation and to minimize voltage drop, droop and EMI. The following guidelines must be considered:

1. Please place the input capacitors near the VINx pin as close as possible.
2. Output decoupling capacitors for load must be placed near the load as close as possible for decoupling high frequency ripples.
3. Locate APL3538 and output capacitors near the load to reduce parasitic resistance and inductance for excellent load transient performance.
4. The negative pins of the input and output capacitors and the GND pin must be connected to the ground plane of the load.
5. Keep VINx and VOUTx traces as wide and short as possible.

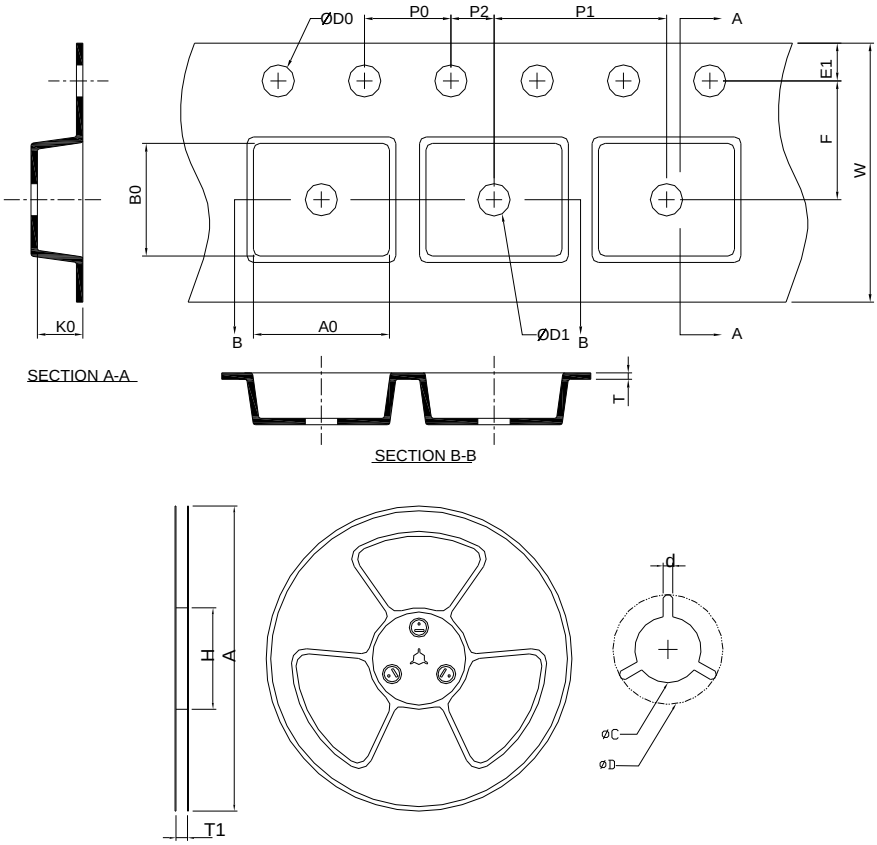
Package Information

TQFN2x2-14



SYMBOL	TQFN2*2-14			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.15	0.25	0.006	0.010
D	1.90	2.10	0.075	0.083
E	1.90	2.10	0.075	0.083
e	0.40 BSC		0.016 BSC	
L	0.27	0.43	0.011	0.017
aaa	0.08		0.003	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFN2x2	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.20	1.75±0.10	3.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	2.35±0.20	2.35±0.20	1.00±0.20

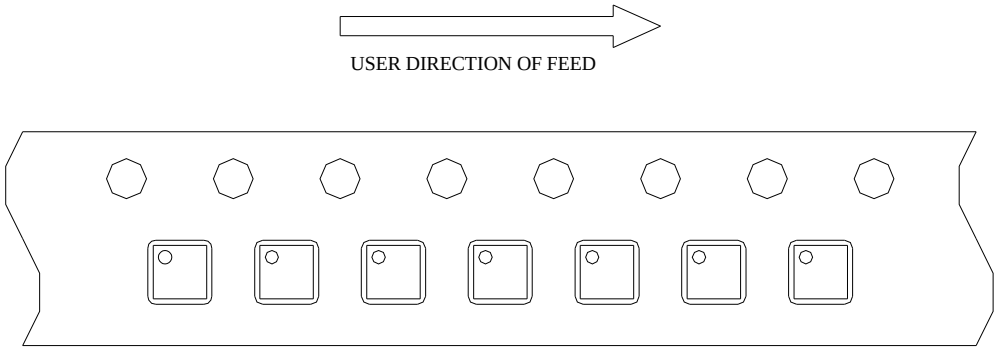
(mm)

Devices Per Unit

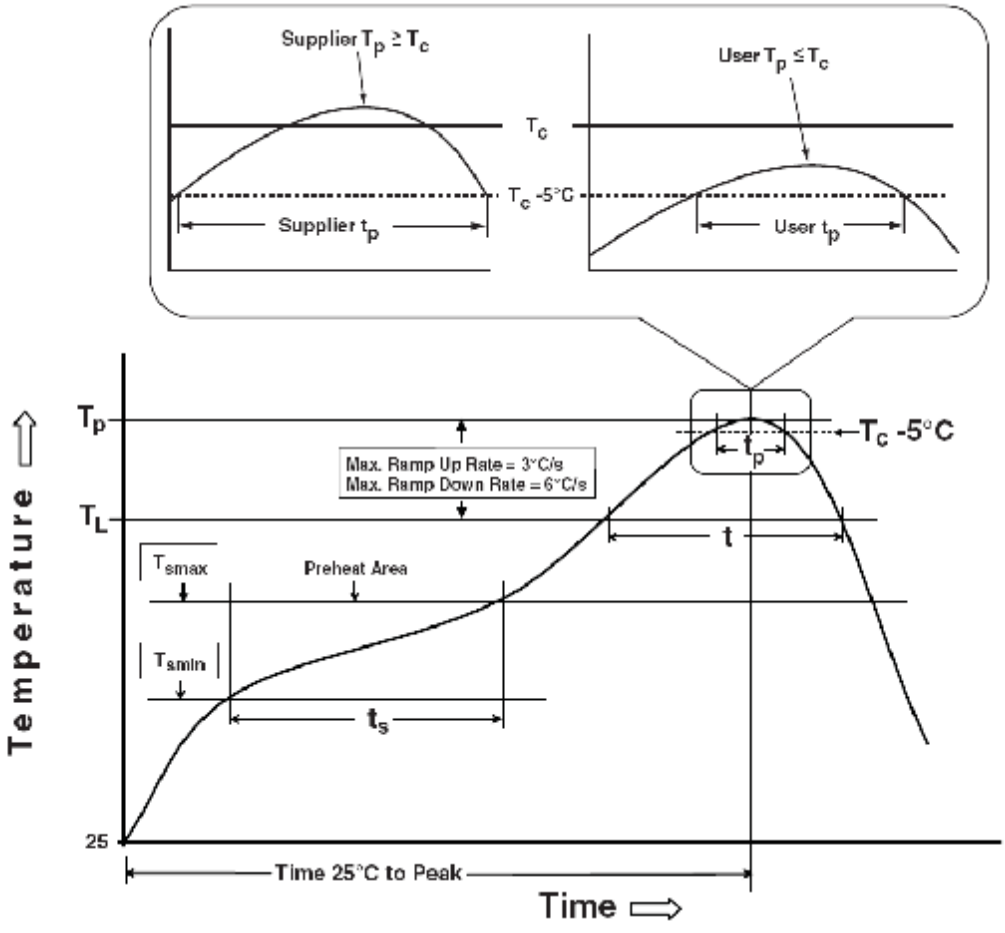
Package Type	Unit	Quantity
TQFN2x2	Tape & Reel	3000

Taping Direction Information

TQFN2x2



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ Tj=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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