# 6A, 24V High-Side Power Distribution Switch with Softstart

## Features

- **Internal 40mΩ High-Side N-Channel MOSFET**
- **Under-Voltage Lockout (UVLO)**
- **Wrong VIN Input Voltage Protection**
- **Short-Circuit Protection During Power-up (SCP)**
- **Adjustable OCP Threshold**
- **Adjustable Softstart Time**
- **Selectable VIN Monitor Voltage**
- **Shutdown Function**
- **Power Good Output**
- **Available in SOP-8P and TDFN3x3-10 Packages**
- **Lead Free and Green Devices Available (RoHS Compliant)**

## Applications

- **LCD TV**
- **LCD Monitor**

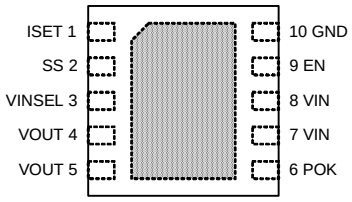
## General Description

APL3548 is a high-side power distribution switch, allow for +12V, +19V or +9.5V power-supply rail. The wrong input voltage protection function protects a wrong input of adapter insertion, when input voltage is out of the target input voltage range the IC is off.

The APL3548 provides a short-circuit protection during power-up. When a short circuit is present before soft start, the IC will limit the output current at 300mA during dead short condition ($V_{OUT}$<1V) unless the short circuit has been removed and the output voltage has risen above 1V. After power-up the OCP function prevents the IC from catastrophic failure from over-load and short circuit conditions. If an OC event is detected, the IC immediately shuts down the internal power switch and will initiate a new soft start cycle. The OCP tripping threshold is set by the external resistor on OCSET pin.

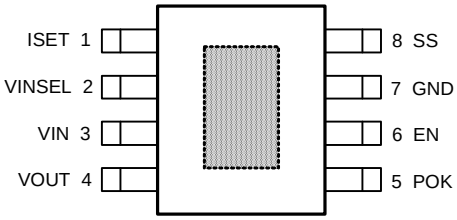
Other features include an adjustable soft start time and a logic-controlled shutdown mode. The device is available in SOP-8P and TDFN3x3-10 Packages.

## Pin Configuration




**TDFN3x3-10**
**Top View**

= Exposed Pad
(connected to ground plane for better heat dissipation)




**SOP-8P**
**Top View**

= Exposed Pad
(connected to ground plane for better heat dissipation)

## Ordering and Marking Information

| | |
|---|---|
| APL3548 □□-□□□<br>Assembly Material<br>Handling Code<br>Temperature Range<br>Package Code | Package Code<br>KA : SOP-8P QB : TDFN3x3-10<br>Operating Ambient Temperature Range<br>I : -40 to 85 °C<br>Handling Code<br>TR : Tape & Reel<br>Assembly Material<br>G : Halogen and Lead Free Device |
| APL3548 KA :  | XXXXX - Date Code |
| APL3548 QB :  | XXXXX - Date Code |

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

## Absolute Maximum Ratings (Note 1)

| Symbol | Parameter | Rating | Unit |
|---|---|---|---|
| $V_{IN}$ | VIN Input Voltage (VIN to GND) | -0.3 to 27 | V |
| $V_{EN}$ , $V_{VINSEL}$ | EN, VINSEL to GND Voltage | -0.3 to 27 | V |
| $V_{POK}$ , $V_{OCSET}$, $V_{SS}$ | POK, OCSET, SS to GND Voltage | -0.3 to 7 | V |
| $T_J$ | Maximum Junction Temperature | 150 | °C |
| $T_{STG}$ | Storage Temperature | -65 to 150 | °C |
| $T_{SDR}$ | Maximum Lead Soldering Temperature (10 Seconds) | 260 | °C |

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Thermal Characteristics

| Symbol | Parameter | | Typical Value | Unit |
|---|---|---|---|---|
| $\theta_{JA}$ | Junction-to-Ambient Resistance | SOP-8P | 50 | °C/W |
| | | TDFN3x3-10 | 60 | °C/W |
| $\theta_{JC}$ | Junction-to-Case Resistance | SOP-8P | 7 | °C/W |
| | | TDFN3x3-10 | 8 | °C/W |

Note 2: $\theta_{JA}$ is measured with the component mounted on a high effective thermal conductivity test board in free air.

## Recommended Operating Conditions

| Symbol | Parameter | | Range | Unit |
|---|---|---|---|---|
| $V_{IN}$ | VIN Input Voltage (VIN to GND) | | 4.5 to 24 | V |
| $V_{EN}$ , $V_{VINSEL}$ | EN, VINSEL to GND Voltage | | 4.5 to 24 | V |
| $C_{SS\_MIN}$ | Minimum Soft-Start Capacitor | Internal Soft-Soft Time | OPEN | nF |
| | | Adjustable Soft-Start Time, $V_{IN}$=4.5~6V | 3.3 | |
| | | Adjustable Soft-Start Time, $V_{IN}$> 6V | 2.2 | |
| $I_{OUT}$ | $V_{OUT}$ Maximum Pulse Current < 10us | | 6 | A |
| | $V_{OUT}$ Maximum Continuous Current | $T_A \leqq 50^oC$ | 5 | A |
| $T_A$ | Ambient Temperature | | -40 to 85 | °C |
| $T_J$ | Junction Temperature | | -40 to 125 | °C |

Note 3: Refer to the typical application circuit

## Electrical Characteristics

Unless otherwise specified, these specifications apply over $V_{IN}$=19V, $V_{EN}$ =5V and $T_A$= -40 to 85 °C. Typical values are at $T_A$=25°C.

| Symbol | Parameter | Test Conditions | | APL3548 | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| **UNDER-VOLTAGE LOCKOUT (UVLO) AND SUPPLY CURRENT** | | | | | | | |
| $V_{UVLO\_R}$ | VIN UVLO Threshold Voltage | $V_{IN}$ rising | | 3.3 | - | 4.2 | V |
| $V_{UVLO\_HYS}$ | VIN UVLO Hysteresis | | | - | 0.35 | - | V |
| $T_{D(ON)}$ | Power-On Delay Time | $V_{IN}$ >$V_{UVLO}$, $V_{EN}$=5V, and $V_{VINSEL(H)}$>$V_{VINSEL}$> $V_{VINSEL(L)}$ | | - | 10 | - | ms |
| $I_{VIN}$ | VIN Supply Current | No load, $V_{EN}$ =5V | | - | 250 | 400 | µA |
| | | No load, $V_{EN}$ =0V | | - | 10 | 50 | µA |
| **POWER MOSFET** | | | | | | | |
| | Power MOSFET On Resistance | $T_J$= 25 °C. | SOP-8P | - | 44 | 50 | mΩ |
| | | | TDFN3x3-10 | - | 40 | 48 | mΩ |
| **WRONG VIN INPUT VOLTAGE PROTECTION** | | | | | | | |
| $V_{VINSEL(L)}$ | VINSEL Low Detection Rising Threshold | $V_{VINSEL}$ rising, IC is on, $V_{IN}$=4.5V to 24V | | 1.296 | 1.350 | 1.404 | V |
| | VINSEL Low Detection Falling Threshold | $V_{VINSEL}$ falling, IC is off, $V_{IN}$=4.5V to 24V | | 1.152 | 1.200 | 1.248 | mV |
| $V_{VINSEL(H)}$ | VINSEL High Detection Rising Threshold | $V_{VINSEL}$ rising, IC is off, $V_{IN}$=4.5V to 24V | | 1.728 | 1.800 | 1.872 | V |
| | VINSEL High Detection Falling Threshold | $V_{VINSEL}$ falling, IC is on, $V_{IN}$=4.5V to 24V | | 1.584 | 1.650 | 1.716 | mV |
| | VINSEL Detection Disable Threshold | $V_{VINSEL}$ falling, VINSEL detection function is disabled. $V_{IN}$=4.5V to 24V | | 0.15 | 0.2 | 0.25 | V |
| | VINSEL Detection Disable Threshold Hysteresis | $V_{VINSEL}$ rising, VINSEL detection function is eabled. $V_{IN}$=4.5V to 24V | | - | 100 | - | mV |
| | VINSEL Input Current | $V_{VINSEL}$=24V | | - | - | 1 | µA |
| | VINSEL Low Detection Debounce | $V_{VINSEL}$ falling, $V_{VINSEL}$ < $V_{VINSEL(L)}$ (Note 4) | | - | 10 | - | µs |
| | VINSEL High Detection Debounce | $V_{VINSEL}$ rising, $V_{VINSEL}$ > $V_{VINSEL(H)}$ (Note 4) | | - | 10 | - | µs |

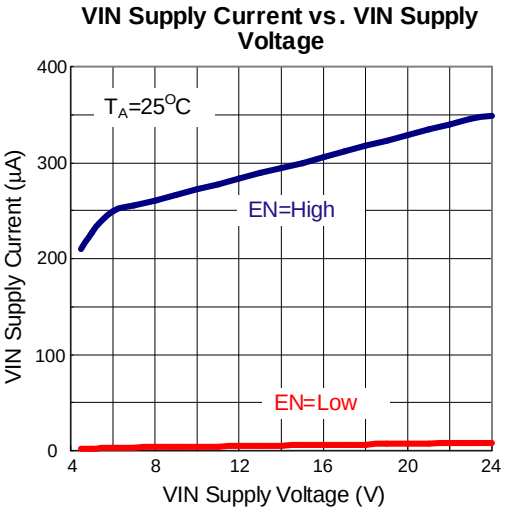
## Electrical Characteristics (Cont.)

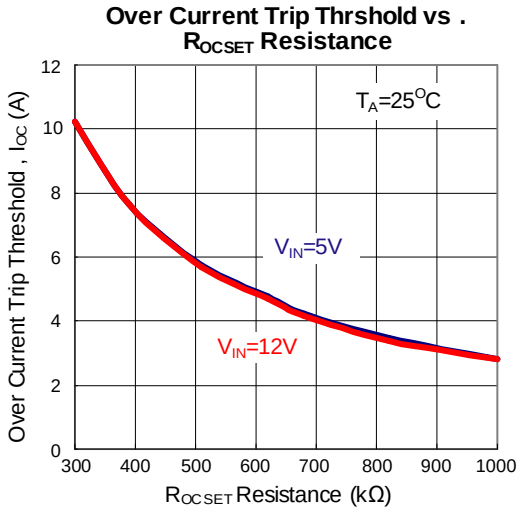
Unless otherwise specified, these specifications apply over $V_{IN}$=19V, $V_{EN}$ =5V and $T_A$= -40 to 85 °C. Typical values are at $T_A$=25°C.

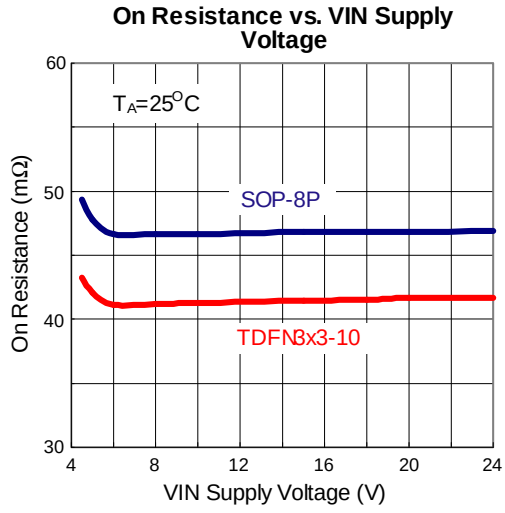
| Symbol | Parameter | Test Conditions | APL3548 | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| **CHARGE PUMP AND SOFTSTART AND DISCHARGE** | | | | | | |
| | Internal 5V Voltage | | - | 5.3 | - | V |
| | SS Pin Output Current | $V_{IN}$=4.5~24V, SS=GND | - | 2 | - | µA |
| | Internal Soft-Soft Time | $V_{IN}$=19V | | 2.4 | | ms |
| | SS Pin Discharge Resistance | $V_{IN}$=4.5~24V, EN=GND, SS=1V | - | 2 | - | kΩ |
| | VOUT Discharge Resistance | $V_{IN}$=19V, EN=GND, VOUT=1V | - | 75 | - | Ω |
| **PROTECTIONS** | | | | | | |
| | Pre-Charge Current | $V_{IN}$=12V | - | 200 | - | mA |
| | OCSET Output Voltage | | - | 0.6 | - | V |
| | Over Current Tripping Point | $R_{OCSET}$=1MΩ | - | 2.8 | - | A |
| | | $R_{OCSET}$=390kΩ | - | 7.7 | - | A |
| | Over Temperature Protection | (Note 4) | - | 140 | - | °C |
| | Over Temperature Protection Hysteresis | (Note 4) | - | 50 | - | °C |
| **EN INPUT** | | | | | | |
| $V_{EN\_TH}$ | EN Logic Input Threshold | | 0.9 | 1.25 | 1.6 | V |
| | EN Input Logic Hysteresis | | - | 0.2 | - | V |
| | EN Pull-up Current | | - | 1 | - | µA |
| **POK OUTPUT** | | | | | | |
| $V_{POK}$ | Rising POK Threshold Voltage | $V_{OUT}$ rising, $V_{OUT}/V_{IN}$, $V_{POK}$=High | 85 | 90 | 95 | % $V_{IN}$ |
| | POK Threshold Hysteresis | $V_{OUT}$ falling, $V_{POK}$=Low | - | 5 | - | % $V_{IN}$ |
| | POK Low Voltage | $I_{POK}$=10mA | - | - | 0.5 | V |
| | POK Leakage Current | $V_{POK}$=5V | - | - | 1 | µA |
| $t_{D(POK)}$ | POK Rising Delay Time | $V_{OUT}$ rising, POK assertion | 1 | 2 | 3 | ms |
| | POK Falling Debounce Time | $V_{OUT}$ falling (Note 4) | - | 10 | - | µs |

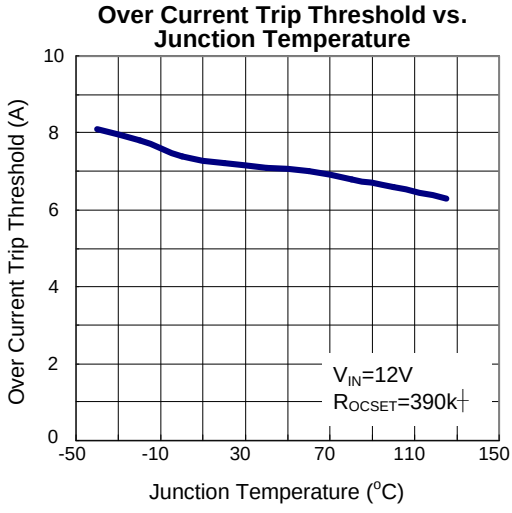
Note 4: Guarantee by design, not production test.

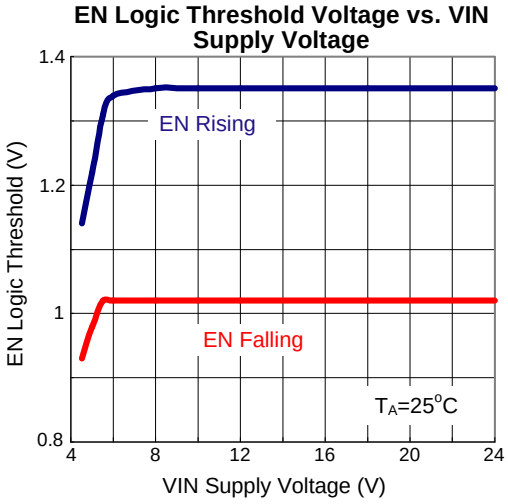
## Typical Operating Characteristics

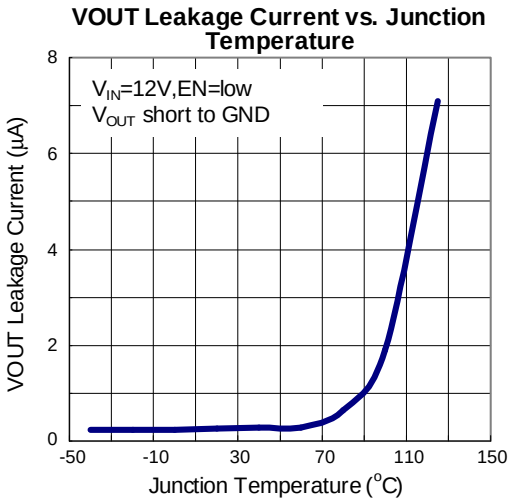


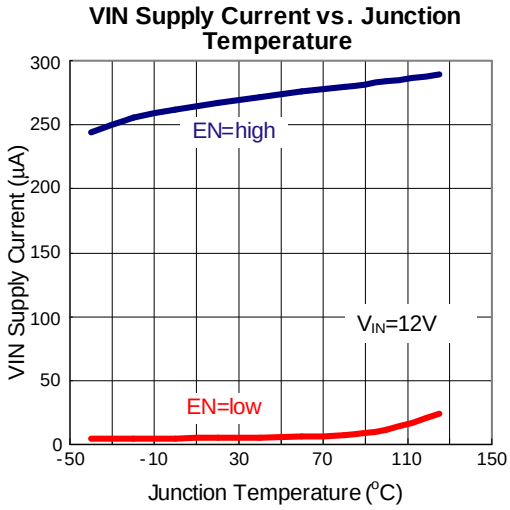



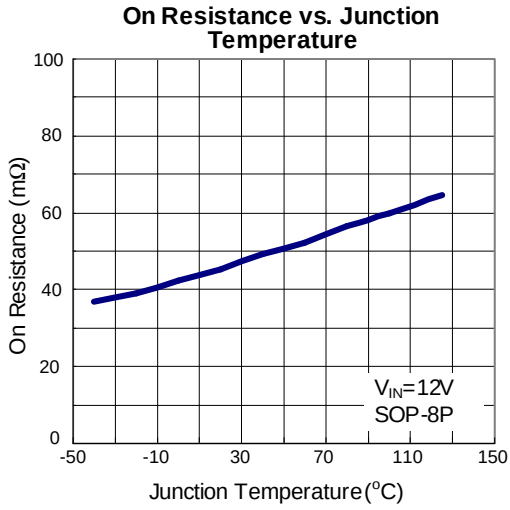



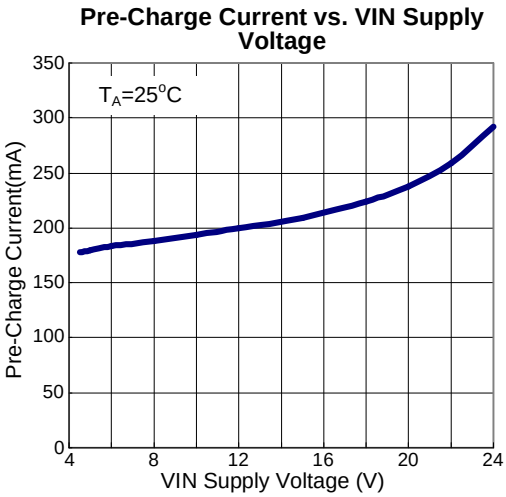



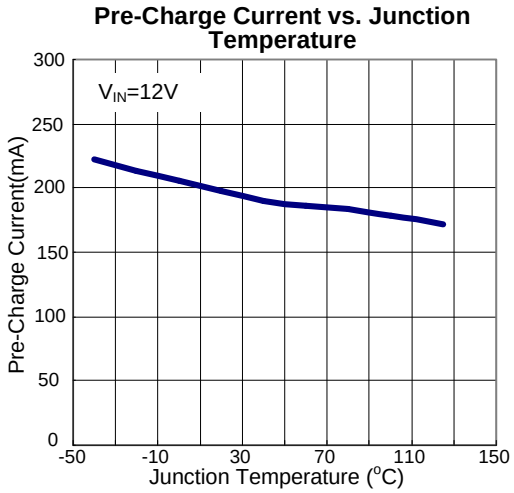



## Typical Operating Characteristics (Cont.)



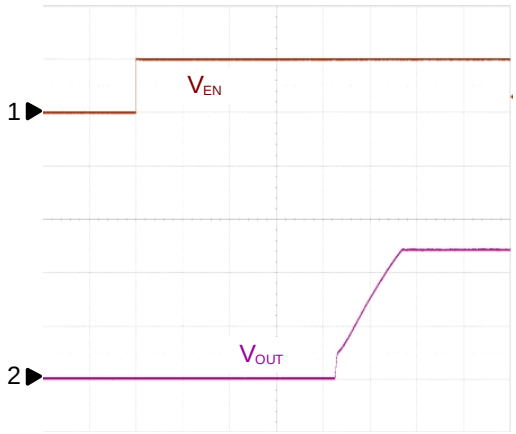



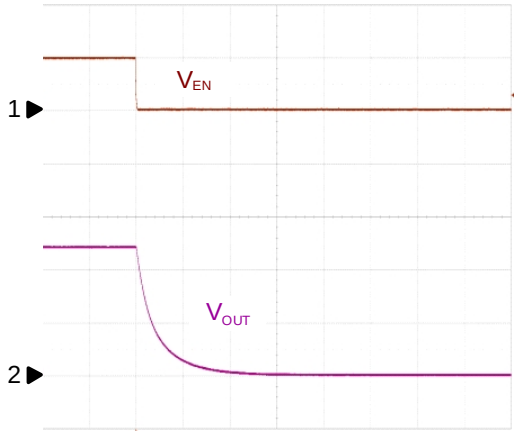
## Operating Waveforms

### Turn On Response



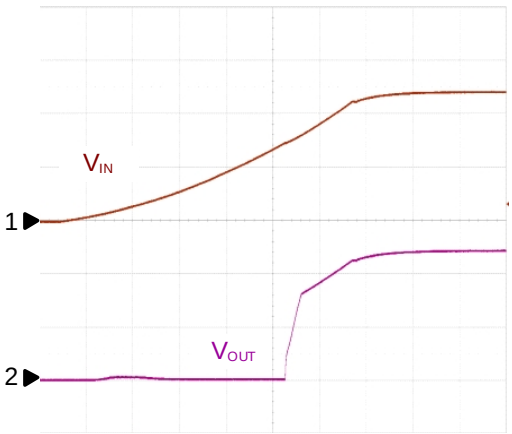

$V_{IN}$=12V,$C_{OUT}$=10µF/MLCC,$C_{IN}$=10µF/MLCC
No $R_{LOAD}$,$C_{SS}$=4.7nF
CH1:$V_{EN}$,5V/Div, DC
CH2:$V_{OUT}$,5V/Div, DC
TIME:2ms/Div

### Turn Off Response



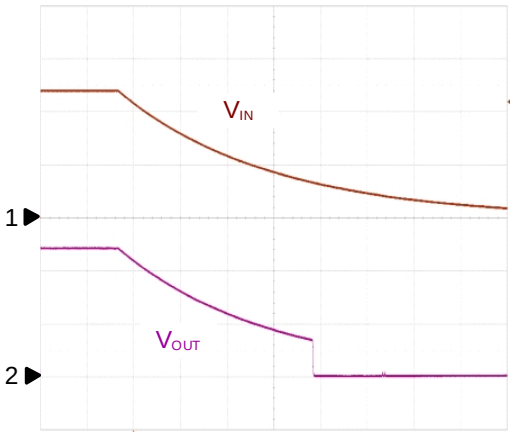

$V_{IN}$=12V,$C_{OUT}$=10µF/MLCC,$C_{IN}$=10µF/MLCC
No $R_{LOAD}$,$C_{SS}$=4.7nF
CH1:$V_{EN}$,5V/Div, DC
CH2:$V_{OUT}$,5V/Div, DC
TIME:2ms/Div

### UVLO at Rising




$V_{IN}$=12V,$C_{OUT}$=10µF/MLCC,$C_{IN}$=10µF/MLCC
No $R_{LOAD}$,$C_{SS}$=4.7nF
CH1:$V_{IN}$,5V/Div, DC
CH2:$V_{OUT}$,5V/Div, DC
TIME:5ms/Div

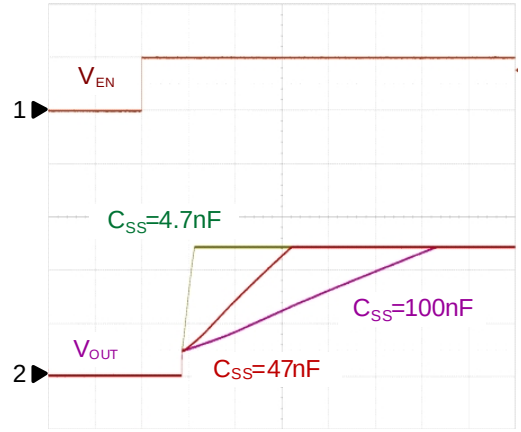
### UVLO at Falling




$V_{IN}$=12V,$C_{OUT}$=10µF/MLCC,$C_{IN}$=10µF/MLCC
No $R_{LOAD}$,$C_{SS}$=4.7nF
CH1:$V_{IN}$,5V/Div, DC
CH2:$V_{OUT}$,5V/Div, DC
TIME:200ms/Div

## Operating Waveforms (Cont.)

### Softstart with Different $C_{SS}$ Capacitor

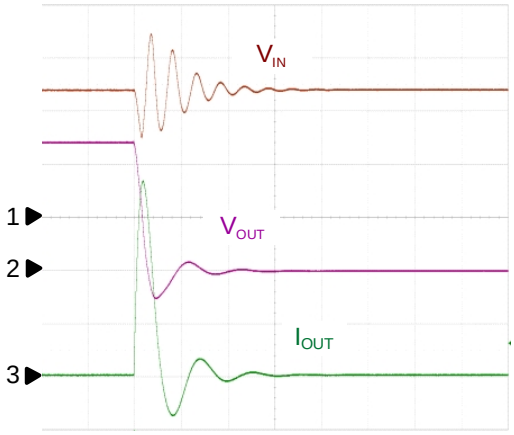



$V_{IN}$=12V,$C_{OUT}$=10µF/MLCC,$C_{IN}$=10µF/MLCC
No $R_{LOAD}$,$C_{SS}$=4.7/47/100nF
CH1:$V_{EN}$,5V/Div, DC
CH2:$V_{OUT}$,5V/Div, DC
TIME:5ms/Div

### Over Current Response with Ramped Load

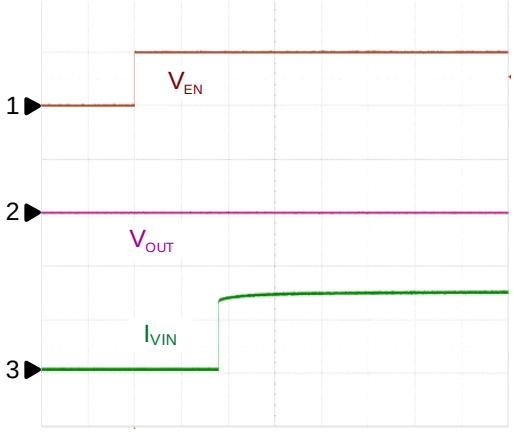

$V_{IN}$=12V,$C_{OUT}$=10µF/MLCC,$C_{IN}$=10µF/MLCC
No $R_{LOAD}$,$C_{SS}$=47nF,$R_{OCSET}$=390kΩ
CH1:$V_{OUT}$,5V/Div, DC
CH2:$I_{OUT}$,2A/Div, DC
TIME:100µs/Div

### Short Circuit Response




$V_{IN}$=12V,$C_{OUT}$=10µF/MLCC,$C_{IN}$=10µF/MLCC
$C_{SS}$=47nF,$R_{OCSET}$=390kΩ,$V_{OUT}$ short to ground
CH1:$V_{IN}$,5V/Div, DC
CH2:$V_{OUT}$,5V/Div, DC
CH3:$I_{OUT}$,10A/Div, DC
TIME:10µs/Div

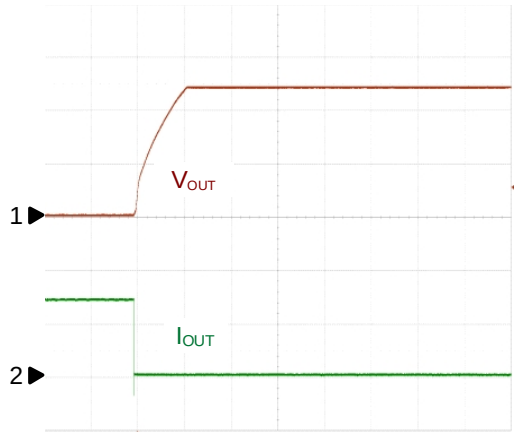
### Device Enabled into Short Circuit




$V_{IN}$=12V,$C_{OUT}$=10µF/MLCC,$C_{IN}$=10µF/MLCC
$C_{SS}$=47nF,$R_{OCSET}$=390kΩ
$V_{OUT}$ short to ground then EN power on
CH1:$V_{EN}$,5V/Div, DC
CH2:$V_{OUT}$,5V/Div, DC
CH3:$I_{VIN}$,100mA/Div, DC
TIME:5ms/Div

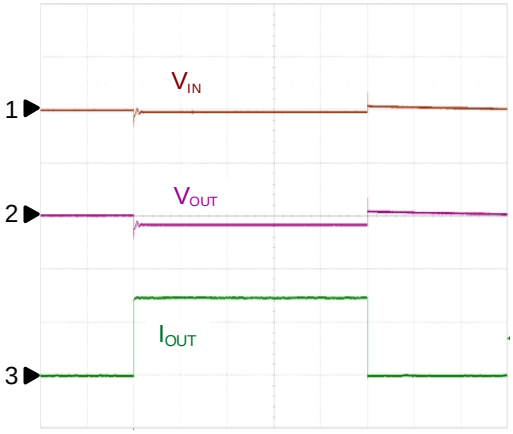
## Operating Waveforms (Cont.)

### Short Circuit Release




$V_{IN}$=12V,$C_{OUT}$=10µF/MLCC,$C_{IN}$=10µF/MLCC
$C_{SS}$=47nF,$R_{OCSET}$=390kΩ,No Load
CH1:$V_{OUT}$,5V/Div, DC
CH2:$I_{OUT}$,100mA/Div, DC
TIME:1ms/Div

### Load Transient

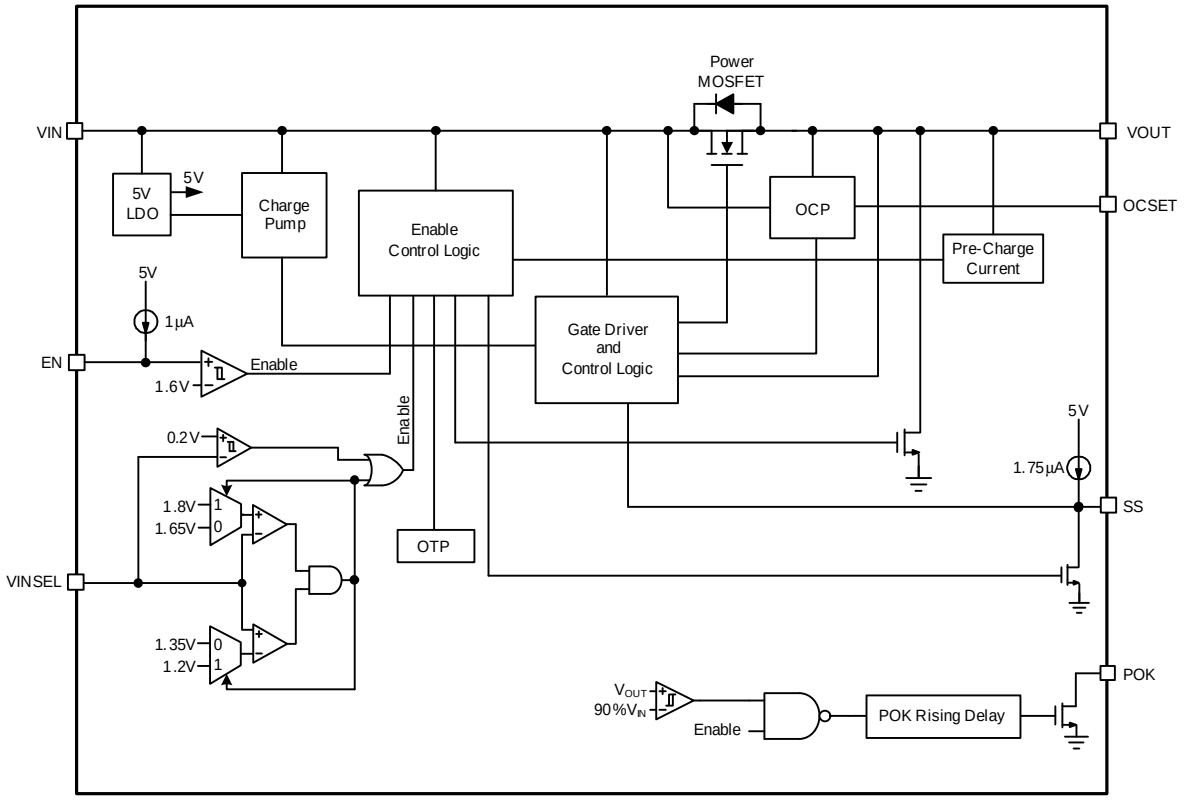



$V_{IN}$=12V,$C_{OUT}$=10µF/MLCC,$C_{IN}$=10µF/MLCC
$C_{SS}$=47nF,$R_{OCSET}$=390kΩ,$I_{OUT}$=0-3-0A
CH1:$V_{IN}$,1V/Div, Offset=12V
CH2:$V_{OUT}$,1V/Div, Offset=12V
CH3:$I_{OUT}$,2A/Div, DC
TIME:1ms/Div

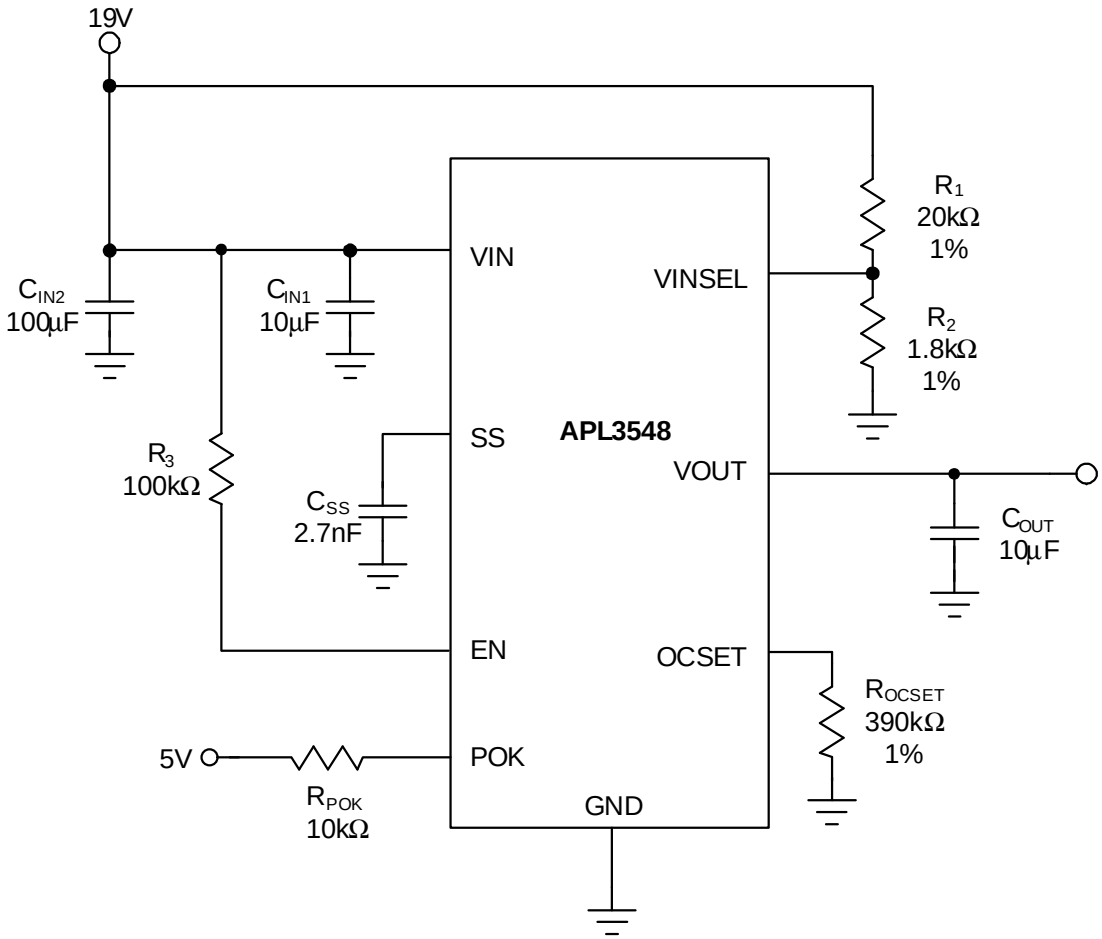
## Pin Description

| PIN | | | FUNCTION |
|---|---|---|---|
| NO. | | NAME | |
| SOP-8P | TDFN3x3-10 | | |
| 1 | 1 | OCSET | Over-Current Trip Point Adjustment Pin. A resistor ($R_{OCSET}$) from this pin to ground sets the over current tripping point threshold. |
| 2 | 3 | VINSEL | Input Voltage Sense Pin. Connect a resistive divider from VIN to VINSEL to GND to monitor the input voltage. Pulling $V_{VINSEL}$ below 0.3V will disable this function. |
| 3 | 7,8 | VIN | Power Input Pin. Provide power to the internal circuitry and also connect to the internal power MOSFET' s Drain terminal. When the Power MOSFET is turned on, VIN provides power to VOUT. |
| 4 | 4,5 | VOUT | Power Output Pin. This pin is internally connected to the internal power MOSFET' s source terminal. When the Power MOSFET is turned on, the VOUT can draw power from VIN. Current can flow from VOUT to VIN too. |
| 5 | 6 | POK | Power Okay Indicator Output. The POK is an open-drain pull-down device. When VOUT voltage falls and reaches the falling Power-OK voltage threshold, the POK output is pulled low; when VOUT voltage rises and reaches the rising Power-OK voltage threshold, the POK output is in high impedance. |
| 6 | 9 | EN | Enable Input. Pulling the $V_{EN}$ above 2V will enable the IC; pulling $V_{EN}$ below 0.6V will disable the IC. This pin is pulled high by an internal current source. |
| 7 | 10 | GND | Ground pin. |
| 8 | 2 | SS | VOUT Rising Slew Rate Control. A capacitor from this pin to ground sets a VOUT rising slew rate. |

## Block Diagram



## Typical Application Circuit



## Function Description

### Under-voltage Lockout (UVLO)

The APL3548 power switch is built-in an under-voltage lockout circuit to keep the output shut off until internal circuitry is operating properly. The UVLO circuit has hysteresis and a de-glitch feature so that it will typically ignore undershoot transients on the input. When input voltage exceeds the UVLO threshold, the output voltage starts a soft-start to reduce the inrush current.

### Power Switch

The power switch is an N-channel MOSFET with a low $R_{DS(ON)}$. When IC is off, the MOSFET prevents a current flowing from VIN to VOUT. Once the MOSFET is turned on, the current is by-directional. Note that the MOSFET possesses a body diode which allows the current to flow through it in shutdown and body diode forward-biased condition, $V_{OUT}$-$V_{IN}$>0.3V.

### Over Current Protection

The APL3548 power switch provides the over current protection function. The OCP threshold is set by the resistance from OCSET pin to ground. The OCP threshold equation is as below:

$I_{OCP}(A)=2800/R_{OCSET}(k\Omega)+0.7$

When the OCP threshold is tripped, the IC immediately turns off its power switch and thus prevents over current flowing from VIN to VOUT. In output dead short condition, an internal 200mA current source provides the power to VOUT. If the short circuit condition persists, so as the 200mA current source. Only when OTP shutdown or dead short removal the 200mA is turned off.

### Wrong VIN Input Voltage Protection

The APL3548 provides an input voltage detection function to protect a wrong input adapter insertion. Connect a resistive divider from VIN to VINSEL to GND to set the target input voltage. The target input voltage is set at:
$V_{IN(target)}$=1.5V x (1+R1/R2)
The IC is enabled When input voltage is within the $V_{IN(target)}$ +15% ($V_{IN}$ also must be above $V_{UVLO}$ and EN is high); the device is shut down when input voltage is outside the VIN (target)+20%.

### Enable/Shutdown Control

The APL3548 has an active-high enable function. Pulling the $V_{EN}$ above 2V will enable the IC; pulling $V_{EN}$ below 0.6V will disable the IC and the POK is pulled low immediately (ignore the $V_{POK(TH)}$ and $T_{D(POK)}$), the $V_{OUT}$ voltage is also discharged to GND by an internal resistor . EN pin is pulled high by an internal current source and can be left floating.

### Soft-Start

The APLA3548 provides an adjustable soft-start circuitry to control rise rate of the output voltage and limit the current surge during start-up. The soft-start ramp-up rate is controlled by a capacitor from SS pin to the ground.
Under a specific $V_{IN}$ being applied to the APL3548, the soft start time can be calculated by the following equation:

$t_{SS}=C_{SS}$ x ($V_{IN}$-1.5)/$I_{SS}$ x 10

where,
$t_{SS}$ is soft-start time of $V_{OUT}$ rising from 0 to 100%, of which unit is second.
$C_{SS}$ is the value of the capacitor connected from SS pin to GND, of which unit is micro-Farad.
$V_{IN}$ is the amplitude of input voltage applied to this device, of which unit is volt. $I_{SS}$ is typically 1.75μA.

### POK Output

The power okay function monitors the output voltage and drives the POK low to indicate a fault. When a fault condition such as over temperature, or wrong VIN input voltage is occurred, or over-current and the VOUT output voltage falls to 85% of the VIN input voltage, the POK is pulled low. When the VOUT output voltage reaches to 90% of VIN input voltage, and after POK rising delay time, the POK is pulled high. Since the POK is an open-drain device, connecting a resistor to a pull high voltage is necessary.

## Function Description (Cont.)

### Over-Temperature Protection

When the junction temperature exceeds 140°C, the internal thermal sense circuit turns off the power FET and allows the device to cool down. When the device's junction temperature cools by 20°C, the internal thermal sense circuit will enable the device, resulting in a pulsed output during continuous thermal protection. Thermal protection is designed to protect the IC in the event of over-temperature conditions. For normal operation, the junction temperature cannot exceed $T_J$=125°C.

## Application Information

### Input Capacitor

A 10µF or higher ceramic bypass capacitor from VIN to GND, located near the APL3548, is strongly recommended to suppress the ringing during short circuit fault event. When the load current trips the OCP threshold in an over load condition such as a short circuit, hot plug-in or heavy load transient the IC immediately turns off the internal power switch that will cause $V_{IN}$ ringing due to the parasitical inductance between power source and $V_{IN}$. Without the bypass capacitor, the output short may cause sufficient ringing on the input to damage internal control circuitry. Input capacitor is especially important to prevent $V_{IN}$ from ringing too high in some applications where the inductance between power source to VIN is large (ex, an extra bead is added between power source line to VIN for EMI reduction) or applications where $V_{IN}$ voltage is 19V or so which is near its maximum rating, additional input capacitance may be needed on the input to reduce voltage overshoot from exceeding the absolute maximum voltage of the device during over load conditions.

### Output Capacitor

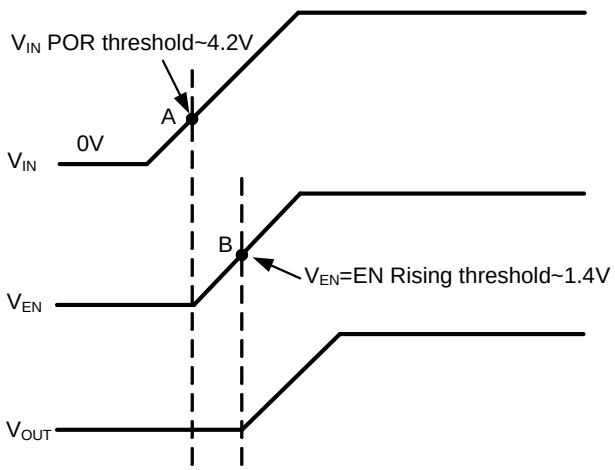
A low-ESR 10µF between $V_{OUT}$ and GND is strongly recommended to reduce the voltage droop during hot-attachment of downstream peripheral.
Higher-value output capacitor is better when the output load is heavy. Additionally, bypassing the output with a 0.1µF ceramic capacitor improves the immunity of the device to short-circuit transients.

### Layout Consideration

The PCB layout should be carefully performed to maximize thermal dissipation and to minimize voltage drop, droop and EMI. The following guidelines must be considered:
1. Please place the input capacitors near the VIN pin as close as possible.
2. Output decoupling capacitors for load must be placed near the load as close as possible for decoupling high frequency ripples.
3. Locate APL3548 and output capacitors near the load to reduce parasitic resistance and inductance for excellent load transient performance.
4. The negative pins of the input and output capacitors and the GND pin must be connected to the ground plane of the load.
5. Keep $V_{IN}$ and $V_{OUT}$ traces as wide and short as possible.

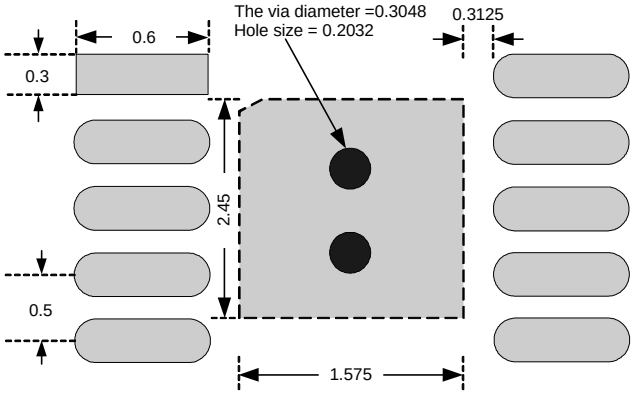
### Power Sequence

The following figure shows the recommended power sequence. $V_{IN}$ must reach POR threshold voltage(Point A) before $V_{EN}$ reaches Rising threshold voltage(Point B).

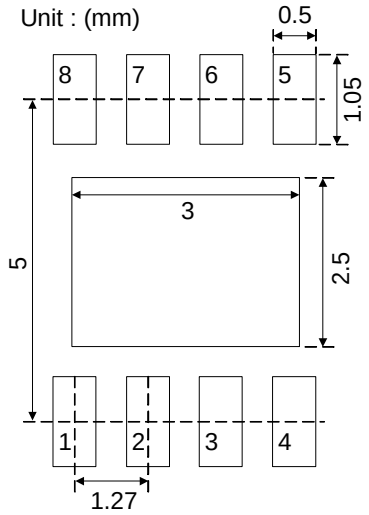


## Application Information

**Recommended Minimum Footprint**



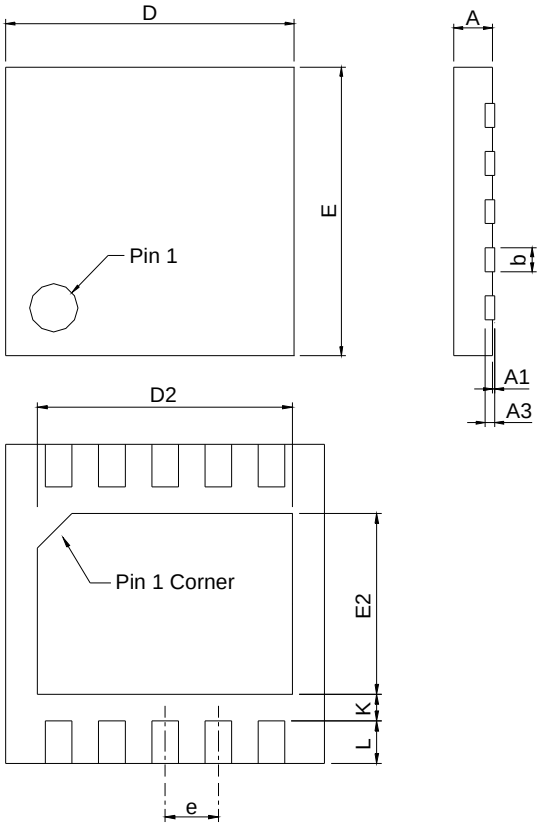

TDFN3x3-10 Unit: mm




SOP-8P

## Package Information

**TDFN3x3-10**

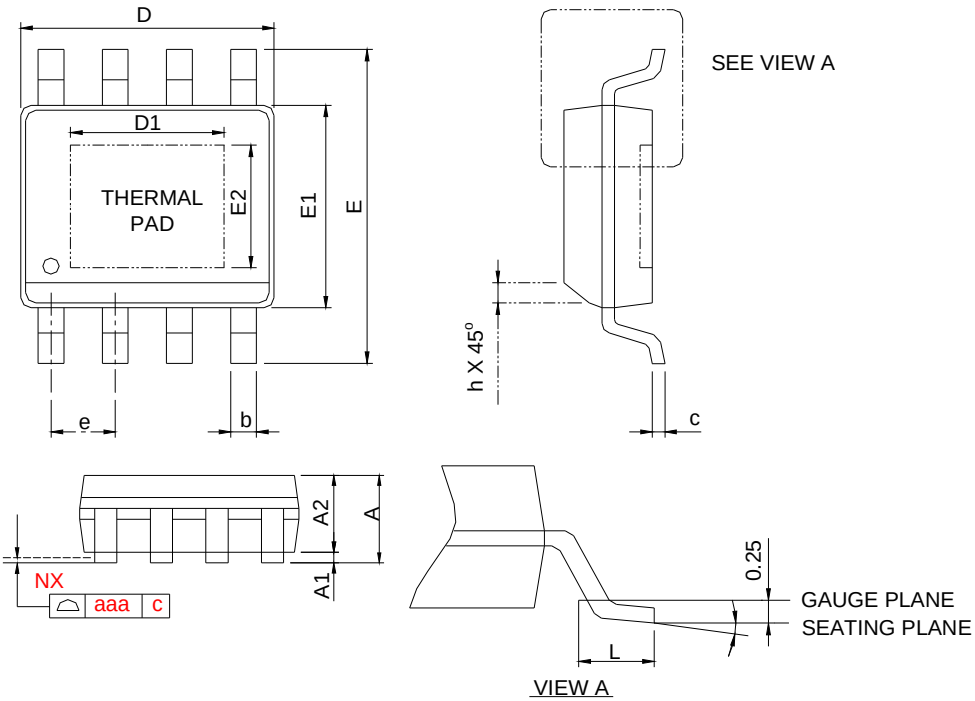



| SYMBOL | TDFN3x3-10 | | | |
|---|---|---|---|---|
| | MILLIMETERS | | INCHES | |
| | MIN. | MAX. | MIN. | MAX. |
| A | 0.70 | 0.80 | 0.028 | 0.031 |
| A1 | 0.00 | 0.05 | 0.000 | 0.002 |
| A3 | 0.20 REF | | 0.008 REF | |
| b | 0.18 | 0.30 | 0.007 | 0.012 |
| D | 2.90 | 3.10 | 0.114 | 0.122 |
| D2 | 2.20 | 2.70 | 0.087 | 0.106 |
| E | 2.90 | 3.10 | 0.114 | 0.122 |
| E2 | 1.40 | 1.75 | 0.055 | 0.069 |
| e | 0.50 BSC | | 0.020 BSC | |
| L | 0.30 | 0.50 | 0.012 | 0.020 |
| K | 0.20 | | 0.008 | |

Note : 1. Followed from JEDEC MO-229 VEED-5.

## Package Information

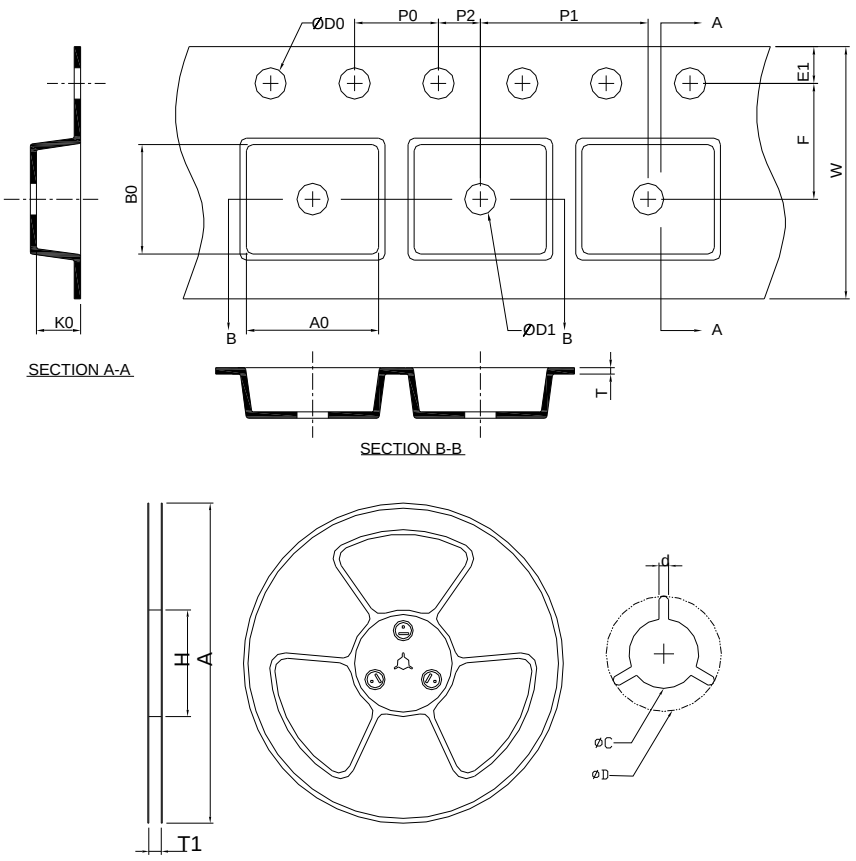
**SOP-8P**




| SYMBOL | SOP-8P | | | |
|---|---|---|---|---|
| | MILLIMETERS | | INCHES | |
| | MIN. | MAX. | MIN. | MAX. |
| A | | 1.60 | | 0.063 |
| A1 | 0.00 | 0.15 | 0.000 | 0.006 |
| A2 | 1.25 | | 0.049 | |
| b | 0.31 | 0.51 | 0.012 | 0.020 |
| c | 0.17 | 0.25 | 0.007 | 0.010 |
| D | 4.80 | 5.00 | 0.189 | 0.197 |
| D1 | 2.50 | 3.50 | 0.098 | 0.138 |
| E | 5.80 | 6.20 | 0.228 | 0.244 |
| E1 | 3.80 | 4.00 | 0.150 | 0.157 |
| E2 | 2.00 | 3.00 | 0.079 | 0.118 |
| e | 1.27 BSC | | 0.050 BSC | |
| h | 0.25 | 0.50 | 0.010 | 0.020 |
| L | 0.40 | 1.27 | 0.016 | 0.050 |
| θ | 0°C | 8°C | 0°C | 8°C |
| aaa | 0.10 | | 0.004 | |

Note : 1. Followed from JEDEC MS-012 BA.
2. Dimension "D" does not include mold flash, protrusions or gate burrs.
Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .
3. Dimension "E" does not include inter-lead flash or protrusions.
Inter-lead flash and protrusions shall not exceed 10 mil per side.

## Carrier Tape & Reel Dimensions




| Application | A | H | T1 | C | d | D | W | E1 | F |
|---|---|---|---|---|---|---|---|---|---|
| TDFN3x3-10 | 330±2.00 | 50 MIN. | 12.4+2.00 -0.00 | 13.0+0.50 -0.20 | 1.5 MIN. | 20.2 MIN. | 12.0±0.30 | 1.75±0.10 | 5.5±0.05 |
| | **P0** | **P1** | **P2** | **D0** | **D1** | **T** | **A0** | **B0** | **K0** |
| | 4.0±0.10 | 8.0±0.10 | 2.0±0.05 | 1.5+0.10 -0.00 | 1.5 MIN. | 0.6+0.00 -0.40 | 3.30±0.20 | 3.30±0.20 | 1.00±0.20 |
| **Application** | **A** | **H** | **T1** | **C** | **d** | **D** | **W** | **E1** | **F** |
| SOP-8P | 330.0±2.00 | 50 MIN. | 12.4+2.00 -0.00 | 13.0+0.50 -0.20 | 1.5 MIN. | 20.2 MIN. | 12.0±0.30 | 1.75±0.10 | 5.5±0.05 |
| | P0 | P1 | P2 | D0 | D1 | T | A0 | B0 | K0 |
| | 4.0±0.10 | 8.0±0.10 | 2.0±0.05 | 1.5+0.10 -0.00 | 1.5 MIN. | 0.6+0.00 -0.40 | 6.55±0.20 | 5.25±0.20 | 2.10±0.20 |

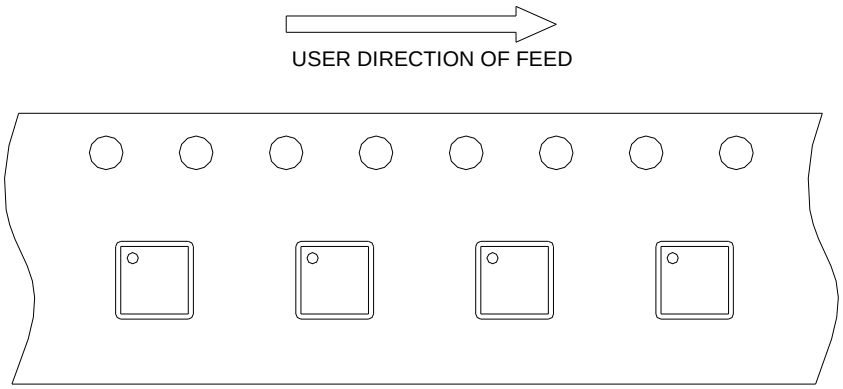
(mm)

## Devices Per Unit

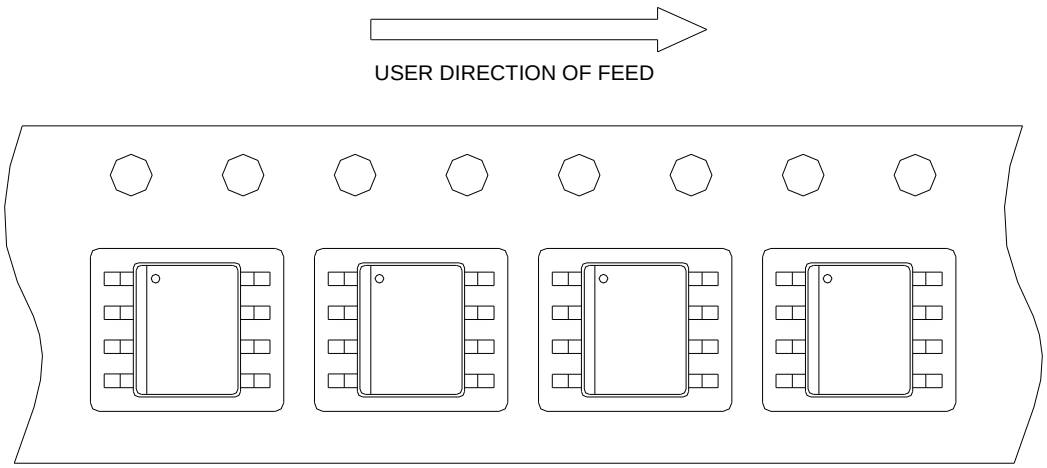
| Package Type | Unit | Quantity |
|---|---|---|
| **TDFN-3x3-10** | Tape & Reel | 3000 |
| **SOP-8P** | Tape & Reel | 2500 |

## Taping Direction Information

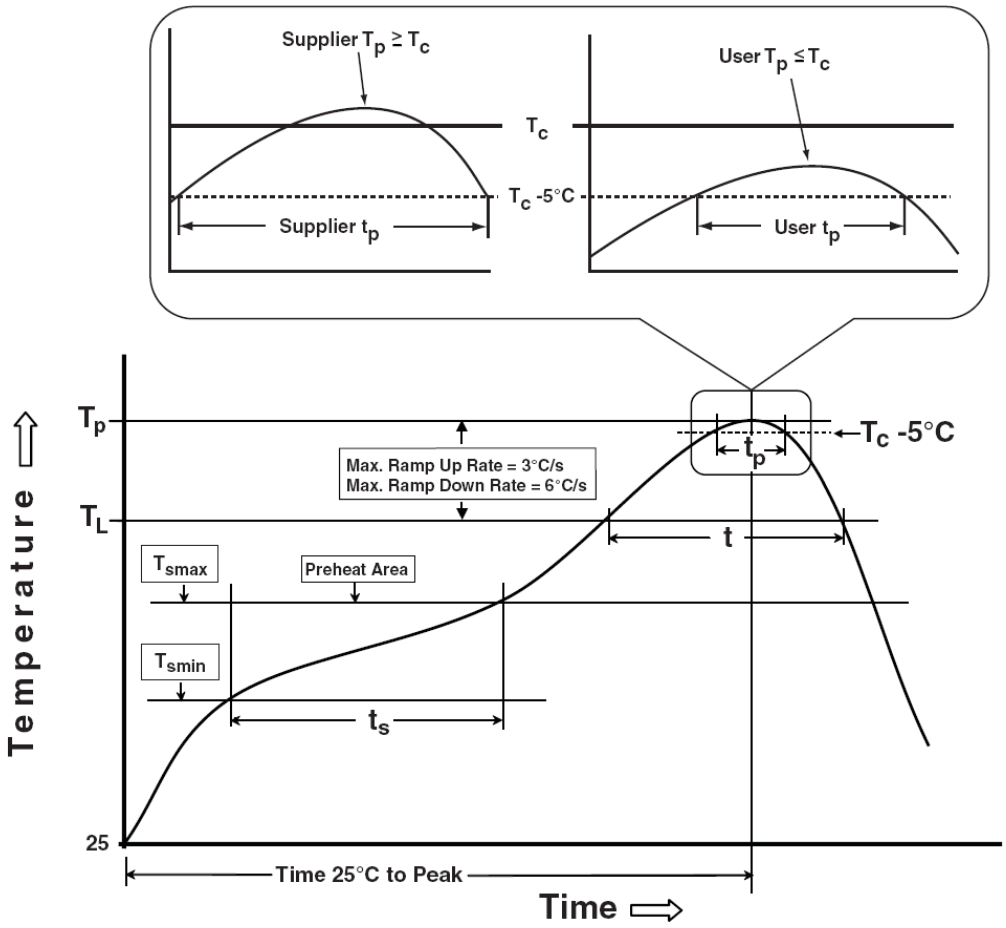
**TDFN3x3-10**




**SOP-8P**



## Classification Profile



## Classification Reflow Profiles

| Profile Feature | Sn-Pb Eutectic Assembly | Pb-Free Assembly |
|---|---|---|
| **Preheat & Soak**<br>Temperature min ($T_{smin}$)<br>Temperature max ($T_{smax}$)<br>Time ($T_{smin}$ to $T_{smax}$) ($t_s$) | <br>100 °C<br>150 °C<br>60-120 seconds | <br>150 °C<br>200 °C<br>60-120 seconds |
| Average ramp-up rate ($T_{smax}$ to $T_P$) | 3 °C/second max. | 3°C/second max. |
| Liquidous temperature ($T_L$)<br>Time at liquidous ($t_L$) | 183 °C<br>60-150 seconds | 217 °C<br>60-150 seconds |
| Peak package body Temperature ($T_p$)* | See Classification Temp in table 1 | See Classification Temp in table 2 |
| Time ($t_P$)** within 5°C of the specified classification temperature ($T_c$) | 20** seconds | 30** seconds |
| Average ramp-down rate ($T_p$ to $T_{smax}$) | 6 °C/second max. | 6 °C/second max. |
| Time 25°C to peak temperature | 6 minutes max. | 8 minutes max. |
| * Tolerance for peak profile Temperature ($T_p$) is defined as a supplier minimum and a user maximum.<br>** Tolerance for time at peak profile temperature ($t_p$) is defined as a supplier minimum and a user maximum. | | |

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

| Package Thickness | Volume $mm^3$ <350 | Volume $mm^3$ 350 |
|---|---|---|
| <2.5 mm | 235 °C | 220 °C |
| ≥2.5 mm | 220 °C | 220 °C |

Table 2. Pb-free Process – Classification Temperatures (Tc)

| Package Thickness | Volume $mm^3$ <350 | Volume $mm^3$ 350-2000 | Volume $mm^3$ >2000 |
|---|---|---|---|
| <1.6 mm | 260 °C | 260 °C | 260 °C |
| 1.6 mm – 2.5 mm | 260 °C | 250 °C | 245 °C |
| ≥2.5 mm | 250 °C | 245 °C | 245 °C |

## Reliability Test Program

| Test item | Method | Description |
|---|---|---|
| SOLDERABILITY | JESD-22, B102 | 5 Sec, 245°C |
| HOLT | JESD-22, A108 | 1000 Hrs, Bias @ $T_j$=125°C |
| PCT | JESD-22, A102 | 168 Hrs, 100%RH, 2atm, 121°C |
| TCT | JESD-22, A104 | 500 Cycles, -65°C~150°C |
| HBM | MIL-STD-883-3015.7 | VHBM≧2KV |
| MM | JESD-22, A115 | VMM≧200V |
| Latch-Up | JESD 78 | 10ms, $1_{tr}$≧100mA |

## Customer Service

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