USB Power-Distribution Switches

Features

- **VIN Input Voltage Range: 4.5 to 22V**
- **30V Absolute Ratings at VIN Pin**
- **5A Output Current Capability**
- **Low On Resistance**
- **Adjustable Soft-start Time by SS pin**
- **Fast Over Current Protection Response Time**
- **Input Over Voltage Protection by OVSET Pin.**
- **Fault Report on ACOK Pin.**
- **Built in Surge protection clamped at 27V**
- **Built in Thermal Shutdown Protection**
- **Built in True Reverse-Current Blocking (TRCB)**
- **Built in Enable/ Shutdown Control by DPREN Pin-Integrated Internal Charge Pump**
- **ESD Protection :**
  - **EC61000-4-2 contact discharge over with 8kV**
  - **HBM with over 2kV**
  - **CDM with over 500V at VIN pin**
- **TQFN3x3-16D Package**
- **Lead Free and Green Devices Available (RoHS Compliant)**

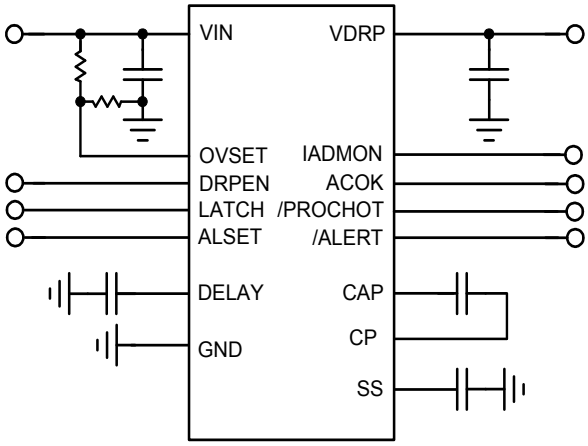
Applications

- **Notebook and Desktop Computers**
- **USB PD Type C Ports/Hubs**
- **High-side Power Protection Switches**

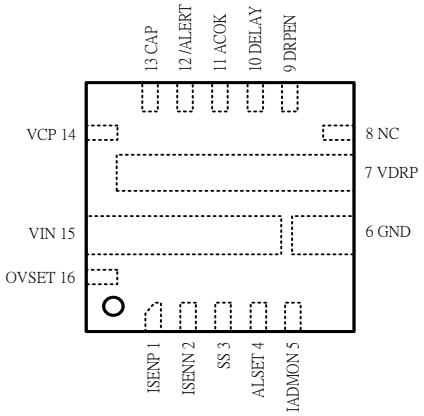
General Description

The APL3572 is designed for USB PD Type C applications. The low on resistance N-channel MOSFET power switch can satisfy the voltage drop requirements of USB specification.
The protection features include current limit protection, short circuit protection, over-temperature protection, input over voltage protection output over voltage protection, out put surge protection and reverse current blocking .
Other features include a deglitched ACOK output to indicate the fault condition and an enable input to enable or disable the device.

Simplified Application Circuit



Pin Configuration



TQFN3x3-16D
(Top View)
APL3572

Ordering and Marking Information

APL3572□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code QB : TQFN3x3-16D Operating Ambient Temperature Range I : -40 to 85°C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APL3572QB: APL 3572 • XXXXX X - Date Code	

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020C for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant)and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter		Rating	Unit
V_{VIN}	VIN to GND Voltage	>20ns pulse width	-0.3 ~ 30	V
		<20ns pulse width	-0.3 ~ 40	V
	ISENN, ISENP to GND Voltage	>20ns pulse width	-0.3 ~ 33	V
		<20ns pulse width	-0.3 ~ 40	V
	DRPEN to GND Voltage		-0.3 ~ 30	V
	/ALERT, ACOK, ALSET, IADMON, OVSET, VCP, SS, DELAY to GND Voltage		-0.3 ~ 6	V
	CAP to GND Voltage		-0.3 ~ 10	V
T_J	Maximum Junction Temperature		-40 ~ 150	°C
T_{STG}	Storage Temperature		-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)		260	°C

Note 1: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under“recommended operating conditions”is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics (Note2)

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air	38.5	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note3)

Symbol	Parameter	Range	Unit
V_{VIN}	VIN Input Voltage	4.5 ~ 22	V
I_{OUT}	OUT Output Current	0~5	A
C_{SS}	SS Pin External Capacitor Range	2.2 ~ 15	nF
C_{IN}	Input Capacitor Range	10 ~ 22	µF
C_{OUT}	Output Capacitor Range	40 ~ 100	µF
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3: Refer to the typical application circuit

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{VIN}=20V, V_{DPREN} =5V and T_A= -40 ~ 85 °C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
BASIC OPERATIOM							
V_{VIN}	VIN Input Voltage			4.5	–	22	V
I_Q	VIN Supply Current	V_{VIN}=20V, No load, V_{DRPEN}=0V		–	–	40	μA
		V_{VIN}=20V, No load, V_{DRPEN}=5V		–	300	–	μA
	VDRP Off State Leakage Current	V_{VIN}=20V, VDRP=GND, V_{DRPEN}=0V		–	–	4	μA
	VDRP Reverse Leakage Current	V_{VIN}=GND, V_{VDRP}=20V, V_{DRPEN}=0V		–	–	1	μA
POWER SWITCH							
$R_{DS(ON)}$	Power Switch On Resistance	V_{VIN}=20V, I_{OUT}=3A, resistance between VIN and VDRP	T_A= 25 °C	–	20	25	mΩ
			T_A= -40 ~ 85 °C	–	20	40	mΩ
UNDER-VOLTAGE LOCKOUT							
V_{UVLO_H}	VIN UVLO Threshold Voltage	V_{VIN} rising, T_A= -40 ~ 85 °C		3.6	3.8	4.0	V
	VIN UVLO Hysteresis			–	0.2	–	V
INPUT CURRENT REPORT							
K	ISENP-to-ISENN Differential Voltage to IADMON Voltage Gain	V_{VIN}=20V		–	32	–	V/V
	IADMON Voltage Accuracy	V_{VIN}=20V, ISENP=ISENN=floating	I_{LOAD}=3A	–	10	–	%
		V_{VIN}=20V, R_{SENSE}=10mΩ	I_{LOAD}=3A	–	1.7	–	%
			I_{LOAD}=5A	–	1.0	–	%
	IADMON Driving Capability			–	–	10	nA
OVER CURRENT PROTECTION							
I_{OCP}	Output Over Current Protection Threshold	V_{VIN}=20V		8	–	–	A
	OCP Response Time	C_L=1μF, VDRP short circuit to ground		–	–	1	μs
	Recovery Time During Hiccup mode	C_{DELAY}=5.6nF		–	16	–	ms
	Precharge Current			–	150	–	mA
	DELAY Source Current			–	10	–	μA
	DELAY Threshold Voltage			–	1	–	V
ACOK AND /ALERT OUTPUT PIN							
	Output Low Voltage	I_{INPUT}=5mA		–	0.2	0.4	V
	Leakage Current	V_{INPUT}=5V, Open drain MOSFET off		–	–	1	μA
	/ALERT Debounce Time			—	1	—	ms
DRPEN INPUT PIN							
V_{IH}	Input Logic HIGH	V_{VIN}=4.5V to 22V, T_A= -40 ~ 85 °C		1.2	–	–	V
V_{IL}	Input Logic LOW	V_{VIN}= 4.5V to 22V, T_A= -40 ~ 85 °C		—	–	0.5	V
	Input Current	V_{DRPEN}= 5V, T_A= -40 ~ 85 °C		–	–	1	μA
SOFTSTART							
	SS Source Current			–	6	–	μA
$t_{D(ON)}$	Turn on Delay Time			–	200	–	μs
$t_{D(OFF)}$	Turn off Delay Time			–	50	–	μs
t_{SS}	Soft-Start Time	No load, C_{OUT}=10μF, V_{VIN}=20 C_{SS}=2.4nF		–	1	–	ms

Electrical Characteristics (Cont.)

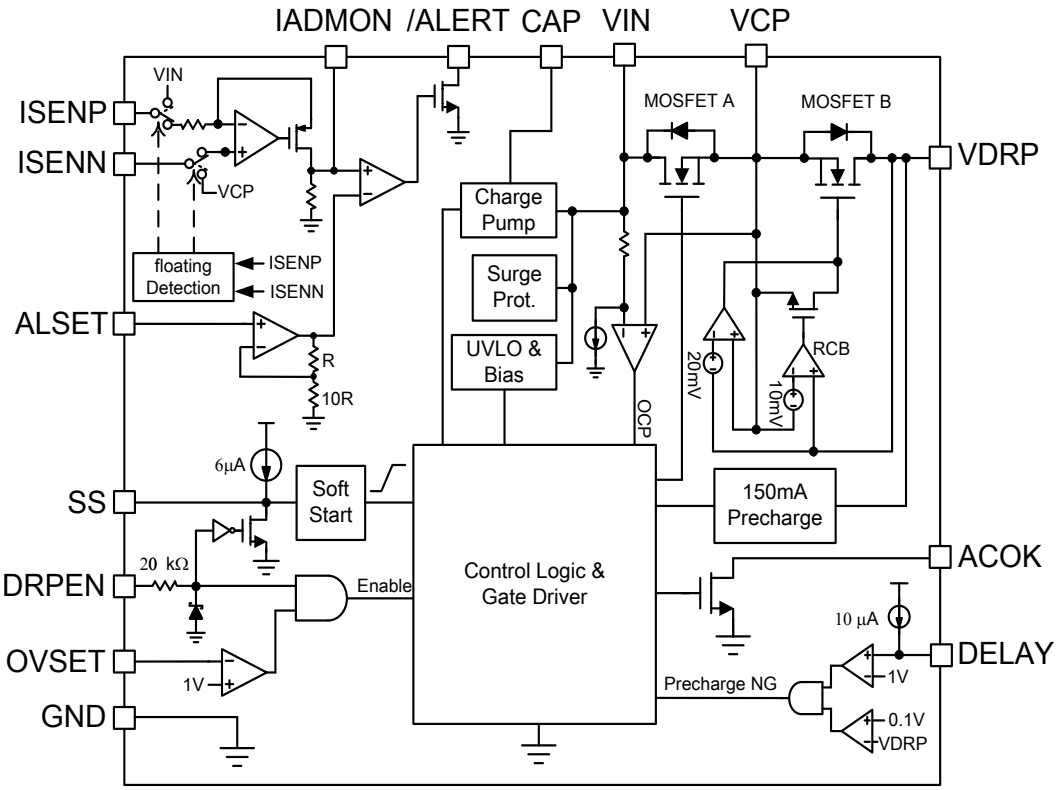
Unless otherwise specified, these specifications apply over V_{VIN}=20V, V_{DPREN} =5V and T_A= -40 ~ 85 °C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OVERT-TEMPERATURE PROTECTION (OTP)						
T_{OTP}	Over-Temperature Threshold	T_J rising	–	150	–	°C
	Over-Temperature Hysteresis		–	50	–	°C
OVER-VOLTAGE AND SURGE PROTECTION						
	OVSET OVP Threshold	V_{OVSET} rising	0.95	1	1.05	V
	OVSET OVP Threshold Hysteresis		–	100	–	mV
	Output Surge Protection Threshold		–	27	–	V

Pin Descriptions

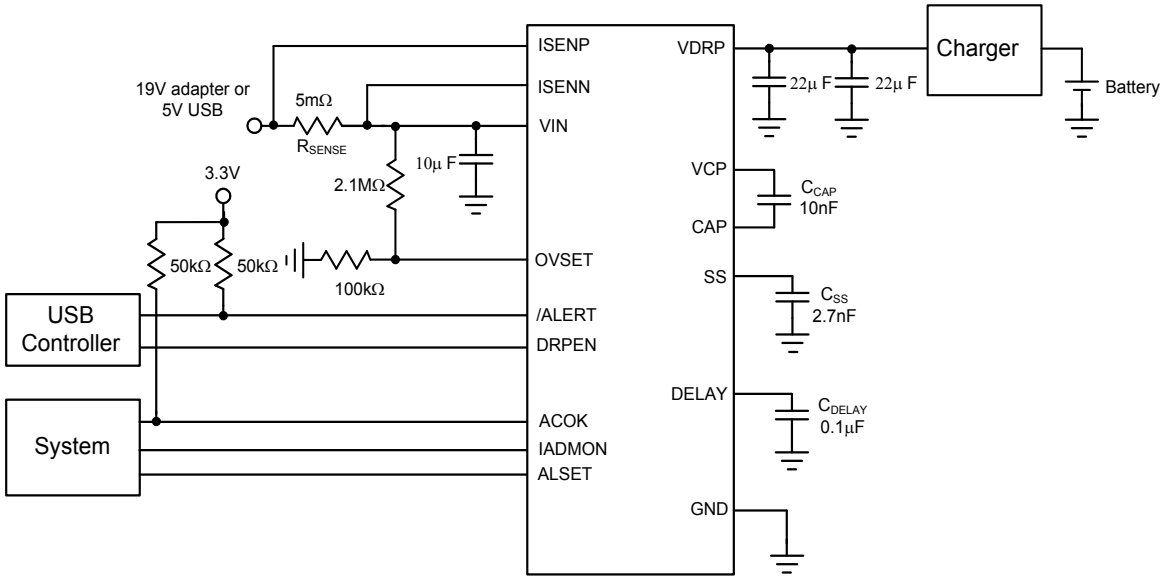
PIN		FUNCTION
NO.	NAME	
1	ISENP	Current Sense "+" input pin. When this pin is not used, it can be left floating. When floating, the APL3572 uses MOSFET A dropout voltage to sense input current.
2	ISENN	Current Sense "–" input pin. When this pin is not used, it can be left floating. When floating, the APL3572 uses MOSFET A dropout voltage to sense input current.
3	SS	VDRP Softstart Slew Rate Control. Connect this pin with a capacitor to ground to adjust VDRP softstart slew rate.
4	ALSET	Power threshold setting for adapter power path
5	IADMON	VIN input current monitoring output pin.
6	GND	Ground.
7	VDRP	Output Voltage Pin. The output voltage follows the input voltage. When DRPEN is low the output voltage is disconnected from input. It is recommended that the output capacitor be placed greater than 40uF.
8	NC	Not connected internally.
9	DRPEN	Enable Input. Pulling this pin to high enables the device while pulling low disables the device. The DRPEN pin cannot be left floating.
10	DELAY	Delay time setting. Connecting a capacitor from this pin to ground sets the delay time which determines when precharge-not-ok protection is activated.
11	ACOK	Fault Indication Pin. This pin goes low when input OVP or OCP condition is detected.
12	/ALERT	Alert output. When V_{IADMON} exceeds 1.1*V_{ALSET} threshold, /ALERT goes low, otherwise /ALERT keeps high.
13	CAP	Charge pump charge storage pin.
14	VCP	Central point of internal two power MOSFETes.
15	VIN	Power Supply Input. Connect this pin to an external DC power supply. It is recommended that the input capacitor be placed greater than 10uF.
16	OVSET	VIN Voltage Sense Pin. Connect this pin to VIN with a resistive divider to monitor VIN voltage for over voltage protection.

Block Diagram

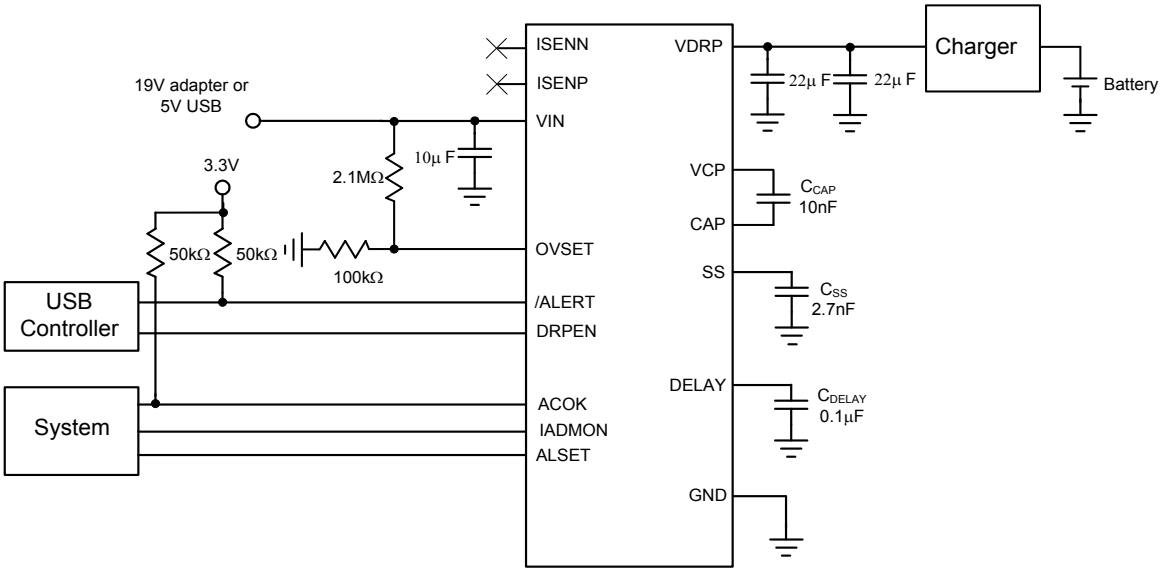


Typical Application Circuit

Application Circuit 1: Current Sense by using an external accurate resistor



Application Circuit 2: Current Sense by using internal power MOSFET's $R_{DS(ON)}$



Function Descriptions

VIN Under-voltage Lockout (UVLO)

The APL3572 is built-in an under-voltage lockout circuit to keep the output shut off until internal circuitry is operating properly. The UVLO circuit has hysteresis and a de-glitch feature so that it will typically ignore undershoot transients on the input. When input voltage exceeds the UVLO threshold, the output voltage starts a soft-start to reduce the inrush current.

Power Switch

The power switches are N-channel MOSFETs with a low $R_{DS(ON)}$. Their body diodes are reversely connected in polarity with each other that can prevent a current flowing from the VDRP back to VIN and VIN to VDRP when IC is off.

Precharge and Softstart

When the APL3572 is enabled, the IC will start a precharge process to determine if there is a short-circuit at VDRP. In precharge process, a 150mA current source is activated to charge output capacitors while a 10μA current source is activated to charge C_{DELAY}. Normally in precharge process the V_{VDRP} will reach 0.1V before V_{DELAY} reaches 1V (PS. DELAY pin must be connected a proper capacitor to ground). The IC then initiates a softstart process to turn on internal power MOSFETes. If a short circuit happens at VDRP during precharge process, the V_{DELAY} will reach 1V while V_{VDRP} is less than 0.1V. The IC then decides not to turn on power MOSFET and in turn enters hiccup mode. When short circuit event is gone, the IC can start a precharge and softstart process to raise V_{VDRP} voltage.

Over Current Protection

The APL3572 provides OCP protection against over load or short circuit conditions. The OCP threshold is proportional to ALSET voltage. When the load current exceeds the OCP threshold, IOCP, for an OCP debounce time, the APL3572 then enters hiccup mode. In the hiccup mode, the output periodically executes soft start process until the fault event has disappeared.

Short-circuit Protection

The APL3572 shuts off output current immediately when output current exceeds short circuit trip threshold in an instant short circuit event.
After the trip of short circuit threshold, the output is shut off and then the device enters hiccup mode. In the hiccup mode, the output periodically executes soft start process until the fault event has disappeared.

ACOK Output

The APL3572 provides an open-drain output to indicate that a fault has occurred. When input OVP or OCP occurs the ACOK goes low. Since the ACOK pin is an open-drain output, connecting a resistor to a pull high voltage is necessary. Normally the pull high resistor is suggested between 2kΩ to 200kΩ.

IADMON, ALSET Input and /ALERT Output

The APL3572 reports the input current to IADMON output pin. Namely, the IADMON output voltage is proportional to input current as shown as the below equation:

$$V_{IADMON}=I_{VIN}*R_{SENSE}*K$$

Where,
I_{VIN} is the input current flowing into VIN pin, which should be equal to load current.
R_{SENSE} is the sensing resistor which could either be the internal MOSFET A $R_{DS(ON)}$ or the external sense resistor, depending on how ISENN and ISENP is connected. Please refer to Typical Application Circuit. The R_{SENSE} is supposed not to exceed 10mΩ for both power dissipation and circuit headroom concern.
K is a constant, which is 31.9.

When V_{IADMON}>1.1*V_{ALSET}, /ALERT goes low, otherwise / ALERT keeps high.

Enable/Disable

Pulling the DRPEN below 0.5V disables the device while pulling DRPEN above 1.2V enables the device. When the IC is disabled the supply current is reduced to less than 40μA. The enable input is compatible with both TTL and CMOS logic levels. The DRPEN pin cannot be left floating.

Over-temperature Protection

When the junction temperature exceeds 150°C, the internal thermal sense circuit turns off the power FET and allows the device to cool down. When the device's junction temperature cools by 50°C, the internal thermal sense circuit will enable the device, resulting in a pulsed output during continuous thermal protection. Thermal protection is designed to protect the IC in the event of over temperature conditions. For normal operation, the junction temperature cannot exceed T_J=+125°C.

Revere Current Block

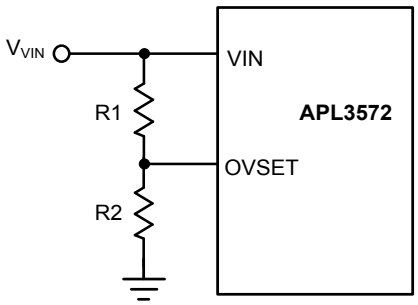
The APL3572 provides reverse current block function or RCB to prevent current flowing from VDRP to VIN. This function can emulate the internal MOSFET B as an ideal diode. In other words, the current is only allowed to flow from VIN to VDRP but forbidden from VDRP to VIN. During normal operation, if a voltage higher then V_{VIN} appears at VDRP, the reverse current could generate a voltage drop between VDRP and VCP. When V_{VDRP} - V_{VCP}>10mV is triggered, the RCB function is activated then. There is another scenario when RCB can be activated. In normal operation if a short circuit happens at VIN, the RCB function can stop current flowing from VDRP to VIN, too. In light load or no load conditions, The VVDRP is regulated at V_{VIN}-20mV until load current is large enough to produce a voltage drop(=I_{LOAD}*$R_{DS(ON)}$) across VDRP to VIN higher than 20mV.

Function Descriptions

VIN Over Voltage Protection

The APL3572 uses OVSET pin to sense input voltage for over voltage protection. The internal VIN OVP threshold is 1V. A resistor divider from VIN to OVSET can program the VIN over voltage threshold, as depicted as below diagram. The VIN OVP threshold can be calculated by the following equation:

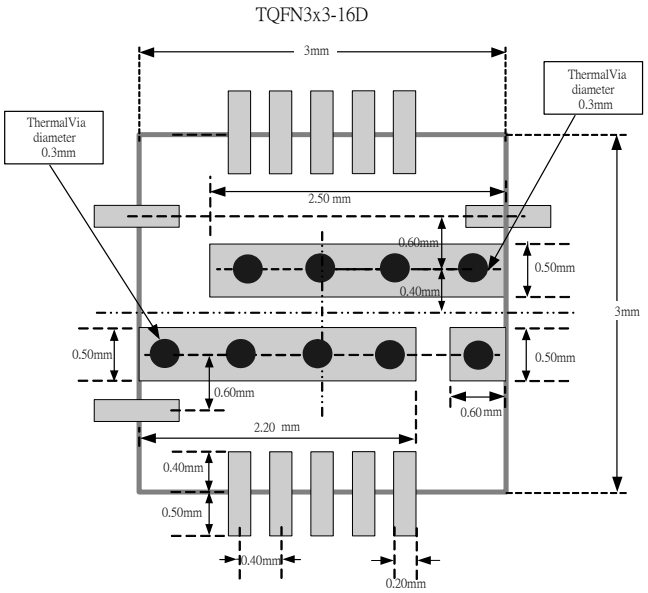
V_{VIN_OVP}=(R1+R2)/R2*1V



Surge Protection

The APL3572 has surge protection on VDRP pin. Any voltage surge surpasses 27V will be clamped to a safe level.

Recommended Minimum Footprint



Application Information

Input Capacitor

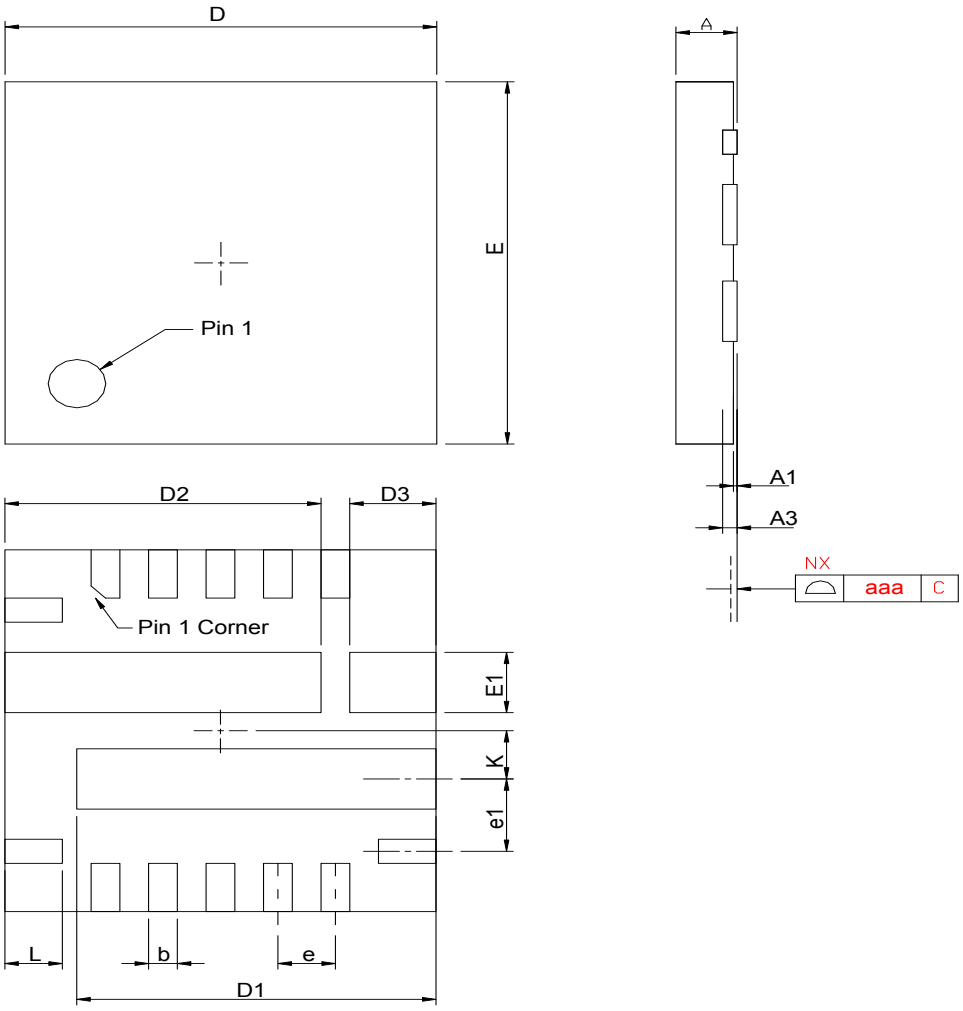
A 10µF or higher ceramic bypass capacitor from VIN to GND, located near the APL3572, is strongly recommended to suppress the ringing during short circuit fault event. When the load current trips the SCP threshold in an over load condition such as a short circuit, hot plug-in or heavy load transient the IC immediately turns off the internal power switch that will cause VIN ringing due to the inductance between power source and VIN. Without the bypass capacitor, the output short may cause sufficient ringing on the input to damage internal control circuitry.
Input capacitor is especially important to prevent V_{IN} from ringing too high in some applications where the inductance between power source to VIN is large (ex, an extra bead is added between power source line to VIN for EMI reduction), additional input capacitance may be needed on the input to reduce voltage overshoot from exceeding the absolute maximum voltage of the device during over load conditions.

Output Capacitor

A low-ESR 40µF between VDRP and GND is strongly recommended to reduce the voltage droop during hot-attachment of downstream peripheral.
Higher-value output capacitor is better when the output load is heavy. Additionally, bypassing the output with a 0.1µF ceramic capacitor improves the immunity of the device to short-circuit transients.

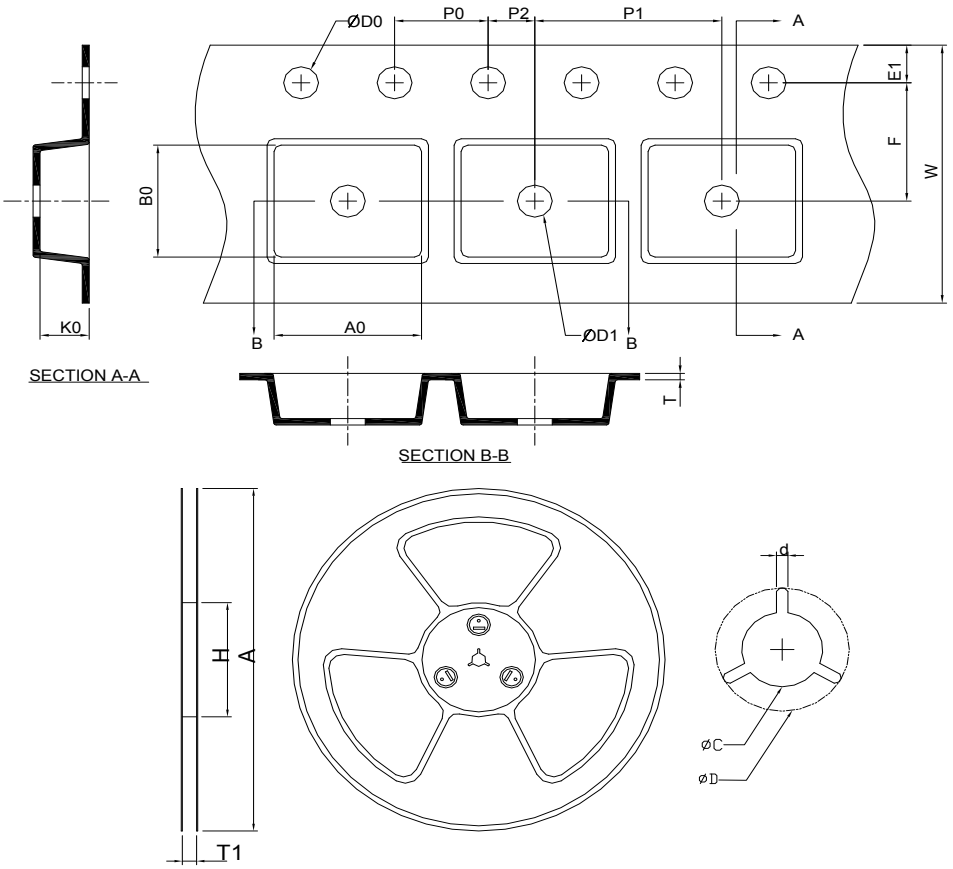
Package Information

TQFN3x3-16D



SYMBOL	TQFN3x3-16D			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.15	0.25	0.006	0.010
D	2.90	3.10	0.114	0.122
D1	2.40	2.60	0.095	0.102
D2	2.10	2.30	0.083	0.091
D3	0.50	0.70	0.020	0.028
E	2.90	3.10	0.114	0.122
E1	0.40	0.60	0.016	0.024
e	0.40 BSC		0.016 BSC	
e1	0.60 BSC		0.024 BSC	
K	0.40 BSC		0.016 BSC	
L	0.30	0.50	0.012	0.020
aaa	0.08		0.003	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFN 3*3-16D	330±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.00±0.20

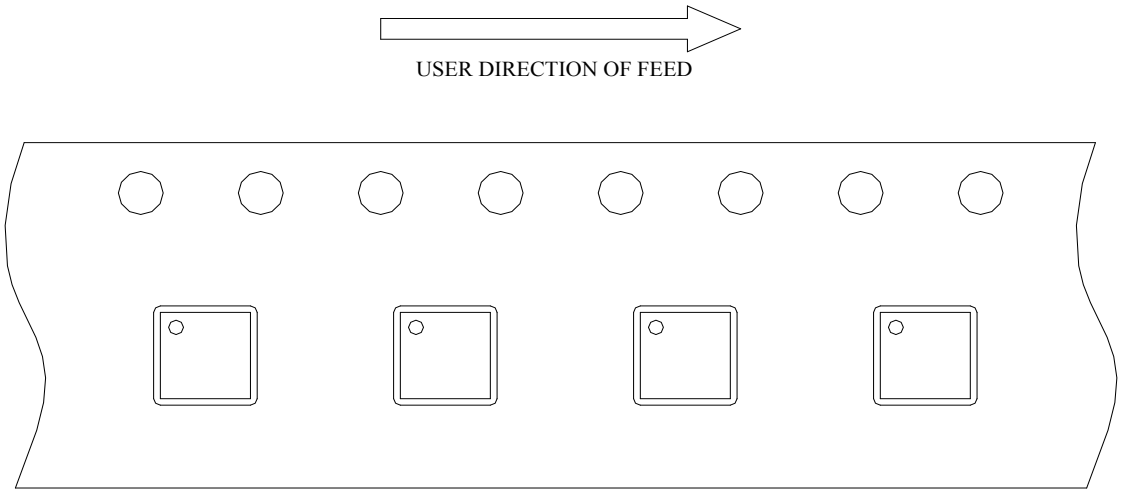
(mm)

Devices Per Unit

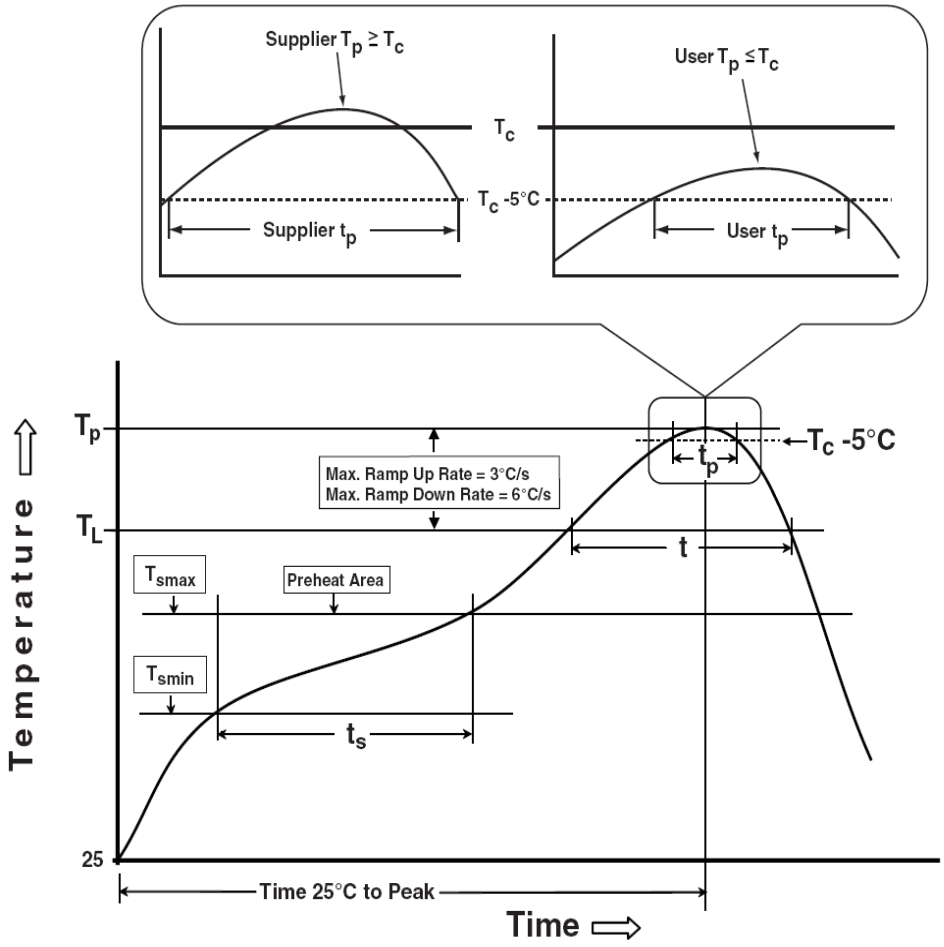
Package type	Packing	Quantity
TQFN 3*3	Tape & Reel	3000

Taping Direction Information

TQFN3x3-16D



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≧ 2KV
MM	JESD-22, A115	VMM ≧ 200V
Latch-Up	JESD 78	10ms, 1_{tr} ≧ 100mA

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Revision History

Version	Date	Revision History	
		Chapter	Description
P1	2017/6/13	-	Preliminary
P2	2017/6/15	-	1. Add Package Information 2. correct DRPEN pin description in Pin Desciptions 3. delete the spec Hiccup Entering Threshold
P3	2017/7/7	-	1. update Typical Application Circuit. 2. update Pin Configuration. 3. update Pin Description 4. update VIN Over Voltage Protection in Function Descriptions 5. change Precharge Current from 300mA to 150mA 6. change OTP hys from 20℃ to 50℃ 7. change Output Surge Protection Threshold from 40V to 31V typ. 8. update Package Information
P4	2017/8/7	-	1. update Block Diagram 2. θJA=38.5℃ /W 3. Recomomended Css=2.5 ~ 12.63nF 4. VIN Supply CurrentV=40uA max. @VDRPEN=0 5. VIN Supply Current=300uA typ. @VDRPEN=5V 6. update Typical Application Circuit 7. DRPEN maximum rating is changed to –0.3V ~ 30V
P5	2017/10/24		1. change IADMON Voltage Gain from 31.9 to 32. 2. update Typical Application Circuit 3. update Block Diagram
A1	2019/02/20		modify cap capacitor to 10nF