USB Power-Distribution Switches

Features

- **VIN Input Voltage Range: 4.5 to 25V**
- **30V Absolute Ratings at VIN Pin**
- **10A Output Current Capability**
- **Low On Resistance**
- **Adjustable Soft-start Time by SS pin**
- **Fast Over Current Protection Response Time**
- **Input Under Voltage Protection by VINUVP Pin.**
- **Fault Report on ACOK Pin.**
- **Built-in Surge Protection when Surge Voltage over 27V**
- **Built-in Thermal Shutdown Protection**
- **Built-in Enable/ Shutdown Control by DPREN Pin**
- **Integrated Internal Charge Pump**
- **Built-in Programmable Short Circuit or Over Current Protection Threshold Setting by ALSET pin**
- **ESD Protection :**
  - **EC61000-4-2 contact discharge over with 8kV**
  - **HBM with over 2kV**
  - **CDM with over 500V at VIN pin**
- **TQFN4x4-16C Package**
- **Lead Free and Green Devices Available (RoHS Compliant)**

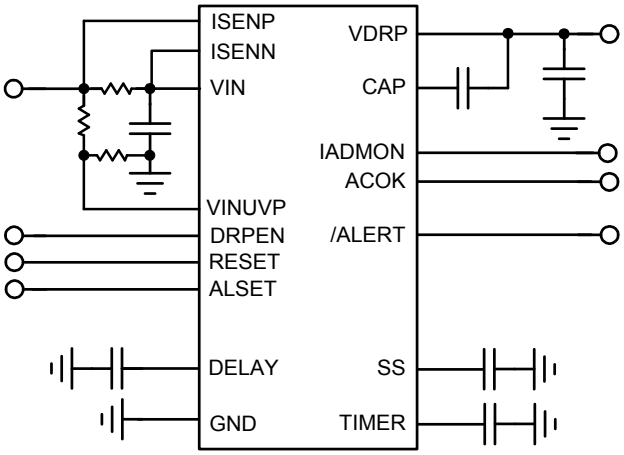
Applications

- **Notebook and Desktop Computers**
- **High-side Power Protection Switches**

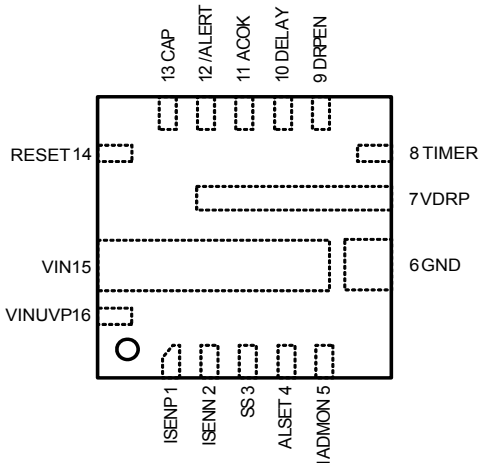
General Description

The APL3573A is designed for desktop adapter applications. The low on resistance N-channel MOSFET power switch can satisfy the voltage drop requirements of USB specification.
The protection features include OCP protection, short circuit protection, over-temperature protection, input under voltage protection, input surge protection.
Other features include a deglitched ACOK output to indicate the fault condition and an enable input to enable or disable the device.

Simplified Application Circuit



Pin Configuration



TQFN4x4-16C
(Top View)
APL3573A

Ordering and Marking Information

APL3573A □□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code QB : TQFN4x4-16C Operating Ambient Temperature Range I : -40 to 85°C Handling Code Temperature Range TR : Tape & Reel Assembly Material L : Lead Free Device G : Halogen and Lead Free Device
APL3573AQB:  XXXXX - Date Code	

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020C for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant)and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter		Rating	Unit
V_{VIN}	VIN to GND Voltage	>20ns pulse width	-0.3 ~ 30	V
		<20ns pulse width	-0.3 ~ 40	V
	ISENN, ISENP to GND Voltage	>20ns pulse width	-0.3 ~ 33	V
		<20ns pulse width	-0.3 ~ 40	V
	DRPEN		-0.3 ~ 30	V
	/ALERT, ACOK, ALSET, IADMON, RESET, VINUVP, DELAY,TIMER,SS,CAP to GND Voltage		-0.3 ~ 6	V
T_J	Maximum Junction Temperature		-40 ~ 150	°C
T_{STG}	Storage Temperature		-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)		260	°C
	Surge protection withstand energy		32	mJ

Note 1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under"recommended operating conditions"is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics (Note2)

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air	36.46	°C/W
θ_{JC}	Junction-to-Case Resistance in free air	12	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note3)

Symbol	Parameter	Range	Unit
V_{VIN}	VIN Input Voltage	4.5 ~ 25	V
I_{OUT}	OUT Output Current	0 ~ 10	A
C_{SS}	SS Pin External Capacitor Range	2.2 ~ 15	nF
C_{IN}	Input Capacitor Range	22 ~ 100	µF
C_{OUT}	Output Capacitor Range	10 ~ 100	µF
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3: Refer to the typical application circuit.

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{VIN}=20V, V_{DPREN} =5V and T_A= -40 ~ 85°C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
BASIC OPERATIOM							
V_{VIN}	VIN Input Voltage			4.5	-	25	V
I_Q	VIN Supply Current	V_{VIN}=20V, No load, V_{DRPEN}=0V		-	-	40	μA
		V_{VIN}=20V, No load, V_{DRPEN}=5V		-	300	-	μA
	VDRP Off State Leakage Current	V_{VIN}=20V, VDRP=GND, V_{DRPEN}=0V		-	-	4	μA
POWER SWITCH							
$R_{DS(ON)}$	Power Switch On Resistance	V_{VIN}=20V, resistance between VIN and VDRP	I_{OUT}=3A, T_A= 25 °C	-	8	10	mΩ
			I_{OUT}=3A, T_A= -40 ~ 85 °C,	-	8	14	mΩ
			I_{OUT}=10A, T_A= 25 °C	-	8	14	mΩ
			I_{OUT}=10A, T_A= -40 ~ 85°C	-	8	14	mΩ
UNDER-VOLTAGE LOCKOUT							
V_{UVLO_H}	VIN UVLO Threshold Voltage	V_{VIN} rising, T_A= -40 ~ 85 °C		3.6	3.8	4.0	V
	VIN UVLO Hysteresis			-	0.2	-	V
INPUT CURRENT REPORT							
K	ISENP-to-ISENN Differential Voltage to IADMON Voltage Gain	V_{VIN}=20V		-	20	-	V/V
	IADMON Voltage Accuracy	V_{VIN}=20V	R_{SENSE}=5mΩ, I_{LOAD}=3A	-3	0	3	%
			R_{SENSE}=5mΩ, I_{LOAD}=10A	-1	0	1	%
			R_{SENSE}=10mΩ, I_{LOAD}=3A	-1.7	0	1.7	%
			R_{SENSE}=10mΩ, I_{LOAD}=10A	-1	0	1	%
	IADMON Driving Capability			-	-	10	nA
	ALSET Internal Pull High Current	V_{ALSET}=1V, T_A= 25 °C		9.7	10	10.3	μA
	TIMER Internal Pull High Current			-	11	-	μA
	/ALERT Threshold	V_{IADMON}/V_{ALSET}		-	1	-	V/V
OVER CURRENT PROTECTION							
I_{SCP}	Short Circuit Protection Threshold	V_{VIN}=20V		66	-	-	A
	SCP Response Time	C_L=1μF, VDRP short circuit to ground		-	-	1	μs
t_{HICC}	Recovery Time During Hiccup mode	C_{DELAY}=5.6nF, T_{DELAY}= C_{DELAY}*1V/I_{DELAY}		-	7*T_{DELAY}	-	ms
	Precharge Current			-	150	-	mA
	DELAY Source Current			-	12	-	μA
	DELAY Threshold Voltage			-	1	-	V
	VDRP Precharge Threshold			-	0.1	-	V
ACOK AND /ALERT OUTPUT PIN							
	Output Low Voltage	I_{INPUT}=5mA		-	0.2	0.4	V
	Leakage Current	V_{INPUT}=5V, Open drain MOSFET off		-	-	1	μA
	/ALERT Debounce Time			-	1	-	ms

Electrical Characteristics (Cont.)

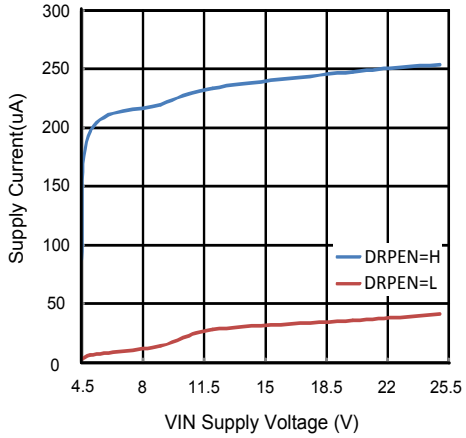
Unless otherwise specified, these specifications apply over V_{VIN}=20V, V_{DPREN} =5V and T_A= -40 ~ 85°C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DRPEN INPUT PIN						
V_{IH}	Input Logic HIGH	V_{VIN}=4.5V to 25V, T_A= -40 ~ 85 °C	1.2	-	-	V
V_{IL}	Input Logic LOW	V_{VIN}= 4.5V to 25V, T_A= -40 ~ 85 °C	-	-	0.5	V
	Input Current	V_{DRPEN}= 5V, T_A= -40 ~ 85 °C	-	-	1	μA
SOFTSTART						
	SS Source Current		-	6	-	μA
$t_{D(ON)}$	Turn on Delay Time		-	200	-	μs
$t_{D(OFF)}$	Turn off Delay Time		-	50	-	μs
t_{SS}	Soft-Start Time	No load, C_{OUT}=10μF, V_{VIN}=20V, C_{SS}=2.7nF	-	1.3	-	ms
		No load, C_{OUT}=10μF, V_{VIN}=20V, C_{SS}=open	-	50	100	μs
OVERT-TEMPERATURE PROTECTION (OTP)						
T_{OTP}	Over-Temperature Threshold	T_J rising	-	150	-	°C
	Over-Temperature Hysteresis		-	30	-	°C
UNDER-VOLTAGE AND SURGE PROTECTION						
	VINUVP UVP Threshold	V_{VINUVP} rising	0.95	1	1.05	V
	VINUVP UVP Threshold Hysteresis		-	100	-	mV
	VIN Surge Protection Threshold		-	27	-	V

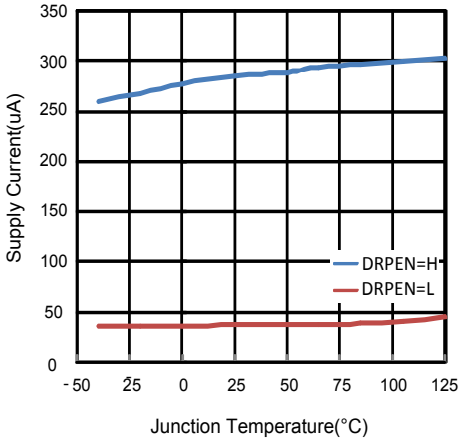
Typical Operating Characteristics

Refer to the typical application circuit. The test condition is V_{IN}=20V, C_{SS}=2.7nF, C_{CAP}=1nF, C_{DELAY}=5.6nF, C_{IN}=10µF, C_{OUT}=22µF*2 , T_A= 25°C unless otherwise specified.

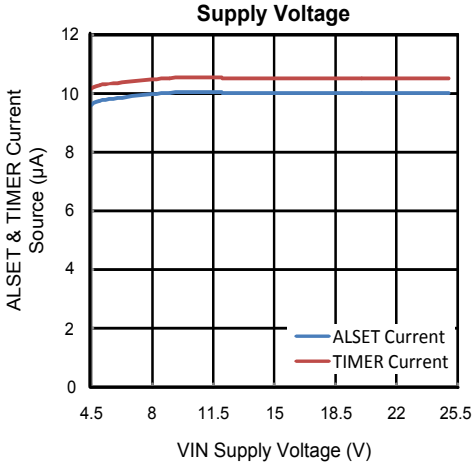
VIN Supply Current vs. Supply Voltage



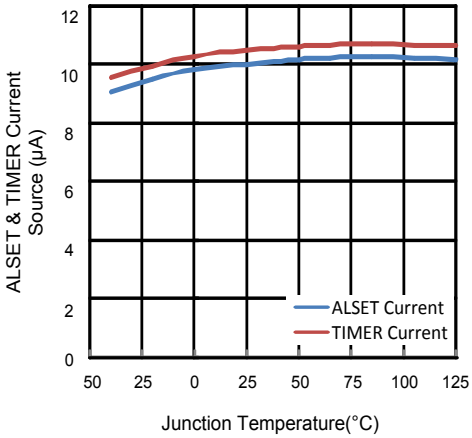
VIN Supply Current vs. Junction Temperature



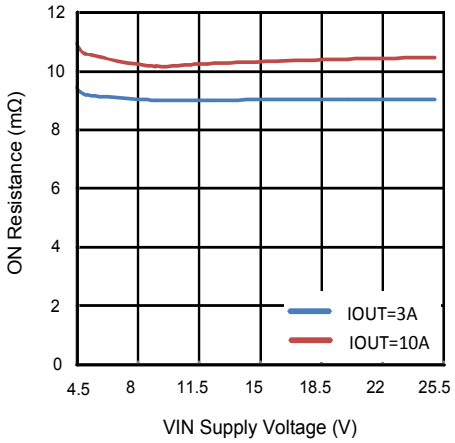
ALSET & TIMER Current Source vs. Supply Voltage



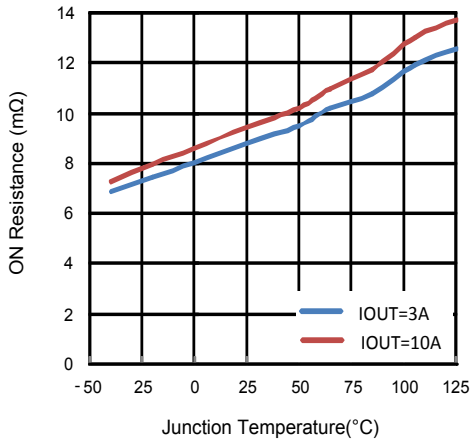
ALSET & TIMER Current Source vs. Junction Temperature



ON Resistance vs. Supply Voltage



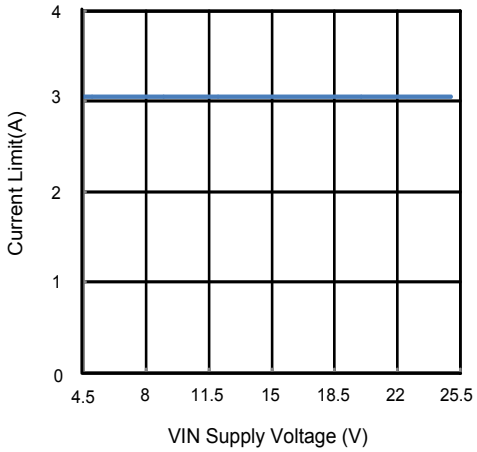
ON Resistance vs. Junction Temperature



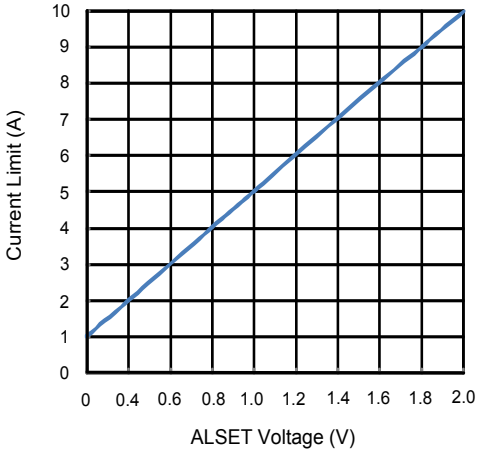
Typical Operating Characteristics (Cont.)

Refer to the typical application circuit. The test condition is V_{IN}=20V, C_{SS}=2.7nF, C_{CAP}=1nF, C_{DELAY}=5.6nF, C_{IN}=10µF, C_{OUT}=22µF*2 , T_A= 25°C unless otherwise specified.

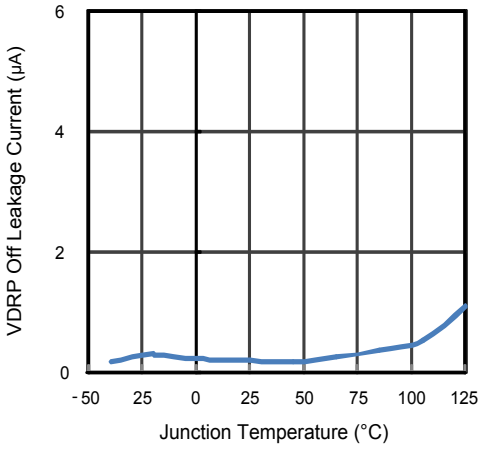
Current Limit vs. Supply Voltage



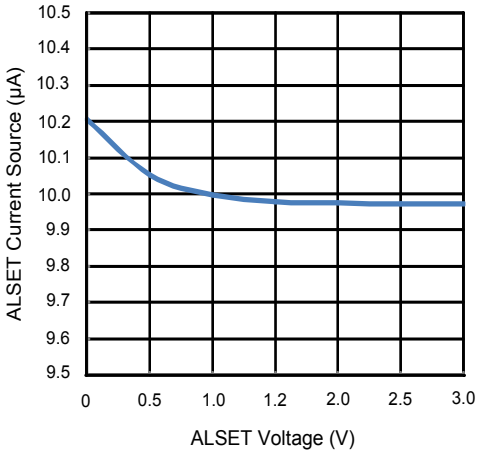
Current Limit vs. ALSET Voltage



VDRP Off Leakage Current vs. Junction Temperature



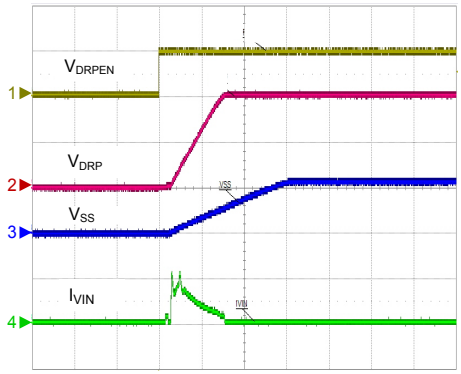
ALSET Current Source vs. ALSET Voltage



Operating Waveforms

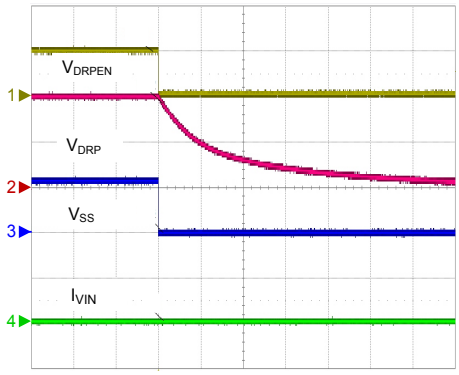
The test condition is V_{IN}=20V, C_{SS}=2.7nF, C_{CAP}=1nF, C_{DELAY}=5.6nF, C_{IN}=10µF, C_{OUT}=22µF*2,T_A= 25°C unless otherwise specified.

EN Power On



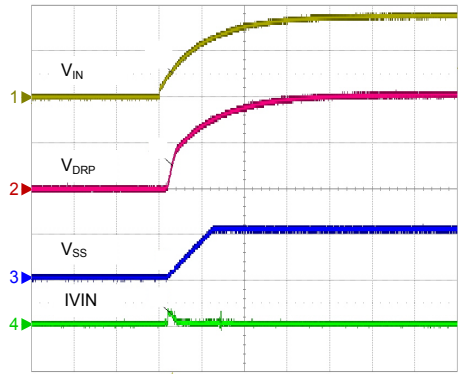
I_{LOAD} =0A
CH1: V_{DRPEN}, 5V/Div, DC
CH2: V_{DRP}, 10V/Div, DC
CH3: V_{SS}, 5V/Div, DC
CH4: I_{VIN}, 1A/Div, DC
TIME: 1ms/Div

EN Power Off



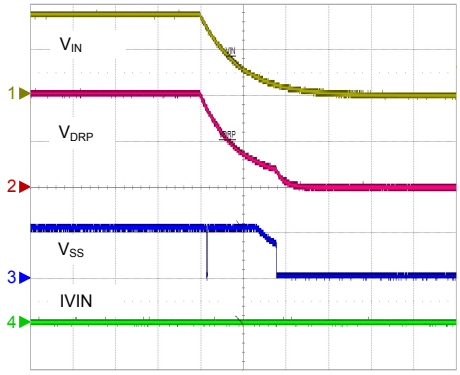
I_{LOAD} =0A
CH1: V_{DRPEN}, 5V/Div, DC
CH2: V_{DRP}, 10V/Div, DC
CH3: V_{SS}, 5V/Div, DC
CH4: I_{VIN}, 1A/Div, DC
TIME: 20ms/Div

VIN Power On



I_{LOAD} =0A
CH1: V_{IN}, 10V/Div, DC
CH2: V_{DRP}, 10V/Div, DC
CH3: V_{SS}, 5V/Div, DC
CH4: I_{VIN}, 2A/Div, DC
TIME: 2ms/Div

VIN Power Off

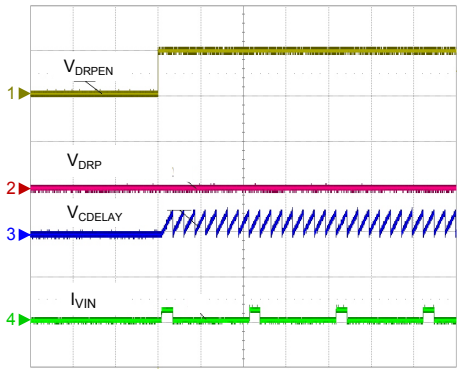


I_{LOAD} =0A
CH1: V_{IN}, 10V/Div, DC
CH2: V_{DRP}, 10V/Div, DC
CH3: V_{SS}, 5V/Div, DC
CH4: I_{VIN}, 2A/Div, DC
TIME: 200ms/Div

Operating Waveforms (Cont.)

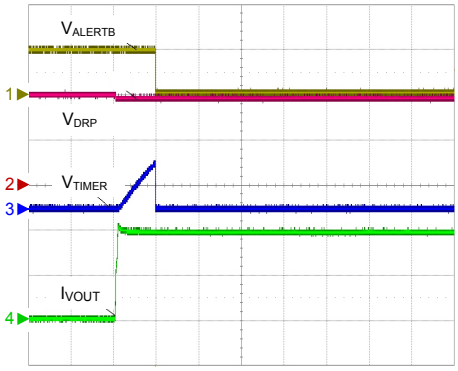
The test condition is V_{IN}=20V, C_{SS}=2.7nF, C_{CAP}=1nF, C_{DELAY}=5.6nF, C_{IN}=10µF, C_{OUT}=22µF*2,T_A= 25°C unless otherwise specified.

Device Enable in VDRP short to GND



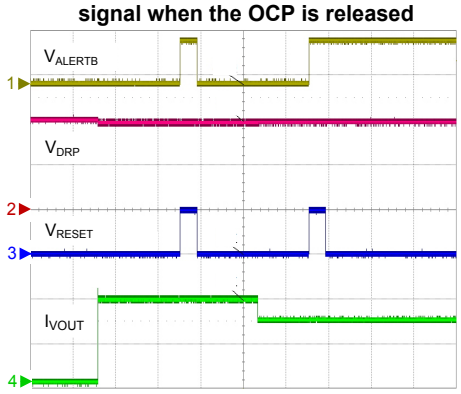
I_{LOAD} =0A
CH1: V_{DRPEN}, 5V/Div, DC
CH2: V_{DRP}, 10V/Div, DC
CH3: V_{CDELAY}, 2V/Div, DC
CH4: I_{VIN}, 500mA/Div, DC
TIME: 2ms/Div

Device Enable in Over Current Protection



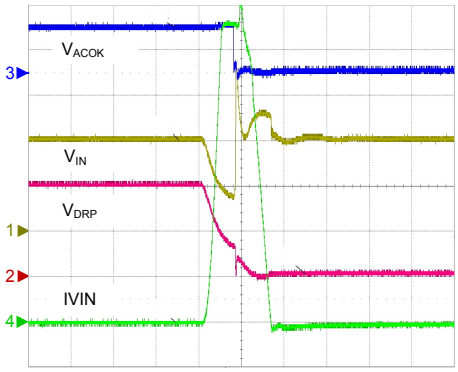
I_{LOAD} =0 to 4A,ALSET=0.8V.
CH1: V_{ALERTB}, 5V/Div, DC
CH2: V_{DRP}, 10V/Div, DC
CH3: V_{TIMER}, 1V/Div, DC
CH4: I_{VOUT}, 2A/Div, DC
TIME: 1ms/Div

RESET pin clears the ALERTB signal when the OCP is released



I_{LOAD} =0A to 4A to 3A, ALSET=0.8V.
CH1: V_{ALERTB}, 5V/Div, DC
CH2: V_{DRP}, 10V/Div, DC
CH3: V_{RESET}, 5V/Div, DC
CH4: I_{VOUT}, 2A/Div, DC
TIME: 500ms/Div

Short Circuit Response

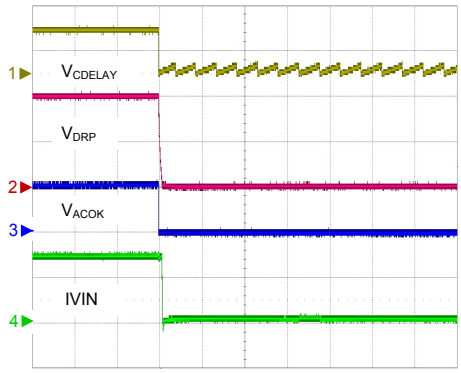


VDRP short to ground.
CH1: V_{IN}, 10V/Div, DC
CH2: V_{DRP}, 10V/Div, DC
CH3: V_{ACOK}, 5V/Div, DC
CH4: I_{VIN}, 10A/Div, DC
TIME: 2us/Div

Operating Waveforms (Cont.)

The test condition is V_{IN}=20V, C_{SS}=2.7nF, C_{CAP}=1nF, C_{DELAY}=5.6nF, C_{IN}=10µF, C_{OUT}=22µF*2,T_A= 25°C unless otherwise specified.

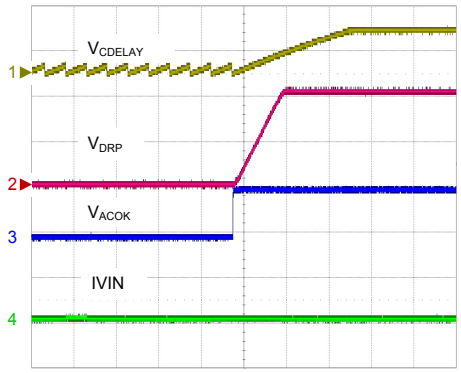
VDRP Short to GND



I_{LOAD} =0A

CH1: V_{DELAY}, 5V/Div, DC
CH2: V_{DRP}, 10V/Div, DC
CH3: V_{ACOK}, 5V/Div, DC
CH4: I_{VIN}, 5A/Div, DC
TIME: 1ms/Div

Short Circuit Release



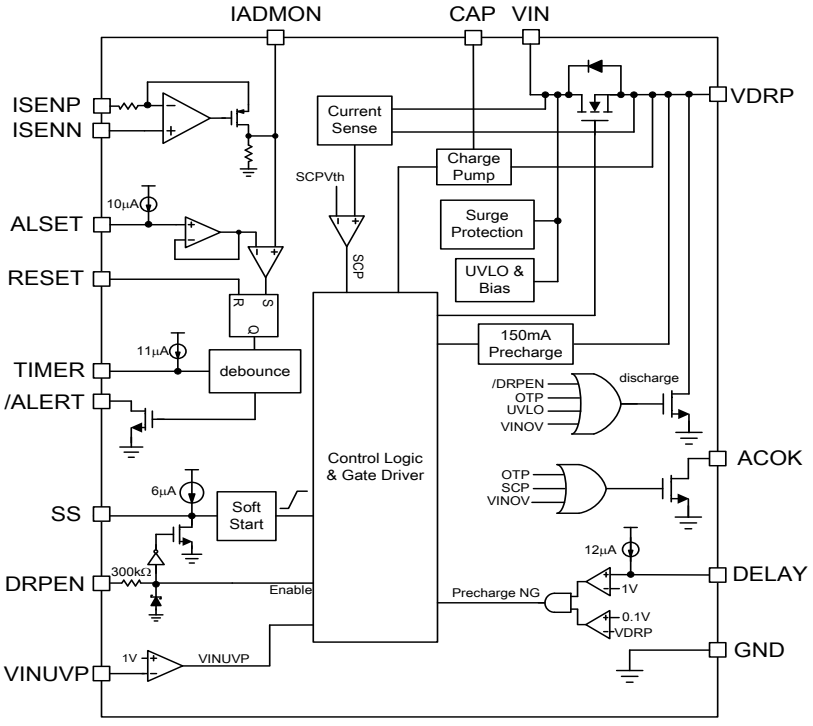
I_{LOAD} =0A

CH1: V_{DELAY}, 5V/Div, DC
CH2: V_{DRP}, 10V/Div, DC
CH3: V_{ACOK}, 5V/Div, DC
CH4: I_{VIN}, 5A/Div, DC
TIME: 1ms/Div

Pin Descriptions

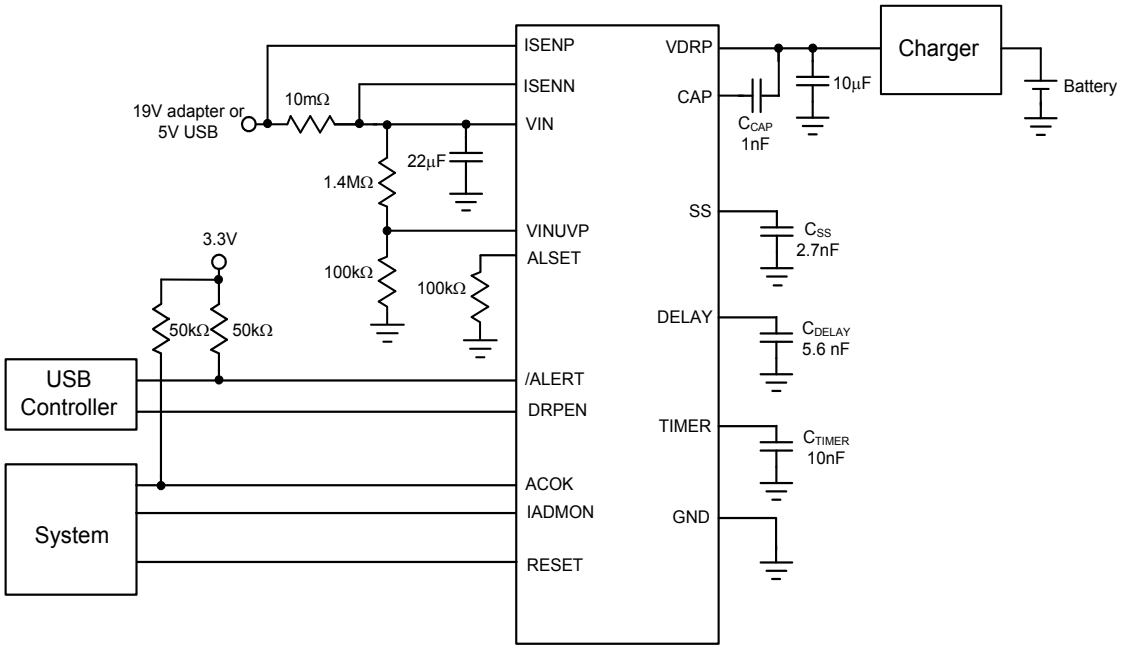
PIN		FUNCTION
NO.	NAME	
1	ISENP	Current Sense “+“ input pin.
2	ISENN	Current Sense “–“ input pin.
3	SS	VDRP Softstart Slew Rate Control. Connect this pin with a capacitor to ground to adjust VDRP softstart slew rate.
4	ALSET	Power threshold setting for adapter power path
5	IADMON	VIN input current monitoring output pin.
6	GND	Ground.
7	VDRP	Output Voltage Pin. The output voltage follows the input voltage. When DRPEN is low the output voltage is disconnected from input. It is recommended that the output capacitor be placed greater than 10uF.
8	TIMER	Debounce time setting pin for /ALERT. When the event of V_{IADMON}>V_{ALSET} persists over the debounce time set by the TIMER pin, the APL3573A latches /ALERT at low level.
9	DRPEN	Enable Input. Pulling this pin to high enables the device while pulling low disables the device. The DRPEN pin cannot be left floating.
10	DELAY	Delay time setting. Connecting a capacitor from this pin to ground sets the delay time which determines when precharge-not-ok protection is activated.
11	ACOK	Fault Indication Pin. This pin goes low when input UVP or OCP condition is detected.
12	/ALERT	Alert output. When V_{IADMON} exceeds 1.0*V_{ALSET} threshold, /ALERT goes low, otherwise /ALERT keeps high.
13	CAP	Charge pump charge storage pin.
14	RESET	Reset input pin. When the /ALERT is latched at low level due to a event of V_{IADMON}>V_{ALSET}, a high level pulse (whose width is 1us at least) present at RESET pin can release /ALERT from low state to high state.
15	VIN	Power Supply Input. Connect this pin to an external DC power supply. It is recommended that the input capacitor be placed greater than 22uF.
16	VINUVP	VIN Voltage Sense Pin. Connect this pin to VIN with a resistive divider to monitor VIN voltage for UVP protection.

Block Diagram

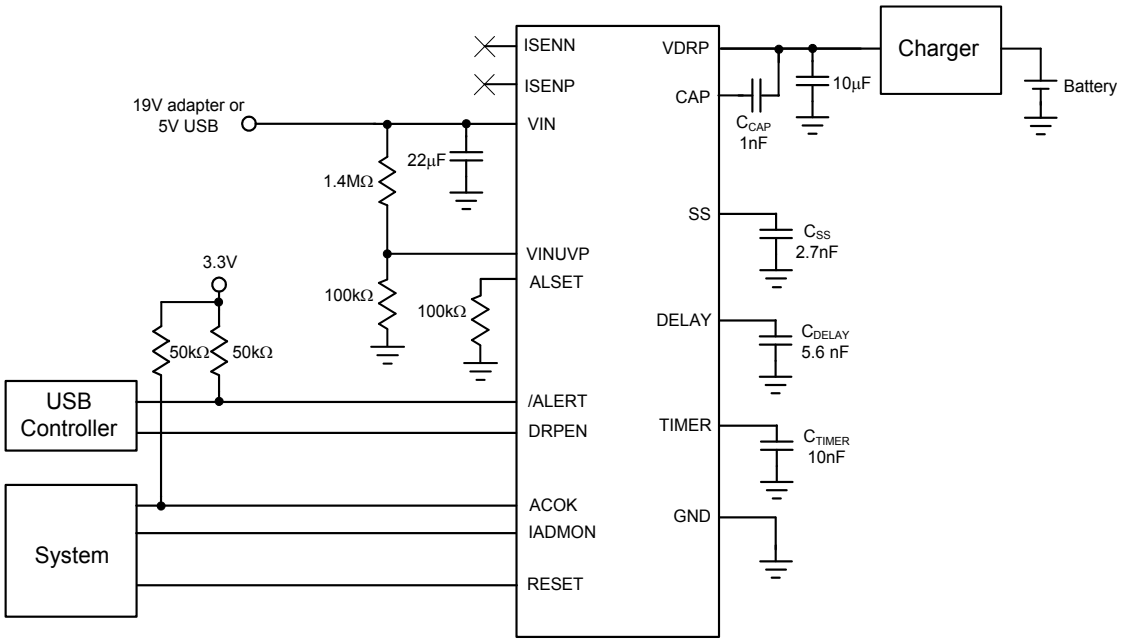


Typical Application Circuit

Application Circuit 1: Current Sense by using an external accurate resistor



Application Circuit 2: Current Sense by using internal power MOSFET's $R_{DS(ON)}$



Function Descriptions

VIN Under-voltage Lockout (UVLO)

The APL3573A is built-in an under-voltage lockout circuit to keep the output shut off until internal circuitry is operating properly. The UVLO circuit has hysteresis and a deglitch feature so that it will typically ignore undershoot transients on the input. When input voltage exceeds the UVLO threshold, the output voltage starts a soft-start to reduce the inrush current.

Power Switch

The power switches are N-channel MOSFETs with a low $R_{DS(ON)}$.

Precharge and Softstart

When the APL3573A is enabled, the IC will start a precharge process to determine if there is a short-circuit at VDRP. In precharge process, a 150mA current source is activated to charge output capacitors while a 12μA current source is activated to charge C_{DELAY}. Normally in precharge process the V_{VDRP} will reach 0.1V before V_{DELAY} reaching 1V (while DELAY pin requires a proper capacitor to ground). The IC then initiates a softstart process to turn on internal power MOSFET. If a short circuit happens at VDRP during precharge process, the V_{DELAY} will reach 1V before V_{VDRP} reaches 0.1V. The IC then decides not to turn on power MOSFET and in turn enters hiccup mode. When short circuit event is gone, the IC can start a precharge and softstart process to raise up V_{VDRP} voltage.

The relationship between V_{SS} voltage and V_{VDRP} voltage ratio is 0.125 times during softstart.
For example, the V_{VDRP} voltage is equal to 20V when the V_{SS} voltage is equal to 2.5V during softstart.
The softstart time can be calculated by the following equation:

$V_{SS}=V_{VDRP}*0.125$

$T_{SS}=(C_{SS}* V_{SS})/6uA(I_{SS})$

Short Circuit Protection

The APL3573A provides SCP protection against over load or short circuit conditions. When Output current above 66A, SCP protection occurs and the APL3573A immediately shuts off the internal power MOSFET and then enters hiccup mode. In the hiccup mode, the output periodically executes soft start process until the fault event has disappeared. When input a 170W adapter (Output Voltage is 20V and Output Current is 8.5A), we can make sure that APL3573A will not be damaged for the short circuit condition.

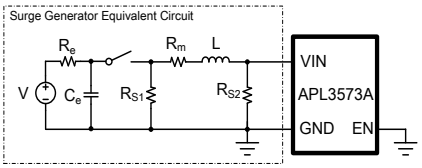
Surge Protection

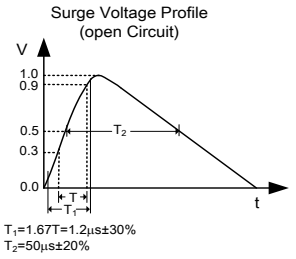
The APL3573A implements a surge protection function in its VIN pin. When a sudden voltage spike appearing on VIN pin is high enough to trigger the surge protection, the APL3573A will limit this voltage at 27V(typical value) and conduct the surge current to ground through an internal low impedance path until the surge protection is no longer activated (namely, below 27V).
Please note that there is a limit of surge protection function: The surge protection function can only deal with transient voltage. If the surge protection function is activated for a long time, the APL3573A's junction temperature will rise and eventually cause potential damage.

Surge Protection (Cont.)

Typically, the APL3573A can sustain a sudden surge when the total dissipating energy is below 32mJ. Please do not operate the APL3573A surge protection function beyond this limitation. The APL3573A can deal with a surge up to V=120V. The capability of surge protection function was evaluated by the method as depicted as below diagram. We used an IEC61000-4-5 and IEC801-5 compliant surge generator to test the capability of surge protection function. The surge generator generates a voltage which is 1.2μs/50μs (open circuit) as shown in the profile below.

Evaluation Method of Surge Protection





ACOK Output

The APL3573A provides an open-drain output to indicate that a fault has occurred. When input UVP or OCP occurs the ACOK goes low. Since the ACOK pin is an open-drain output, connecting a resistor to a pull high voltage is necessary. Normally the pull high resistor is suggested between 2kΩ to 200kΩ.

Enable/Disable

Pulling the DRPEN below 0.5V disables the device while pulling DRPEN above 1.2V enables the device. When the IC is disabled the supply current is reduced to a low level. The enable input is compatible with both TTL and CMOS logic levels. The DRPEN pin cannot be left floating.

IADMON Current Report and /ALERT pin

The APL3573A reports the input current to IADMON output pin. Namely, the IADMON output voltage is proportional to input current as shown as the below equation:

$V_{IADMON}=I_{VIN}*R_{SENSE}*K$

Where,
I_{VIN} is the input current flow into VIN pin.
R_{SENSE} is the sensing resistor which could either be the internal MOSFET A $R_{DS(ON)}$ or the external sense resistor, depending on how ISENN and ISENP is connected. Please refer to Typical Application Circuit.
K is a constant, which is 20.

When the event of $V_{IADMON}>V_{ALSET}$ persists over the debounce time set by the TIMER pin, the APL3573A latches / ALERT at low level.

Function Descriptions (Cont.)

IADMON Current Report and /ALERT pin (Cont.)

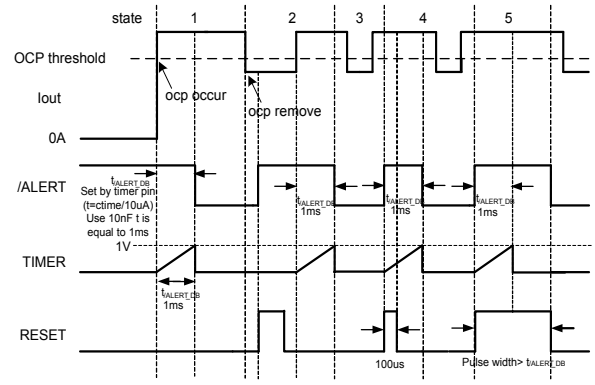
To reset /ALERT low state needs to toggle RESET pin a high level voltage whose pulse width is at least 1us. However, RESET pin can't be pulled up to high level, otherwise OCP will malfunction.The debounce time of /ALERT is set by a capacitor connected from TIMER pin to ground. The debounce time can be calculated by the following equation.

$t_{DEBOUNCE\_ALERT}=C_{TIMER}/11\mu A$

The VALSET voltage is determined by an external resistor connected from ALSET to ground. The V_{ALSET} can be calculated by the following equation.

$V_{ALSET}=10\mu A*R_{ALSET}$

State 1: When the event of $V_{IADMON}>V_{ALSET}$ persists over the debounce time set by the TIMER pin, the APL3573A latches /ALERT at low level. The diagram is as shown in figure below.
State 2: When RESET pin is a high level pulse width whose width is 1us at least, /ALERT can be released from low state to high state.
State 3: /ALERT pin keeps asserted until RESET pin is pulled high no matter of OCP occurrence.
State 4: Once the /ALERT has been asserted due to an OCP event(in state 3), another OCP event can not start the OCP delay timer until RESET assertion. /ALERT deasserts temporarily because OCP persists.
State 5: When RESET pin is a pulse width which is longer than OCP delay timer, /ALERT pin can't assert anyway. The /ALERT pin keeps in low until RESET pin deasserted. Please note that this condition is inhibited because the timing of /ALERT assertion is affected. Please don't let RESET in logic high level the time exceeds the OCP delay time, especially during an OCP event. It is suggested that RESET pin is at least 1us high pulse.

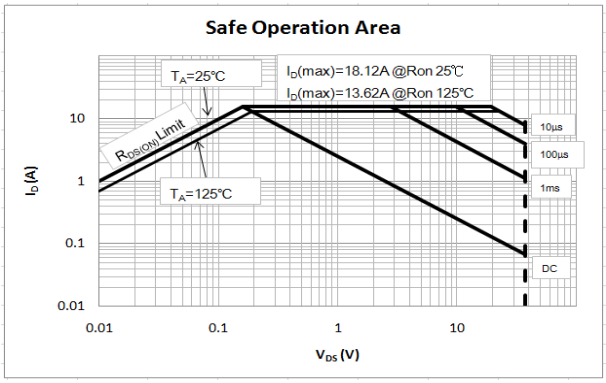


Over-Temperature Protection

When the junction temperature exceeds 150°C, the internal thermal sense circuit turns off the power FET and allows the device to cool down. When the device's junction temperature cools by 30°C, the internal thermal sense circuit will enable the device, resulting in a pulsed output during continuous thermal protection. Thermal protection is designed to protect the IC in the event of over temperature conditions. For normal operation, the junction temperature cannot exceed T_J=+125°C.

SOA of MOSFET

To provide a right Safe Operating Area (SOA) of MOSFET. SOA is define the maximum value of VDS,ID and time envelope of operation which guarantees safe operation when the MOSFET work in forward bias.



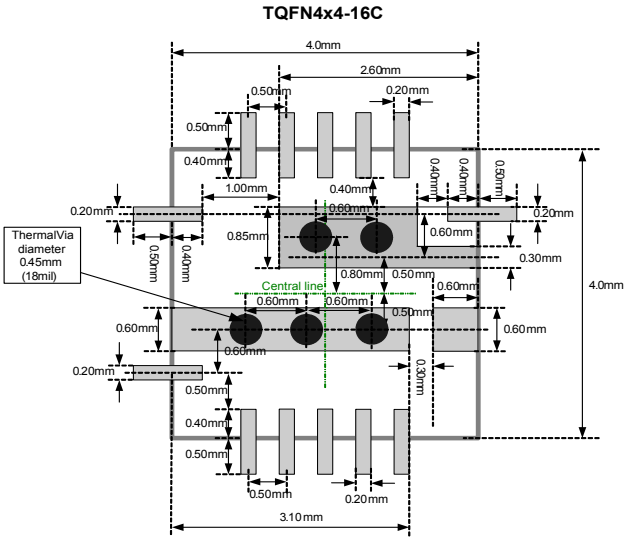
VIN Under Voltage Protection

The APL3573A uses V_{INUVP} pin to sense input voltage for under voltage protection. The internal V_{INUVP} threshold is 1V. A resistor divider from VIN to V_{INUVP} can program the VIN under voltage threshold. When V_{IN} UVP occurs, the IC will enter hiccup mode. When V_{IN} UVP event is gone, the IC can start a precharge and soft start process to raise up V_{VDRP} voltage. The V_{IN} UVP threshold must be set in accordance with following formula.

$V_{INUVP} \leq 0.86 *V_{IN\_NOMINAL}$

Where,
V_{INUVP} means the value of the under voltage threshold. For example, in an application where V_{IN}=20V, the V_{INUVP} threshold must be set not higher than 17.2V. Caution must be taken not to violate the above formula when setting V_{IN} UVP threshold, or the V_{IN} UVP may not work properly.

Recommended Minimum Footprint



Applications and Implementation

Application Information

The APL3573A is designed to enable easy configuration for monitoring adapter input current at all times. With external sensing resistor APL3573A would accurately report current through APL3573A to system via the formula, $V_{IADMON}=I_{VIN}*R_{SENSE}*K$, shown as Table 1. Besides, this device has over current protection as well when input current is more than adapter rated peak current and over current threshold could be programmable by ALSET pin. Connecting different resistance to ALSET pin could set up individual OCP threshold for different adapters.

Table 1. Input current V.S. IADMON voltage

I_VIN (A)	V_IADMON (V)
0	0
0.5	0.1
1	0.2
1.5	0.3
2	0.4
2.5	0.5
3	0.6
3.5	0.7
4	0.8
4.5	0.9
5	1.0
5.5	1.1
6	1.2
6.5	1.3
7	1.4
7.5	1.5
8	1.6
8.5	1.7
9	1.8
9.5	1.9
10	2.0
10.5	2.1
11	2.2
11.5	2.3
12	2.4

Applications and Implementation (Cont.)

Simulation Curve

Figure 1 illustrates the relation between I_VIN and V_IADMON. One could apply this relation to system for monitoring input current.

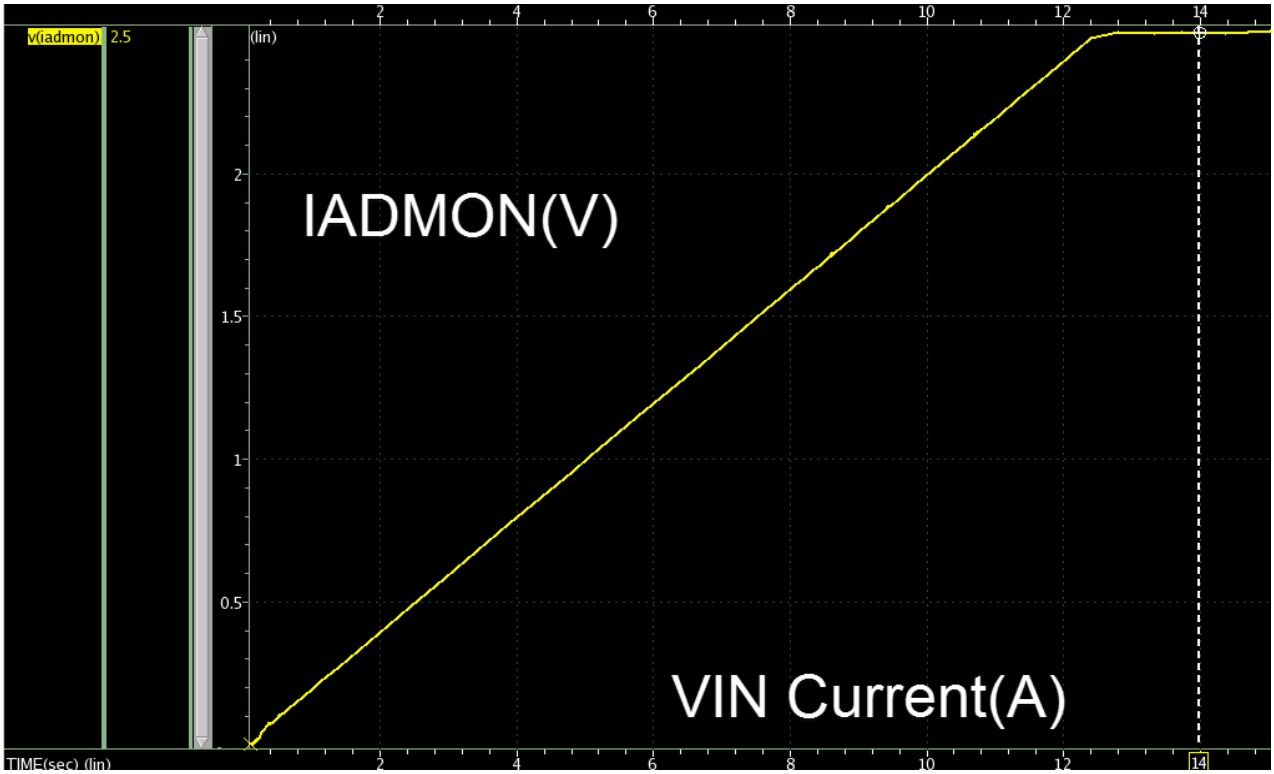


Figure 1. Simulation result of the relation between I_VIN and V_IADMON

Different ALSET resistance mapping to different adapter peak current

Table 2 shows how to design OCP threshold for different adapter. Through resistor connecting to ALSET pin, one could set up "Short circuit protection" threshold as well.

Table 2. ALSET resistance and adapter wattage

Wattage (W)	Output Voltage (Vdc)	Rating Current (A)	Peak Current (A)	R_{ALSET} (Ω)
45	20	2.25	2.7	54k
65	20	3.25	3.9	78k
90	20	4.5	5.4	108k
120	20	6.0	7.5	150k
150	20	7.5	9.0	180k
170	20	8.5	9.35	187k
180	20	9	10	200k
200	20	10	11	220k

Applications and Implementation (Cont.)

Simulation Curve (Cont.)

Figure 2 illustrates the relation between R_ALSET and I_OCP. One could apply this relation to system for monitoring input current.

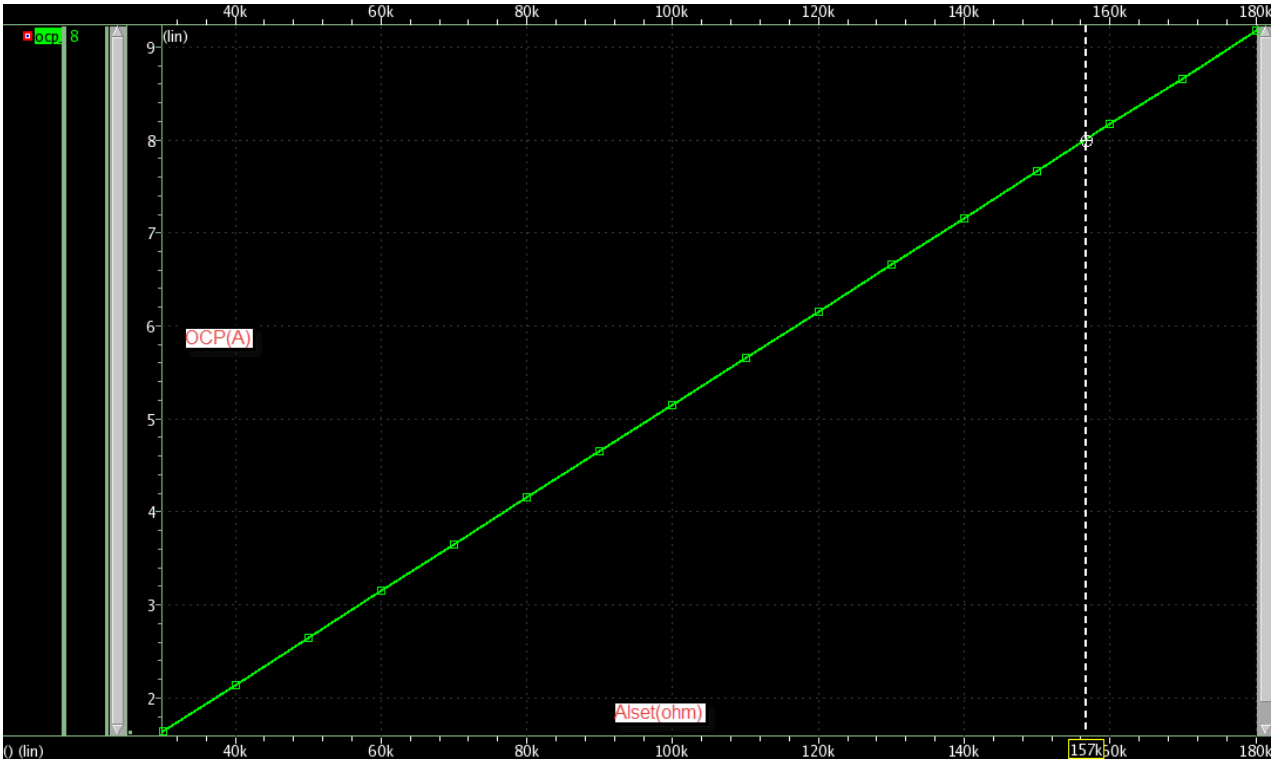


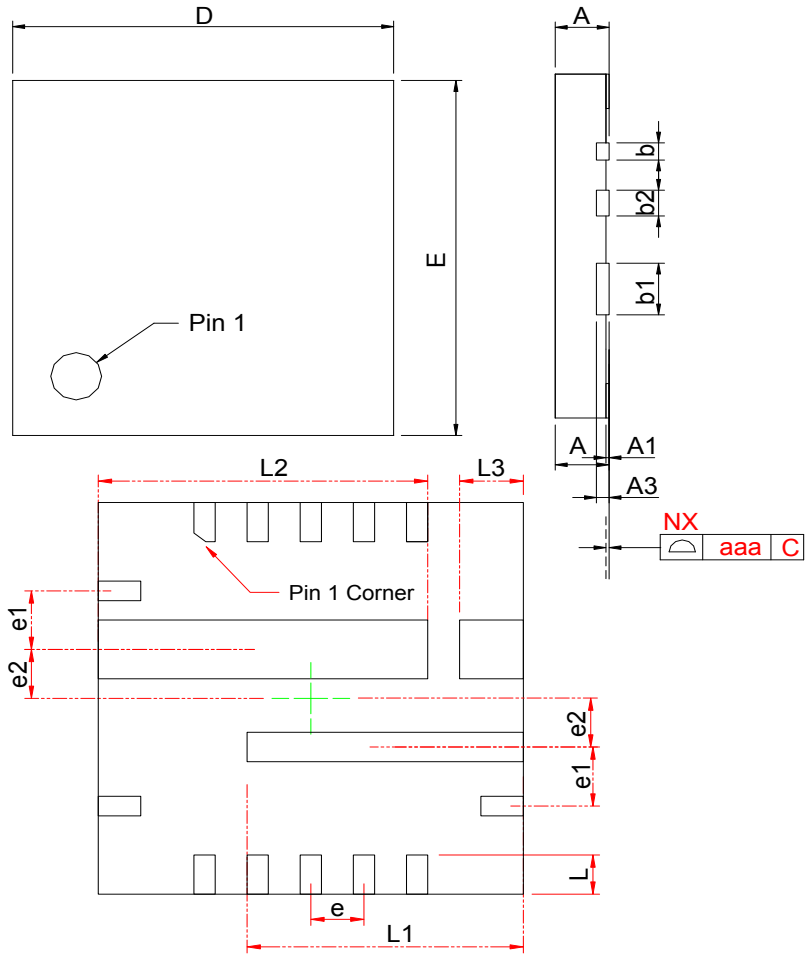
Figure 2. Simulation result of the relation between OCP threshold and R_{ALSET}

Layout Guidelines

- The input capacitors should be placed as closely as possible to APL3573A. The recommended value of input capacitor is 22μF. The additional capacitance could be added to compensate for noise made by power supply.
- The output capacitors should be placed as closely as possible to APL3573A. The recommended value of output capacitor is greater than 10μF.
- Beware of loading effect in the whole trace of IADMON to system EC. Because the IADMON has very weak driving capability, only 10nA, it is necessary to avoid EC consuming more than 10nA, otherwise current accuracy will be substantially affected.
- For great current accuracy, sensing points need to be placed at two terminals of external sensing resistor. If layout routing produces wrong sensing points, current accuracy would be not good.
- It is recommended to extend the copper area of pin 6 (GND) to an external large copper plane and to add 2~4 vias (0.45mm diameter) on this plane to enhance grounding.
- For better heat dissipation, it is recommended to put some vias in both the VDRP(pin 7) and VIN(pin 15) beneath the IC, as shown as the Recommended Minimum Footprint . Through these vias the VDPR and VIN are connected to a larger copper plane in the middle or bottom layer of PCB.

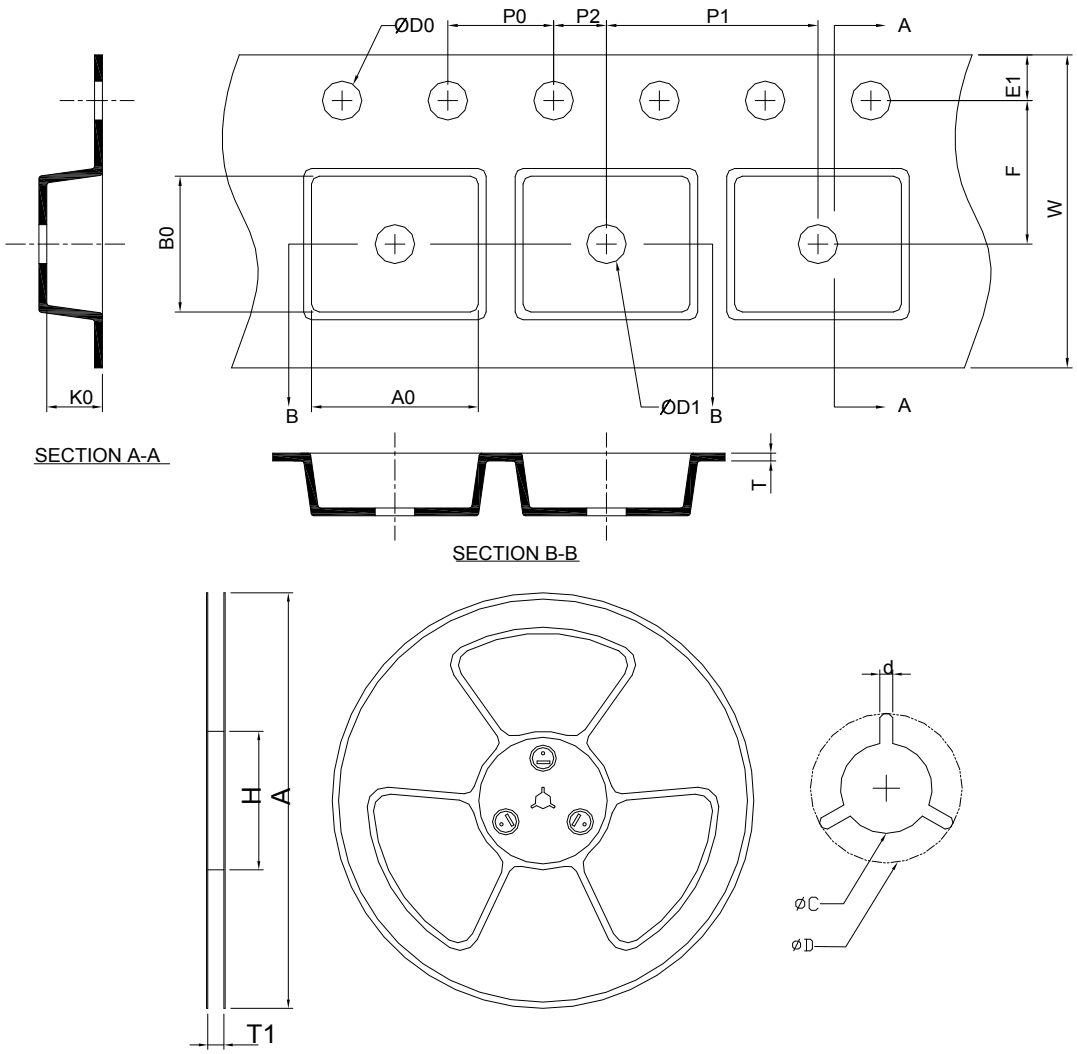
Package Information

TQFN4x4-16C



SYMBOL	TQFN4*4-16C			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.032
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.15	0.25	0.006	0.010
b1	0.55	0.65	0.022	0.026
b2	0.25	0.35	0.010	0.014
D	3.90	4.10	0.154	0.161
E	3.90	4.10	0.154	0.161
L	0.35	0.45	0.014	0.018
L1	2.50	2.70	0.098	0.106
L2	3.00	3.20	0.118	0.126
L3	0.50	0.70	0.020	0.028
e	0.50 BSC		0.020 BSC	
e1	0.60 BSC		0.024 BSC	
e2	0.50 BSC		0.020 BSC	
aaa	0.08		0.003	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFN 4x4	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	4.30±0.20	4.30±0.20	1.00±0.20

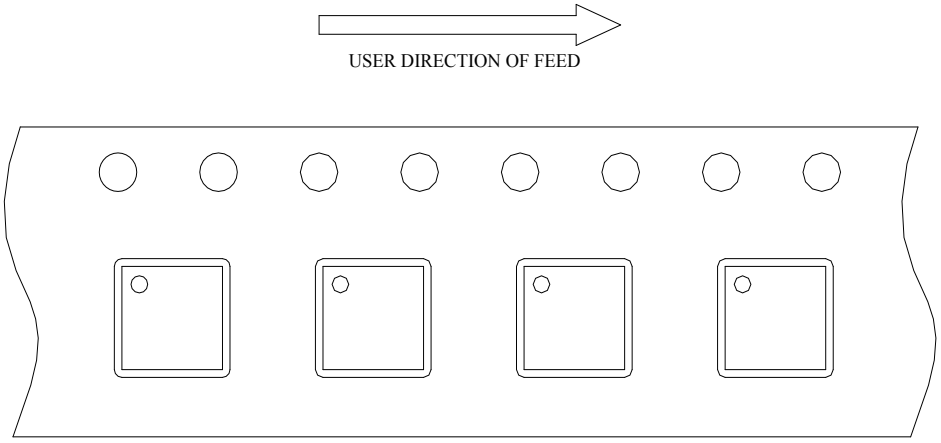
(mm)

Devices Per Unit

Application	Unit	Devices Per Reel
TQFN4*4	Tape & Reel	3000

Taping Direction Information

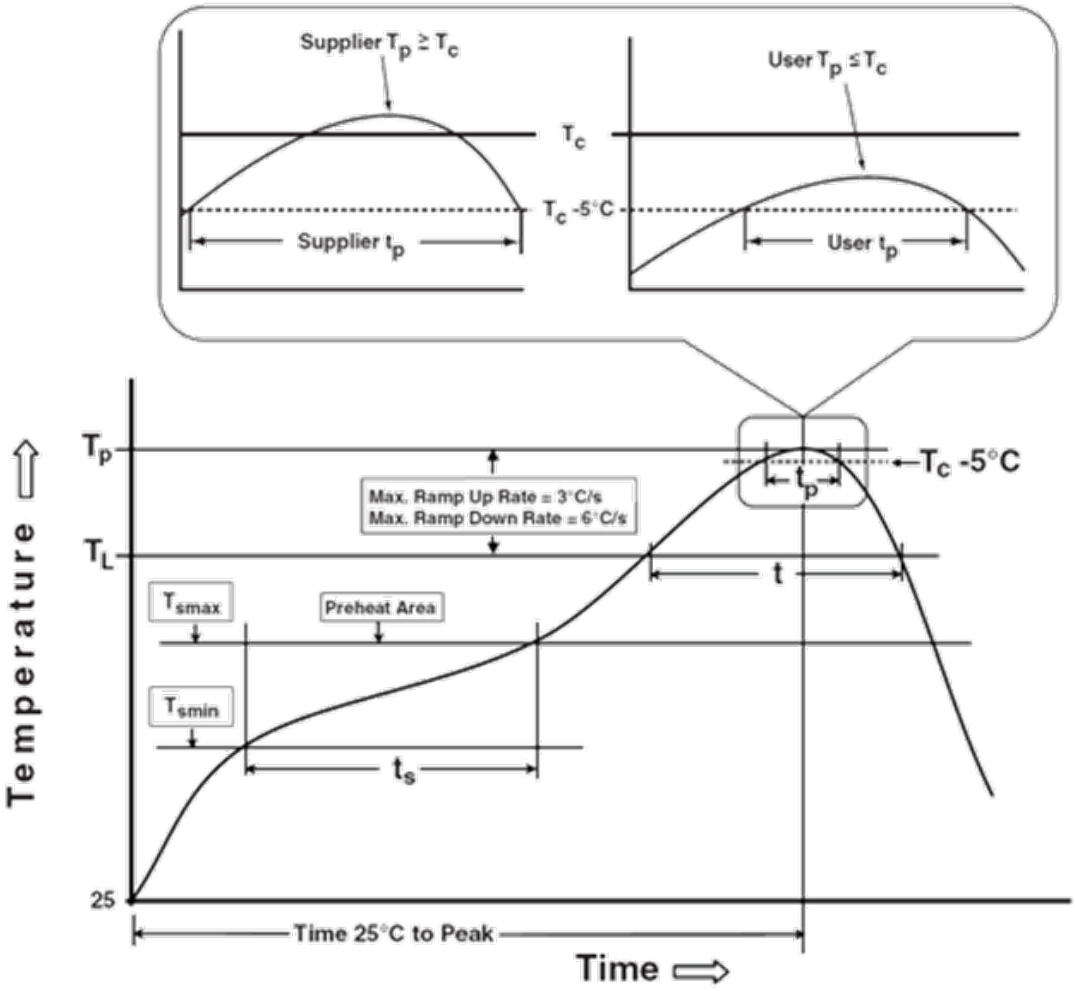
TQFN3x3-16C



Revision History

Version	Date	Revision History	
		Chapter	Description
A1	2018/9/18	-	New Release
A2	2018/10/12	-	Modify IALSET Current and add curve & waveform.
A3	2019/1/22	-	Add description to input and output capacitor. Modify IALSET Current.
A4	2019/7/18	-	Add surge protection description and measure model.
A5	2019/9/3	-	Add softstart time equation.
A6	2020/3/10	-	Add description of adapter application.

Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≧ 2KV
MM	JESD-22, A115	VMM ≧ 200V
Latch-Up	JESD 78	10ms, 1_{tr} ≧ 100mA

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