

Ultra-Low-Noise, High PSRR, Low-Dropout, 300mA Linear Regulator

Features

- **Wide Operating Voltage: 2.3V~6V**
- **Low Dropout Voltage: 290mV @ 3V/300mA**
- **Fixed Output Voltages: 1.5V~3.5V with Step 100mV, 2.85V**
- **Guaranteed 300mA Output Current**
- **High PSRR: 74dB before 10kHz**
- **Low Output Noise: 36mV_{RMS} at 100Hz to 100kHz**
- **Current-Limit Protection**
- **Controlled Short Circuit Current: 50mA**
- **Over-Temperature Protection**
- **Stable with 1mF Capacitor for Any Load**
- **Excellent Load/Line Transient**
- **SOT-23-5 and SC-70-5 Packages**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

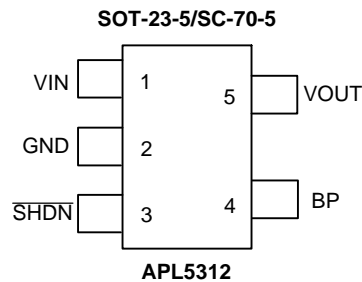
- **Cellular Phones**
- **Portable and Battery-Powered Equipment**
- **Wireless LANs**
- **GPS**

General Description

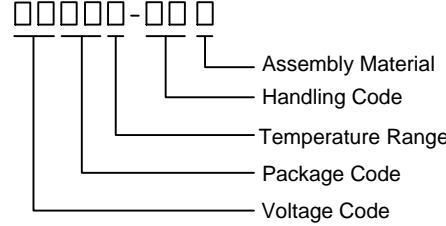
The APL5312 is an ultra low noise, low dropout linear regulator, which operates from 2.3V to 6V input voltage and delivers up to 300mA. Typical dropout voltage is only 290mV at 300mA loading. Designed for use in RF applications, the high PSRR 74dB and low noise 36mV_{RMS} makes it an ideal choice.

Design with an internal P-channel MOSET pass element, the APL5312 maintains a low supply current, independent of the load current and dropout voltage. Other features include thermal-shutdown protection and current-limit protection to ensure specified output current and controlled short-circuit current. The APL5312 regulator comes in a miniature SOT-23-5 and SC-70-5 package.

Pin Configuration



Ordering and Marking Information

<p>APL5312 □□□□□-□□□□</p>  <ul style="list-style-type: none"> □□□□□ - Assembly Material □□□□□ - Handling Code □□□□□ - Temperature Range □□□□□ - Package Code □□□□□ - Voltage Code 	<p>Package Code B : SOT-23-5 S5 : SC-70-5</p> <p>Operating Ambient Temperature Range I : -40 to 85°C</p> <p>Handling Code TR : Tape & Reel</p> <p>Voltage Code 15 : 1.5V 30 : 3.0V</p> <p>Assembly Material G : Halogen and Lead Free Device</p>
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Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020C for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Ordering and Marking Information (Cont.)

SOT-23-5 packages

Product Name	Marking	Product Name	Marking	Product Name	Marking	Product Name	Marking
APL5312-15B	339X	APL5312-16B	33AX	APL5312-17B	33BX	APL5312-18B	33CX
APL5312-19B	33DX	APL5312-20B	33EX	APL5312-21B	33FX	APL5312-22B	33GX
APL5312-23B	33HX	APL5312-24B	33IX	APL5312-25B	33JX	APL5312-26B	33KX
APL5312-27B	33LX	APL5312-28B	33MX	APL5312-29B	33NX	APL5312-30B	33OX
APL5312-31B	33PX	APL5312-32B	33QX	APL5312-33B	33RX	APL5312-34B	33SX
APL5312-35B	33TX	APL5312-285B	33dX				

SC-70-5 packages

Product Name	Marking	Product Name	Marking	Product Name	Marking	Product Name	Marking
APL5312-15S5	339	APL5312-16S5	33A	APL5312-17S5	33B	APL5312-18S5	33C
APL5312-19S5	33D	APL5312-20S5	33E	APL5312-21S5	33F	APL5312-22S5	33G
APL5312-23S5	33H	APL5312-24S5	33I	APL5312-25S5	33J	APL5312-26S5	33K
APL5312-27S5	33L	APL5312-28S5	33M	APL5312-29S5	33N	APL5312-30S5	33O
APL5312-31S5	33P	APL5312-32S5	33Q	APL5312-33S5	33R	APL5312-34S5	33S
APL5312-35S5	33T	APL5312-285S5	33d				

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{IN}, V_{OUT}	Input Voltage or Out Voltage	6.5	V
\overline{SHDN}/BP	VOUT Shutdown Control Pin/Bypass Signal Pin	6.5	V
T_J	Operating Junction Temperature	0 to 125	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_{SDR}	Maximum Lead Temperature Soldering, 10 Seconds	260	°C

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Rating	Unit
θ_{JA}	Thermal Resistance-Junction to Ambient ^(Note 2)	SOT-23-5 SC-70-5 240 325	°C/W
P_D	Power Dissipation, $T_A = 25^\circ\text{C}$ ^(Note 3)	SOT-23-5 SC-70-5 410 310	mW

Note 2 : θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Note 3 : When mounted on a (Copper foil area 50%, 45x45x1.6mm) glass epoxy board.

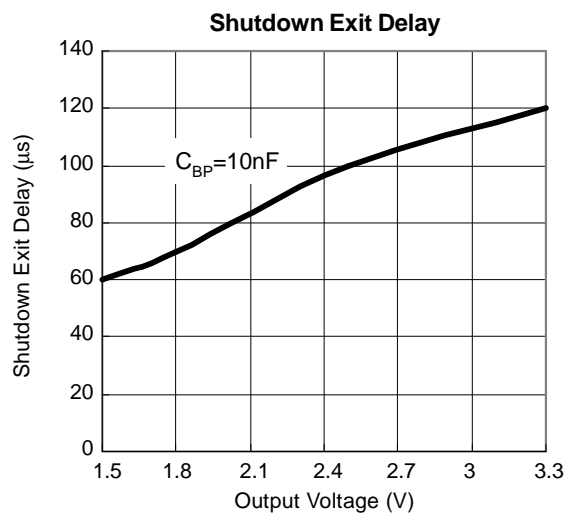
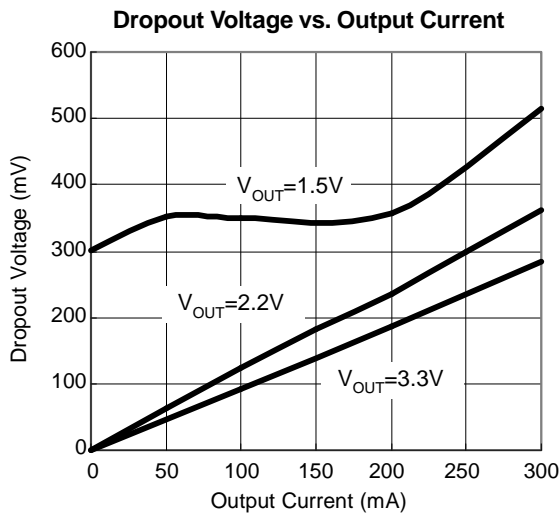
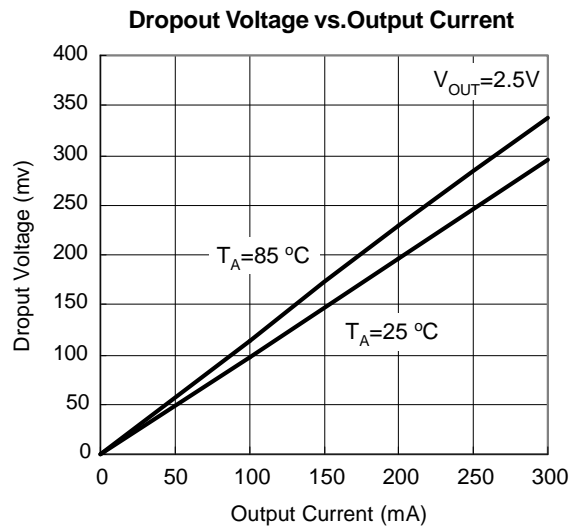
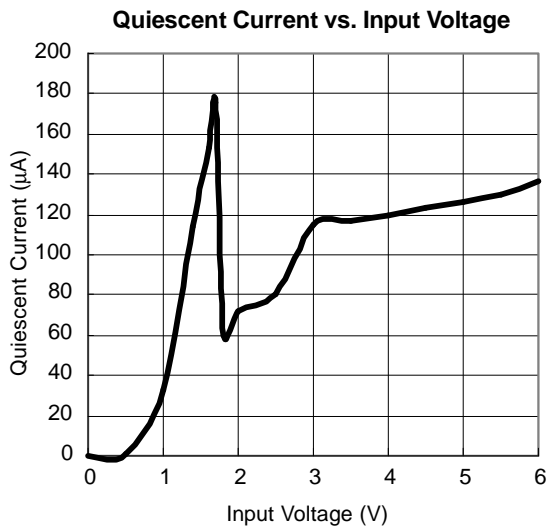
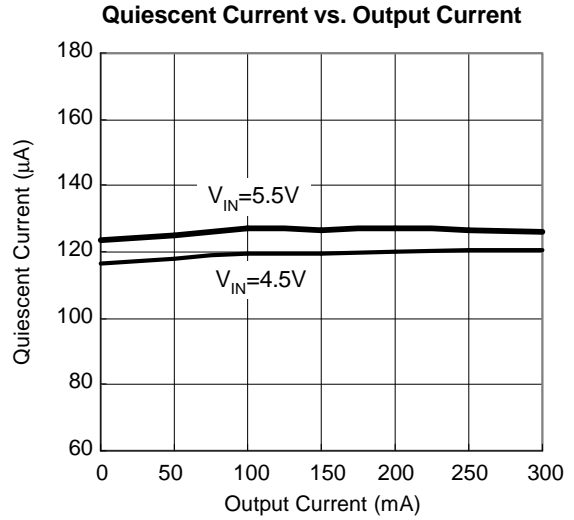
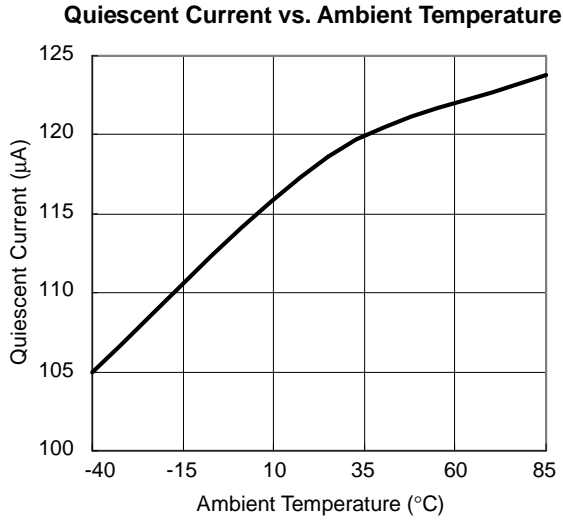
Electrical Characteristics

Unless otherwise noted these specifications apply over full temperature, $V_{IN} = V_{OUT} + 1V$, $C_{IN} = C_{OUT} = 1\mu F$, $T_A = -40$ to $85^\circ C$. Typical values refer to $T_A = 25^\circ C$.

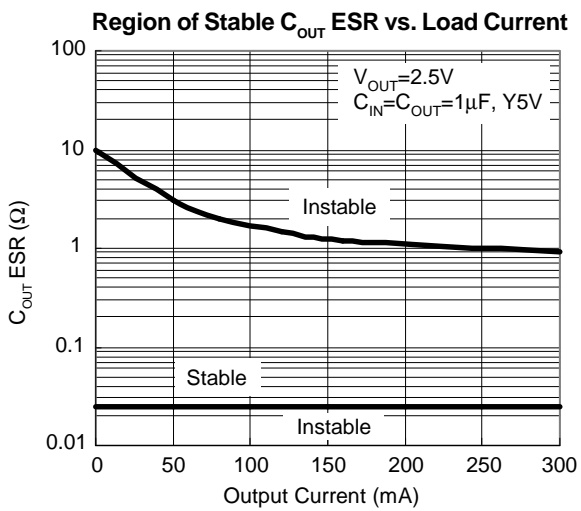
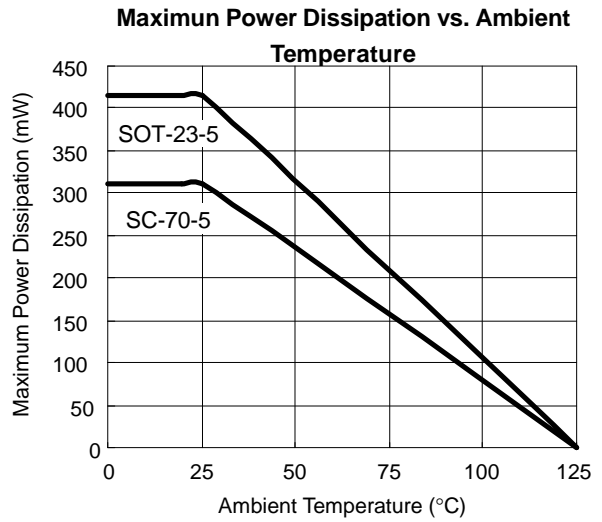
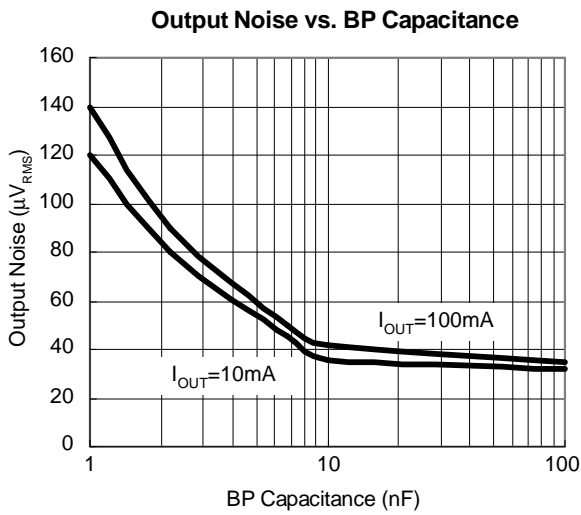
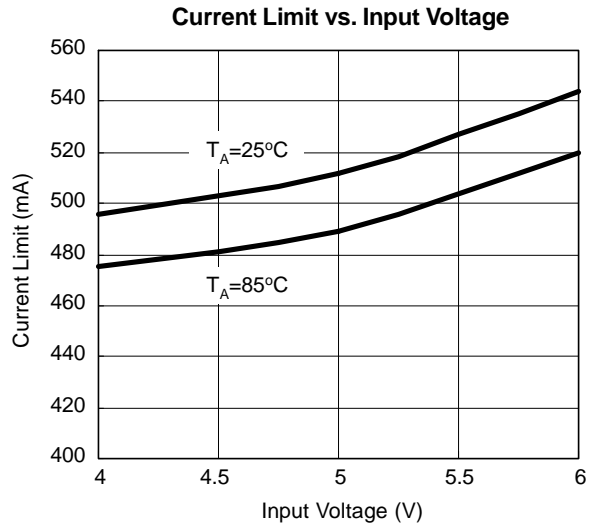
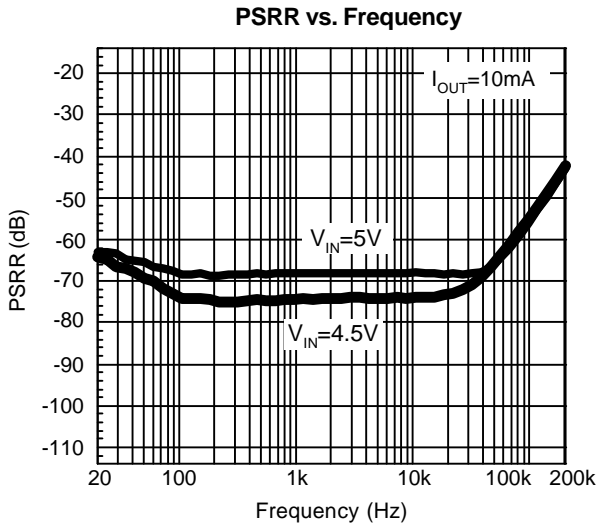
Symbol	Parameter	Test Conditions	APL5312			Unit
			Min.	Typ.	Max.	
V_{IN}	Input Voltage		2.3	-	6	V
V_{OUT}	Output Voltage Accuracy	$V_{IN} = 5V$	-2	-	2	%
	Output Voltage Range		1.5	-	3.5	V
I_{LIMIT}	Circuit Current Limit		450	500	550	mA
I_Q	Quiescent Current	$I_{OUT} = 0mA$	-	120	160	μA
		$I_{OUT} = 300mA$	-	120	160	
I_{OUT}	Load Current		-	300	-	mA
REG_{LINE}	Line Regulation	$V_{OUT} + 0.5V < V_{IN} < 6V$, $I_{OUT} = 10mA$	-	0.1	0.3	%
REG_{LOAD}	Load Regulation	$V_{IN} = V_{OUT} + 1V$, $0mA < I_{OUT} < 300mA$	-	0.8	1.5	%
V_{DROP}	Dropout Voltage ^(Note 4)	$V_{OUT} = 1.5V$, $I_{OUT} = 300mA$	-	520	680	mV
		$V_{OUT} = 2V$, $I_{OUT} = 300mA$	-	430	560	
		$V_{OUT} = 3V$, $I_{OUT} = 300mA$	-	290	380	
PSRR	Ripple Rejection	$f = 1kHz$, $C_{BP} = 10nF$, $I_{OUT} = 10mA$	-	73	-	dB
		$f = 10kHz$, $C_{BP} = 10nF$, $I_{OUT} = 10mA$	-	74	-	
		$f = 100kHz$, $C_{BP} = 10nF$, $I_{OUT} = 10mA$	-	55	-	
I_{SHORT}	Short Current	$V_{OUT} = 0V$	-	50	-	mA
	Noise	$f = 100Hz$ to $100kHz$, $C_{BP} = 10nF$, $I_{OUT} = 10mA$	-	36	-	μV_{RMS}
V_{SHDN}	High Threshold Voltage		1.6	-	$V_{IN} + 0.3$	V
	Low Threshold Voltage		-0.3	-	0.4	
I_{SHDN}	Shutdown Input Bias Current	$V_{SHDN} = V_{IN}$	-	0.1	1	μA
I_{QSHDN}	Shutdown Supply Current	$\overline{SHDN} = LOW$, $V_{IN} = V_{OUT} + 1V$	-	0.1	1	μA
T_{EXIT}	Shutdown Exit Delay	$V_{OUT} = 90\%$, $R_{LOAD} = 50\Omega$	-	100	-	μS
OTS	Over Temperature Shutdown		-	160	-	$^\circ C$
	Over Temperature Shutdown Hysteresis		-	20	-	$^\circ C$
TC	Output Voltage Temperature Coefficient	$T_J = -40 \sim 125^\circ C$	-	100	-	ppm/ $^\circ C$
C_{OUT}	Output Capacitor		-	1	-	μF
	ESR		0.025	-	1	Ω

Note 4 : Dropout voltage definition: $V_{IN} - V_{OUT}$ when V_{OUT} is 2% below the value of V_{OUT} for $V_{IN} = V_{OUT} + 1V$.

Typical Operating Characteristics

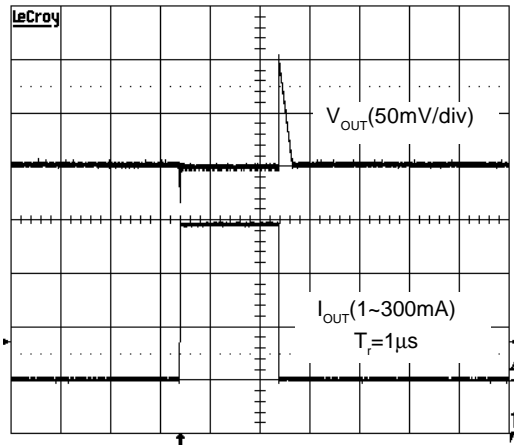


Typical Operating Characteristics (Cont.)



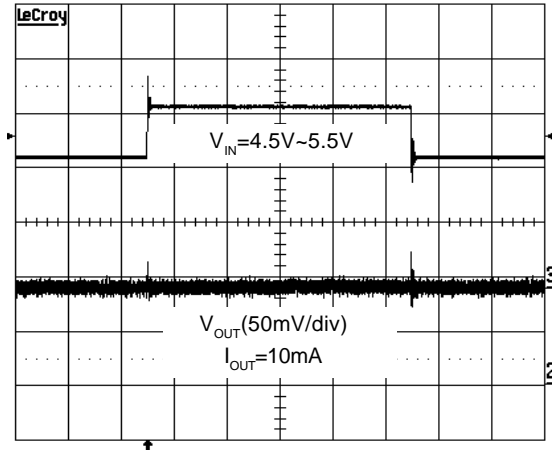
Typical Operating Characteristics (Cont.)

Load Transient



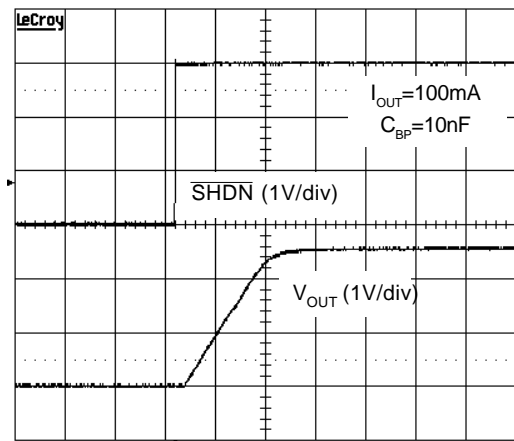
Time (0.1ms/div)

Line Transient



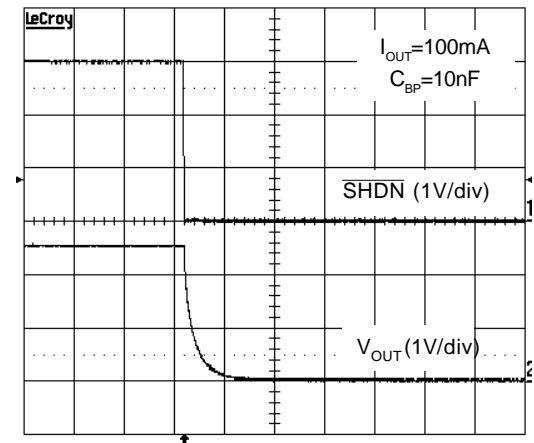
Time (0.1ms/div)

Exiting Shutdown Waveform



Time (50µs/div)

Entering Shutdown Delay

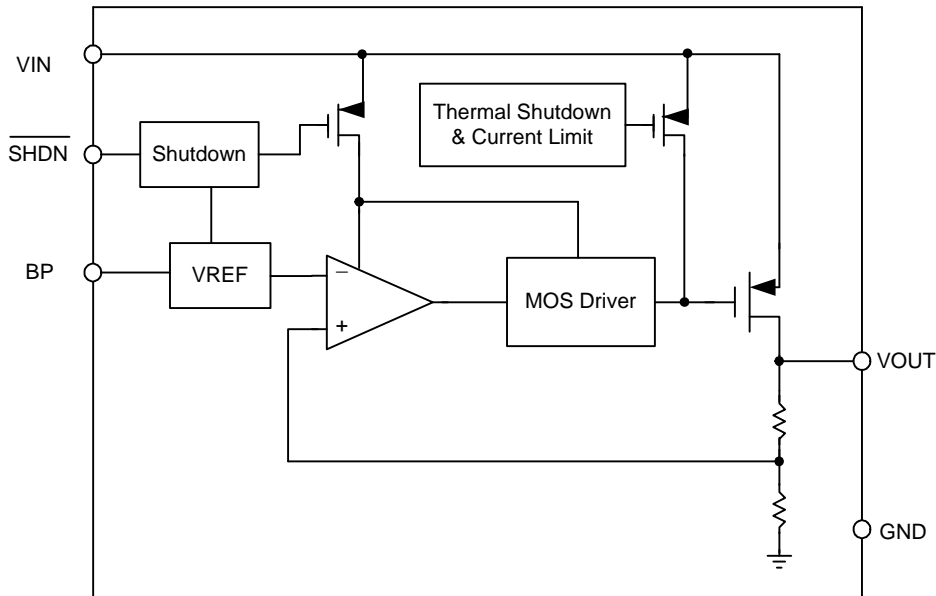


Time (0.1ms/div)

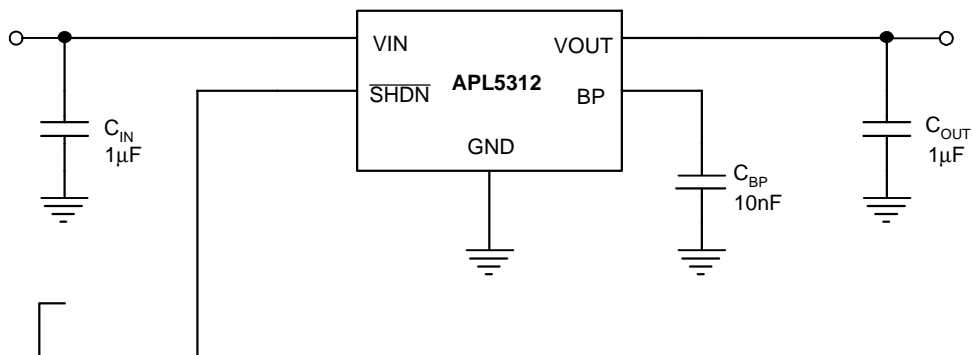
Pin Description

PIN		I/O	FUNCTION
NO.	NAME		
1	VIN	I	Voltage supply input pin
2	GND		GND pin
3	SHDN	I	Shutdown control pin, low = off, high = normal
4	BP	I	Bypass signal pin in fixed output type device
5	VOUT	O	Regulator output pin

Block Diagram



Typical Application Circuit



Application Information

Output Voltage Selection

The APL5312 are supplied with factory-set output voltages from 1.5V to 3.5V.

Capacitor Selection and Regulation Stability

The APL5312 uses at least a 1 μ F capacitor on the input. This capacitor can use Aluminum, Tantalum, or Ceramic capacitors. Input capacitor with large value and low ESR provides better PSRR and line-transient response. The output capacitor also can use Aluminum, Tantalum, or Ceramic capacitor, and its proper values is at least 1 μ F, ESR must be above 25m Ω . Large output capacitor values can reduce noise and improve load-transient response, stability, and PSRR. With X5R and Y5V dielectrics, 1 μ F is sufficient at all operating temperatures. The selection of output capacitor's is important because it with C_{OUT} form a zero to provide the sufficient phase margin (see the Figure C_{OUT} ESR vs. Load Current).

Bypass Capacitor

Use a 10nF bypass capacitor at BP for low-output voltage noise. The leakage current going into the BP pin should be less than 10nA. Increasing the capacitance slightly decreases the output noise. Value above 0.1 μ F and below 1nF are not recommended (see the Figure Output Noise vs. BP Capacitance).

Noise, PSRR, and Load-Transient Response

The APL5312 is designed to deliver ultra-low noise and high PSRR, as well as low dropout and low quiescent currents in battery-powered systems. When operating from sources other than batteries, improve PSRR and transient response can be achieved by increasing input and output capacitors, and bypass capacitor to form the passive filtering techniques (see Output Noise vs. BP Capacitance).

Shutdown

The APL5312 has an active high enable function. Force $\overline{\text{SHDN}}$ high (>1.6V) enables the V_{OUT}, $\overline{\text{SHDN}}$ low (<0.4V) disables the V_{OUT}. Enter the shutdown mode, it also causes the output voltage to discharge through a 500 Ω resistance to ground. In shutdown mode, the quiescent cur-

rent can reduce to 0.1 μ A. The $\overline{\text{SHDN}}$ pin cannot be floating, a floating $\overline{\text{SHDN}}$ pin may cause an indeterminate state on the output. If it is no use, connect to V_{IN} for normal operation.

Input-Output (Dropout) Voltage

The minimum input-output voltage differential (dropout) determines the lowest usable supply voltage. The dropout voltage is a function of drain-to-source on resistance multiplied by the load current.

Current Limit

APL5312 includes a current-limit circuitry for linear regulator. The current-limit protection, which senses the current flowing to the P-channel MOSFET, and controls the output voltage. The point where limiting occurs is I_{OUT}=500mA. The output can be shortened to the ground for an indefinite amount of time without damaging to the part.

Thermal Protection

Thermal protection limits total power dissipation in the APL5312. When the junction temperature exceeds +160 $^{\circ}$ C, the thermal sensor generates a logic signal to turn off the pass element and let IC to cool. When the IC's junction temperature cools down by 20 $^{\circ}$ C, the thermal sensor will turn the pass element on again, resulting in a pulsed output during continuous thermal protection. Thermal protection is designed to protect the IC in the event of fault conditions.

Operating Region and Power Dissipation

The thermal resistance of the case and circuit board, ambient and junction air temperature, and the rate of air flow all control the APL5312's maximum power dissipation. The power dissipation across the device is $P = I_{\text{OUT}}(V_{\text{IN}} - V_{\text{OUT}})$. The maximum power dissipation is:

$$P_{\text{MAX}} = (T_{\text{J}} - T_{\text{A}}) / (\theta_{\text{JC}} + \theta_{\text{CA}})$$

$$\theta_{\text{JA}} = \theta_{\text{JC}} + \theta_{\text{CA}}$$

where $T_{\text{J}} - T_{\text{A}}$ is the temperature difference between the junction and ambient air.

θ_{JC} is the thermal resistance of the package, θ_{CA} is the thermal resistance through the printed circuit board, copper traces, and other materials to the surrounding air, θ_{JA}

Application Information (Cont.)

Operating Region and Power Dissipation (Cont.)

is the thermal resistance between Junction and ambient air. For continual operation, do not exceed the absolute maximum junction Temperature rating of $T_j = 125^\circ\text{C}$.

For example:

The SOT-23-5 package has maximum power dissipation 300mW at $T_A = 55^\circ\text{C}$, relatively 225mW at SC-70-5 package (see Maximum Power Dissipation vs. Ambient Temperature).

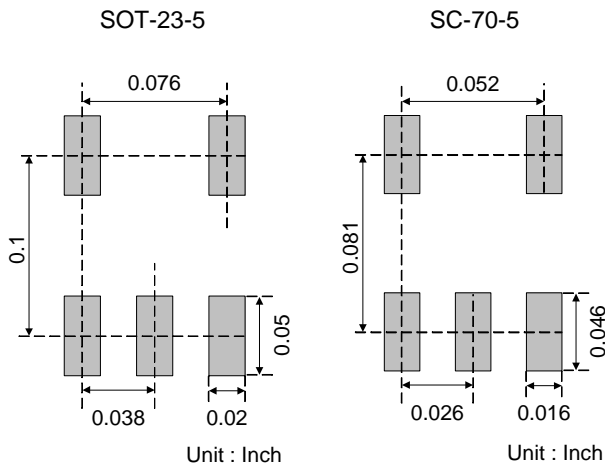
$$V_{IN} = 5\text{V}, I_{OUT} = 250\text{mA}, V_{OUT} = 3.3\text{V},$$

$$P_D = (5-3.3)\text{V} \times 150\text{mA} = 255\text{mW}$$

According to the power dissipation issue, we should adapt the SOT-23-5 package. It could reduce the thermal resistance to maintain the IC longer life.

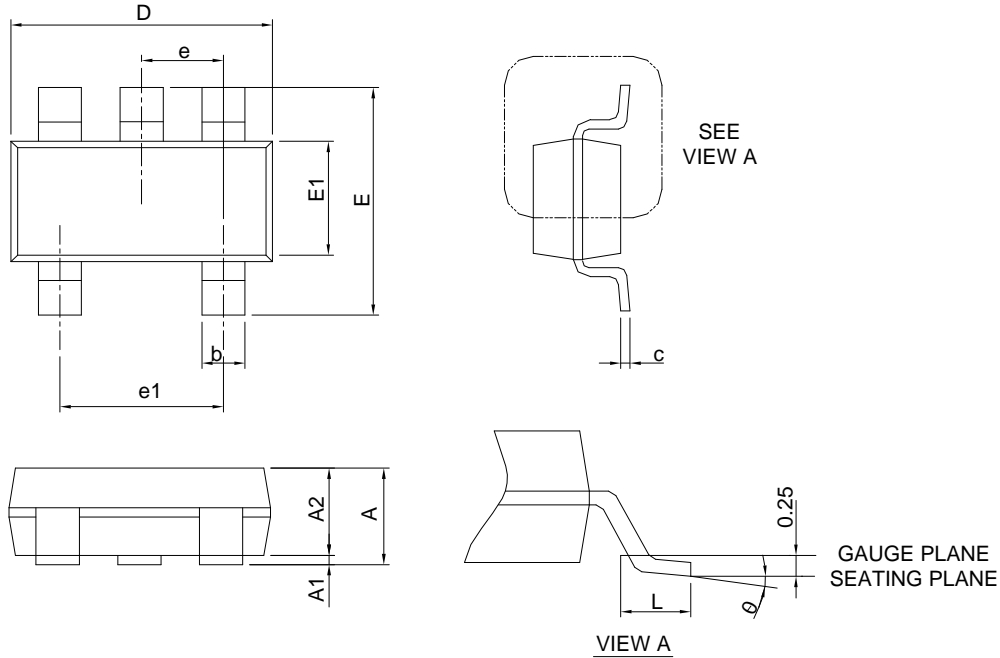
The GND pin provides an electrical connection to the ground and channeling heat away. The printed circuit board (PCB) forms a heat sink and dissipates most of the heat into ambient air.

Recommended Minimum Footprint



Package Information

SOT-23-5



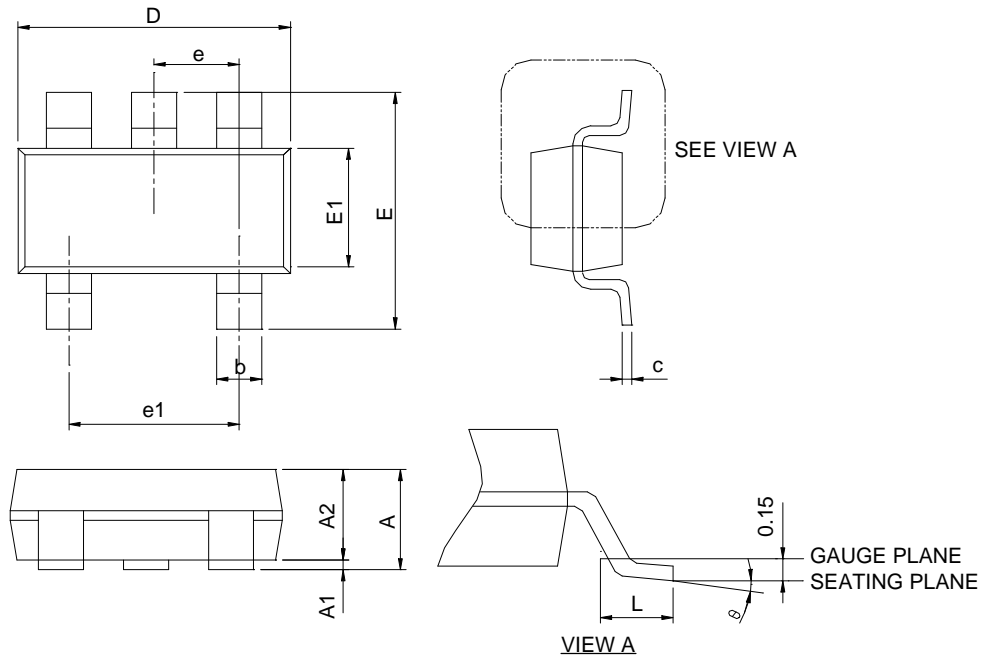
SYMBOL	SOT-23-5			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.45		0.057
A1	0.00	0.15	0.000	0.006
A2	0.90	1.30	0.035	0.051
b	0.30	0.50	0.012	0.020
c	0.08	0.22	0.003	0.009
D	2.70	3.10	0.106	0.122
E	2.60	3.00	0.102	0.118
E1	1.40	1.80	0.055	0.071
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

Note : 1. Follow JEDEC TO-178 AA.

2. Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.

Package Information

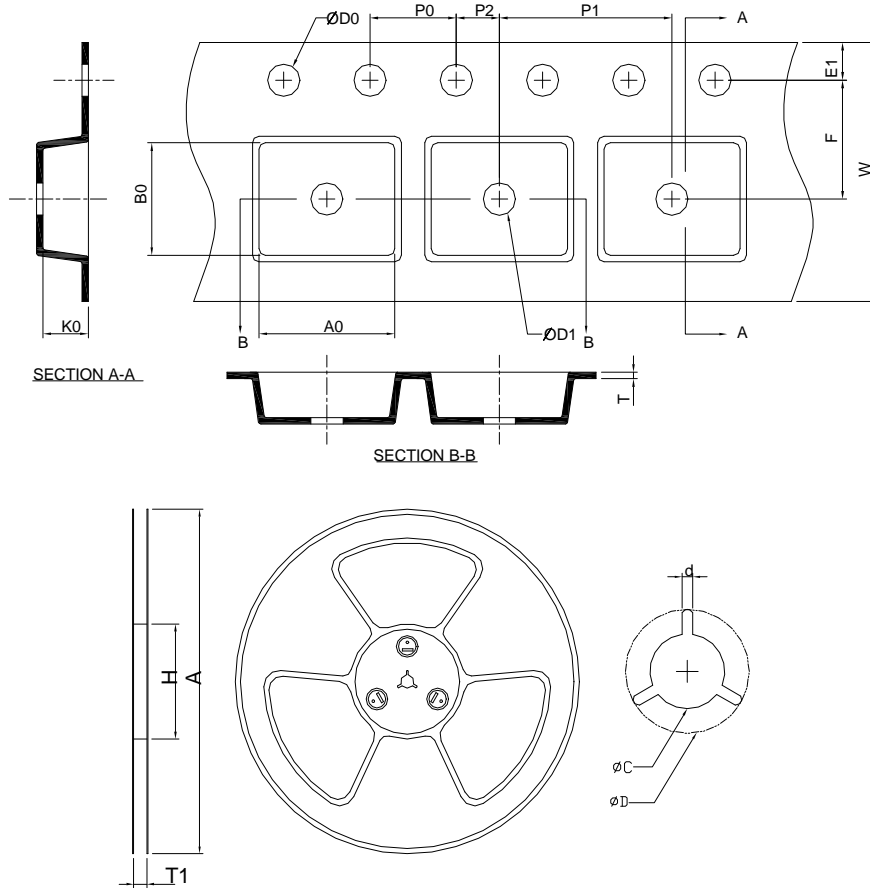
SC-70-5



SYMBOL	SC-70-5			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.80	1.10	0.031	0.043
A1	0.00	0.10	0.000	0.004
A2	0.80	1.00	0.031	0.040
b	0.15	0.30	0.006	0.012
c	0.08	0.25	0.003	0.010
D	1.90	2.20	0.075	0.087
E	2.00	2.40	0.079	0.095
E1	1.15	1.35	0.045	0.053
e	0.65 BSC		0.026 BSC	
e1	1.30 BSC		0.051 BSC	
L	0.15	0.45	0.006	0.018
θ	0°	8°	0°	8°

Note : 1. Followed from JEDEC MO-223 AB.
 2. Dimension D and E1 do not include mold flash, protrusions or gate burrs.
 Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
SOT-23-5	178.0 ±0.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0 ±0.30	1.75 ±0.10	3.5 ±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0 ±0.10	4.0 ±0.10	2.0 ±0.05	1.5+0.10 -0.00	1.0 MIN.	0.6+0.00 -0.40	3.20 ±0.20	3.10 ±0.20	1.50 ±0.20
Application	A	H	T1	C	d	D	W	E1	F
SC-70-5	178.0 ±0.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0 ±0.30	1.75 ±0.10	3.50 ±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0 ±0.10	4.0 ±0.10	2.0 ±0.05	1.5+0.10 -0.00	1.00 MIN.	0.6+0.00 -0.40	2.40 ±0.20	2.40 ±0.20	1.20 ±0.20

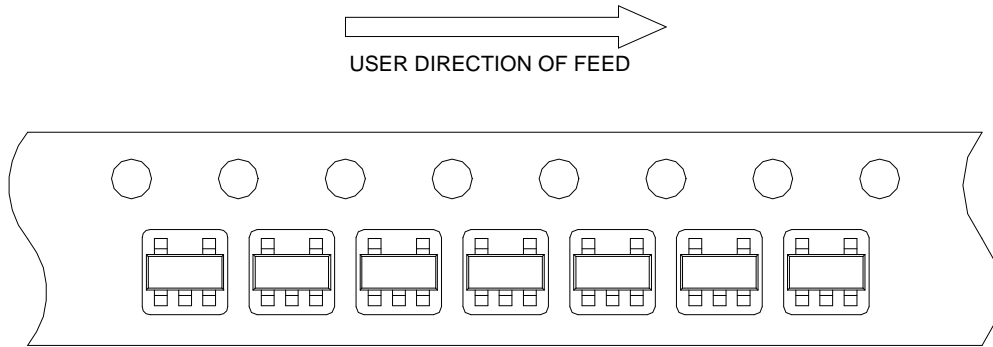
(mm)

Devices Per Unit

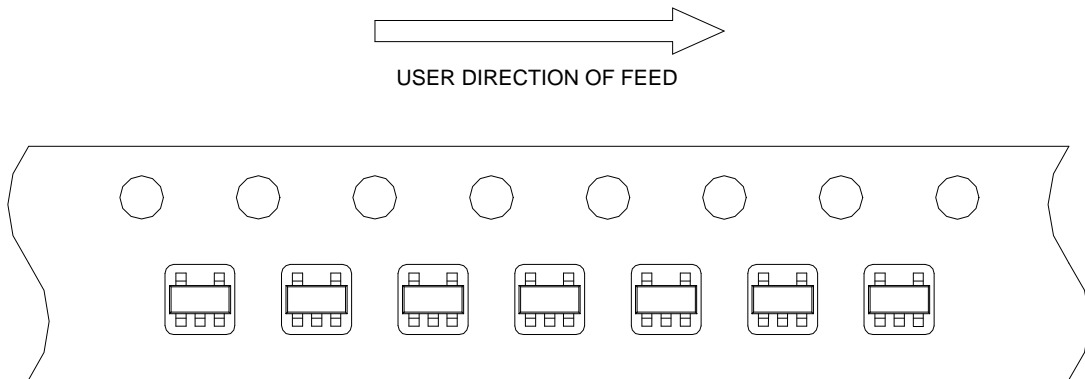
Package Type	Unit	Quantity
SOT-23-5	Tape & Reel	3000
SC-70-5	Tape & Reel	3000

Taping Direction Information

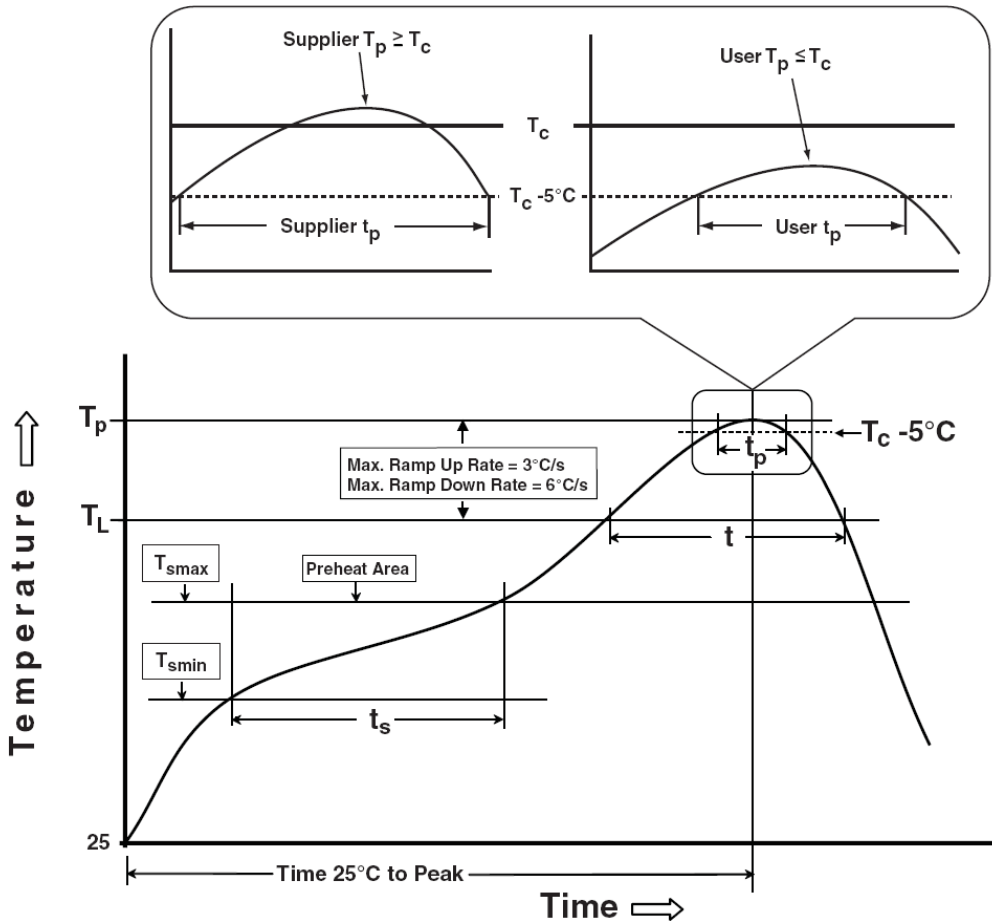
SOT-23-5



SC-70-5



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak		
Temperature min (T_{smin})	100 °C	150 °C
Temperature max (T_{smax})	150 °C	200 °C
Time (T_{smin} to T_{smax}) (t_s)	60-120 seconds	60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L)	183 °C	217 °C
Time at liquidous (t_l)	60-150 seconds	60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_p)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.

* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum.
 ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.

Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm ³ <350	Volume mm ³ ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm ³ <350	Volume mm ³ 350-2000	Volume mm ³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ 125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM 2KV
MM	JESD-22, A115	VMM 200V
Latch-Up	JESD 78	10ms, 1 _r 100mA

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