Dual Input 2A Low Dropout Regulator

Features

- Fast Transient Response
- High Output Accuracy
  - ±20mV over Load, Output Voltage Offset and Temperature
- Adjustable Output Voltage by External Resistors
- Current-Limit Protection
- On-Chip Thermal Shutdown
- Shutdown for Standby or Suspend Mode
- Simple SOP-8 and SOP-8 with Thermal Pad Packages
- Lead Free Available (RoHS Compliant)

Applications

- VGA Card Power
- Chip Set Power

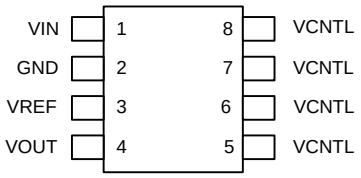
General Description

The APL5330 integrates a power transistor to provide regulated voltage with maximum output current of 2A. It also incorporates current-limit, thermal shutdown and shutdown control functions into a single chip.

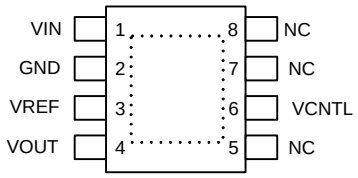
The current-limit circuit limits the maximum output current in overload or short-circuit conditions.

The on-chip thermal shutdown provides protection against any combination of overload that would create excessive junction temperature. The output voltage of the APL5330 tracks the reference voltage on VREF pin. A resistor divider connected to VREF pin is usually used to provide reference voltage to the IC. In addition, an external ceramic capacitor and an open-drain transistor connected to VREF pin provides soft-start and shutdown control. Applying and holding a voltage below 0.35V (typ.) to VREF shuts off the output.

Pin Configuration



SOP-8 (Top View)



SOP-8-P (Top View)

NC = No internal connection

= Thermal Pad

(connected to GND plane for better heat dissipation)

Ordering and Marking Information

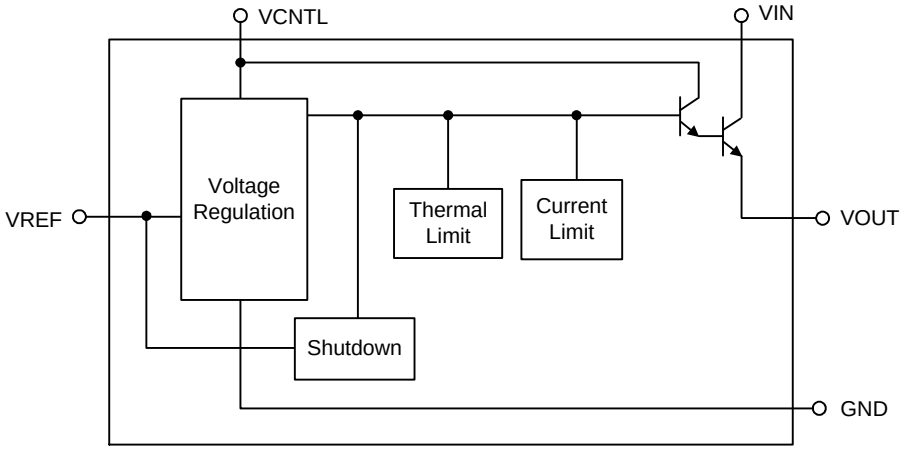
APL5330 □□□-□□□ Lead Free Code Handling Code Temp. Range Package Code	Package Code K : SOP-8 KA : SOP-8-P Operating Ambient Temp. Range E : -20 to 70 °C Handling Code TR : Tape & Reel Lead Free Code L : Lead Free Device Blank : Original Device
APL5330KE-TR : APL5330KAE-TR : APL5330 XXXXX	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS and compatible with both SnPb and lead-free soldiering operations. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J STD-020C for MSL classification at lead-free peak reflow temperature.

Pin Description

PIN NAME	I/O	DESCRIPTION
VIN	I	Main power input pin. Connect this pin to a voltage source and an input capacitor. The APL5330 provides current from VIN pin to VOUT pin by controlling the NPN pass transistor.
GND	O	Signal ground.
VCNTL	I	Power input pin for internal control circuitry. Connect this pin to a voltage source to provide a bias for the internal control circuitry. A bypass capacitor is usually connected near this pin.
VREF	I	Reference voltage input and active-low shutdown control pin. Connect this pin to a resistor divider and a capacitor for soft-start and filtering noise purposes. Pulling and holding the voltage on this pin low by an open-drain transistor shuts down the output.
VOUT	O	Output pin of the regulator. Connect this pin to load. Output capacitors connected to this pin improves stability and transient response. The output voltage tracks the reference voltage, and the output pin provides the maximum current up to 2A.

Block Diagram



Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CNTL}	VCNTL Supply Voltage, VCNTL to GND	-0.2 ~ 7	V
V_{IN}	VIN Supply Voltage, VIN to GND	-0.2 ~ 3.9	V
P_D	Power Dissipation	Internally Limited	W
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Soldering Temperature, 10 Seconds	300	°C
V_{ESD}	Minimum ESD Rating (Human Body Mode)	±3	kV

Thermal Characteristics

Symbol	Parameter	Value	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance in Free Air SOP-8 SOP-8-P	 75 55	°C/W
θ_{JC}	Junction-to-Case Thermal Resistance SOP-8 SOP-8-P	 28 20	°C/W

Note : θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of SOP-8-P is soldered directly on the PCB.

Recommended Operating Conditions

Symbol	Parameter	Range	Unit
V_{CNTL}	VCNTL Supply Voltage (Note 1)	3.1 ~ 6	V
V_{IN}	VIN Supply Voltage (Note 2)	1.2 ~ 3.5	V
V_{REF}	VREF Input Voltage	0.8 ~ 3	V
V_{OUT}	VOUT Output Voltage (Note 3)	V_{REF} ± 0.02	V
I_{OUT}	VOUT Output Current (Note 4)	2	A
T_J	Junction Temperature	-20 ~ 125	°C

Notes :

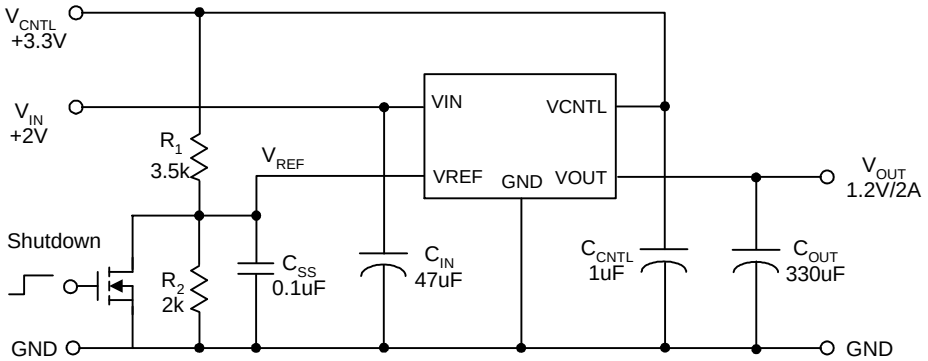
1. Please refer to the VCNTL-to-Vin Dropout Voltage in the “Typical Characteristics” section for the minimun supply voltage on VCNTL.
2. Please supply enough voltage to VIN for providing desired maximum output current. Please refer to the VIN. Dropout Voltage vs Output Current in the Typical Characteristics.
3. The VOUT is regulated to the V_{REF} with additional voltage offset and load regulation except over-load conditions.
4. The maximum I_{OUT} varies with the T_J and the voltages of V_{IN}-V_{OUT} and V_{OUT}.

Electrical Characteristics

Refer to the typical application circuit. These specifications apply over V_{CNTL} = 3.3V, V_{IN} = 2V, V_{REF} = 1.2V and T_A = -20 to 70°C, unless otherwise specified. Typical values are at T_A = 25°C.

Symbol	Parameter	Test Conditions	APL5330			Unit
			Min	Typ	Max	
OUTPUT VOLTAGE						
V_{OUT}	VOUT Output Voltage	I_{OUT} = 0A		V_{REF}		V
	System Accuracy	Over temperature, V_{OUT} offset, and load regulation	-20		20	mV
	Load Regulation	I_{OUT} = 10mA to 2A	-8	-3		mV
	V_{IN} Dropout Voltage	I_{OUT} = 2A		0.47	0.7	V
PROTECTION						
I_{LIM}	Current Limit	T_J = 25°C T_J = 125°C	2.4	2.7 2.6		A
T_{SD}	Thermal Shutdown Temperature	Rising T_J		170		°C
	Thermal Shutdown Hysteresis			30		°C
INPUT CURRENT						
I_{CNTL}	VCNTL Supply Current	I_{OUT} = 0A	0.5	2	4	mA
		I_{OUT} = 2A (Normal Operation)		25	50	
		VREF = GND (Shutdown)		0.3		
I_{VREF}	VREF Bias Current (The current flows out of VREF)	Normal operation		150	500	nA
		VREF = GND (Shutdown)		300	5000	
SHUTDOWN CONTROL						
	Shutdown Voltage Threshold		0.2	0.35	0.65	V

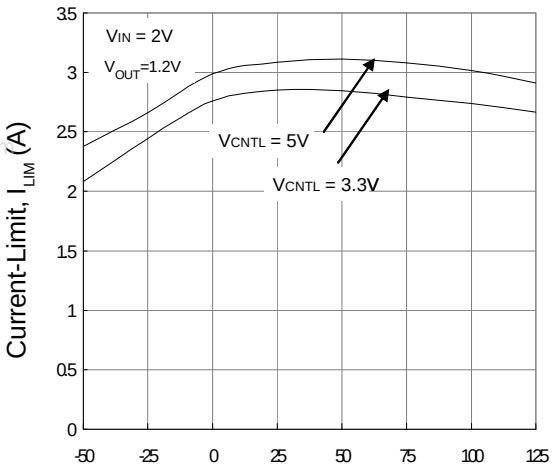
Typical Application Circuit



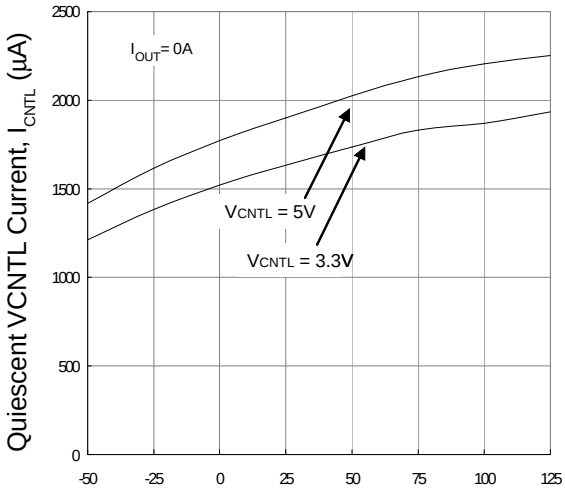
$$V_{OUT} = V_{REFIN} \cdot \frac{R_2}{R_1 + R_2} \quad (V)$$

Typical Characteristics

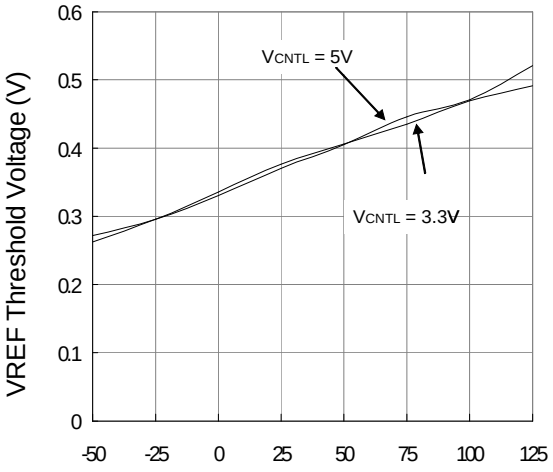
Current-Limit
vs. Junction Temperature



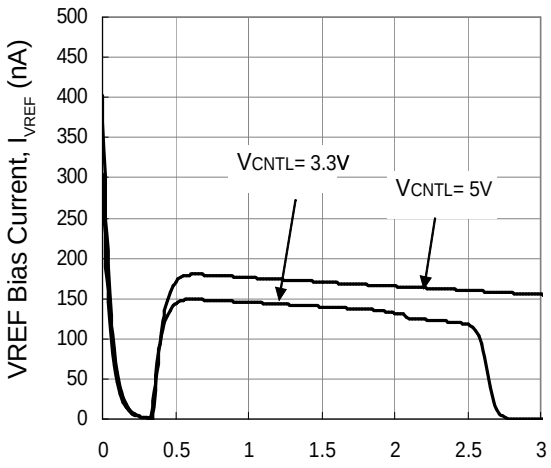
Quiescent VCNTL Current
vs. Junction Temperature



VREF Threshold Voltage
vs. Junction Temperature

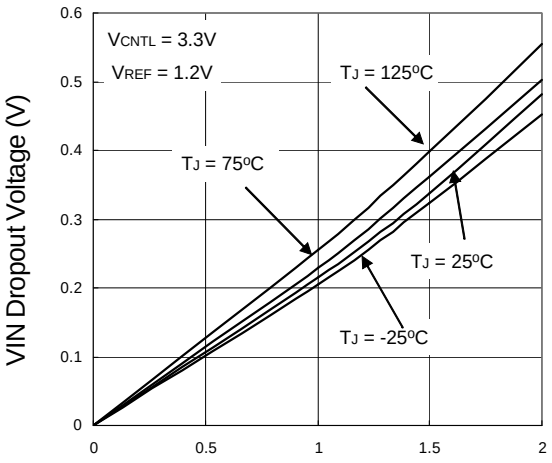


VREF Bias Current
vs. V_{REF} Supply Voltage

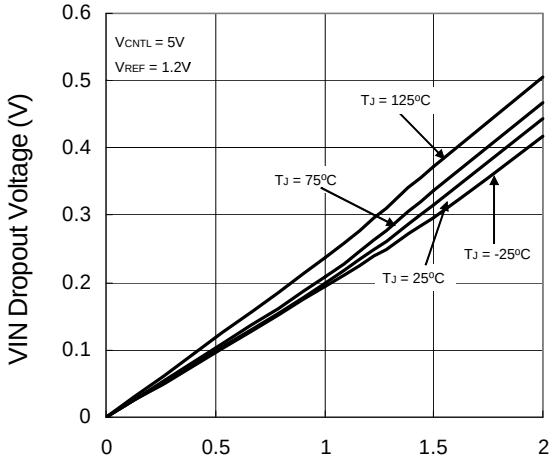


Typical Characteristics (Cont.)

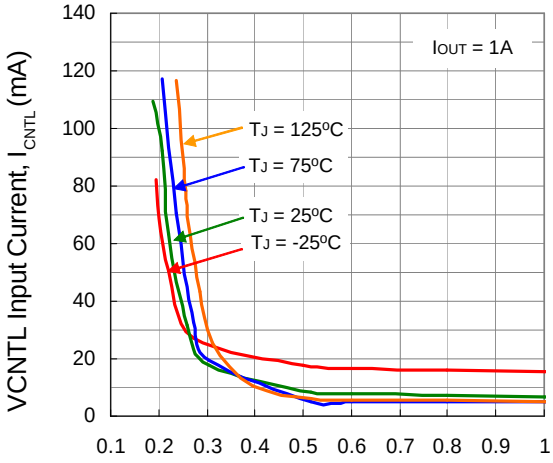
VIN Dropout Voltage
vs. Output Current



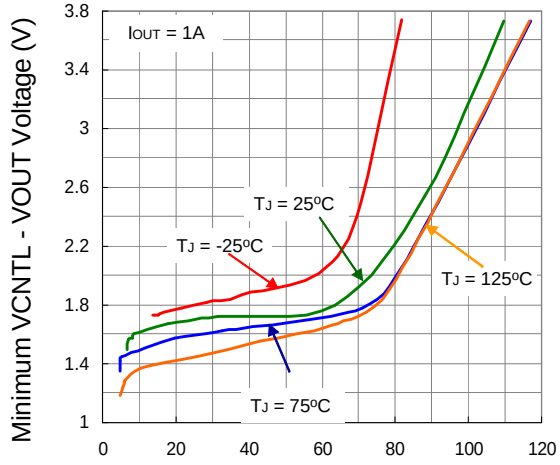
VIN Dropout Voltage
vs. Output Current



VCNTL Input Current
vs. V_{IN} - V_{OUT} Voltage at I_{OUT}=1A

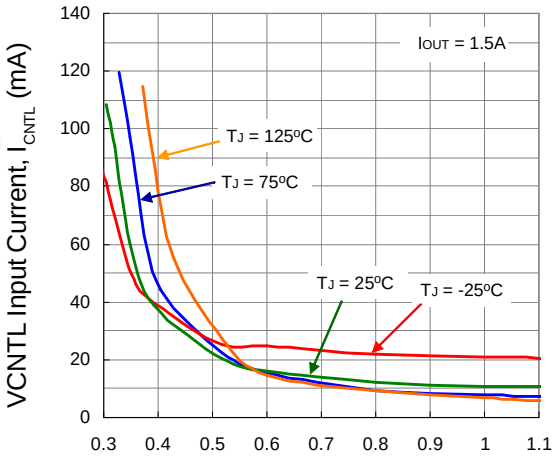


VCNTL-to-VOUT Dropout Voltage
vs. VCNTL Input Current

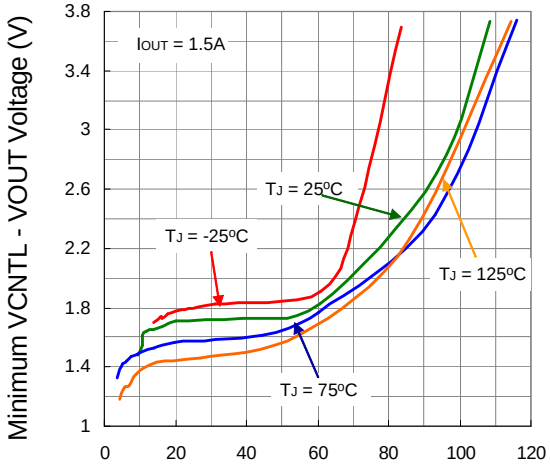


Typical Characteristics (Cont.)

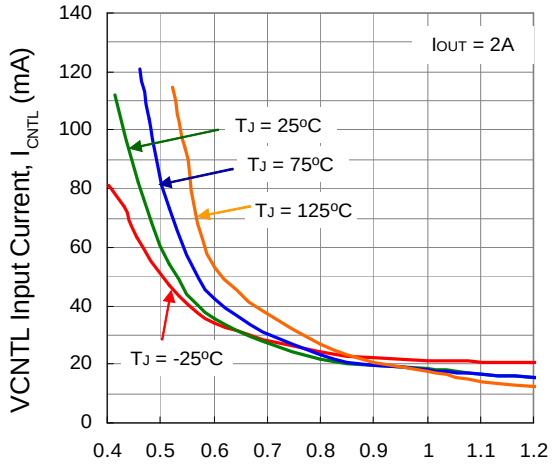
VCNTL Input Current
vs. V_{IN} - V_{OUT} Voltage at I_{OUT}=1.5A



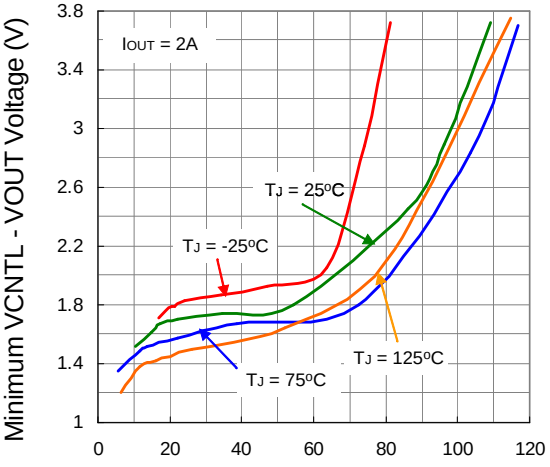
VCNTL-to-VOUT Dropout Voltage
vs. VCNTL Input Current



VCNTL Input Current
vs. V_{IN} - V_{OUT} Voltage at I_{OUT}=2A



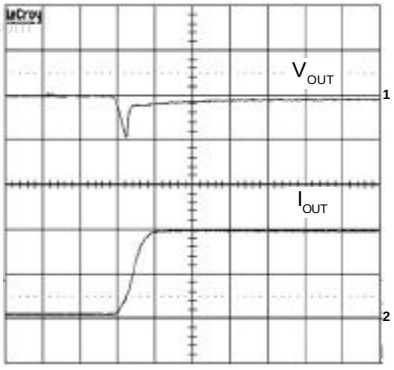
VCNTL-to-VOUT Dropout Voltage
vs. VCNTL Input Current



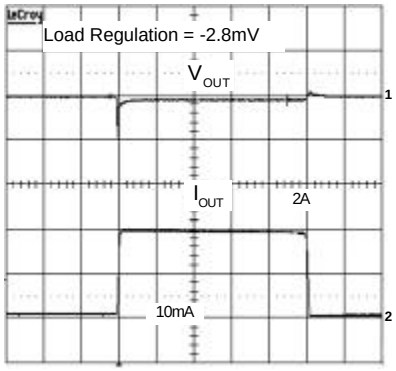
Operating Waveforms

1. Load Transient Response : I_{OUT} = 10mA -> 2A -> 10mA

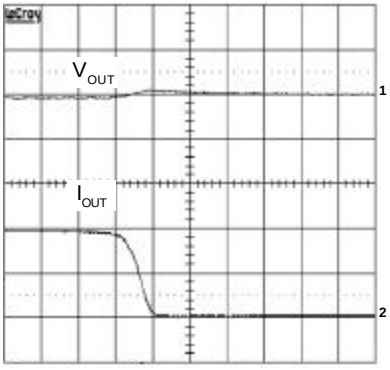
- V_{IN} = 2V, V_{CNTL} = 3.3V, V_{OUT} = 1.2V
- V_{REF} is 1.2V supplied by a regulator
- C_{OUT} = 330µF, ESR = 14mΩ
- I_{OUT} slew rate = 2A/µs



Ch1 : V_{OUT}, 20mV/Div, AC
Ch2 : I_{OUT}, 1A/Div
Time : 1µs/Div



Ch1 : V_{OUT}, 20mV/Div, AC
Ch2 : I_{OUT}, 1A/Div
Time : 10µs/Div

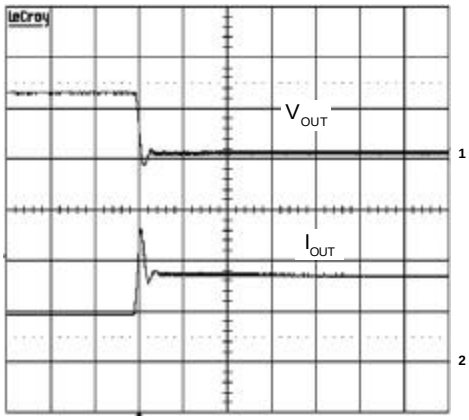


Ch1 : V_{OUT}, 20mV/Div, AC
Ch2 : I_{OUT}, 1A/Div
Time : 1µs/Div

2. Short-Circuit Test

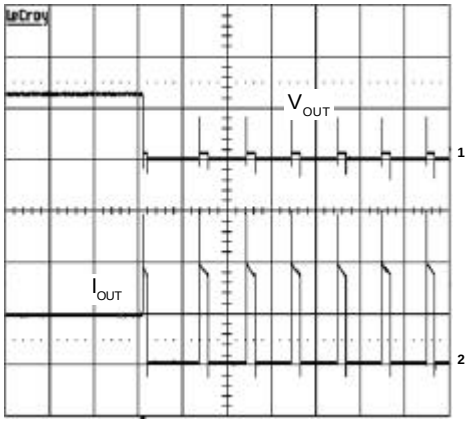
- V_{IN} = 2V, V_{CNTL} = 3.3V, V_{OUT} = 1.2V

V_{OUT} is Shorted to GND



Ch1 : V_{OUT}, 1V/Div, DC
Ch2 : I_{OUT}, 2A/Div
Time : 50µs/Div

V_{OUT} is Shorted to GND

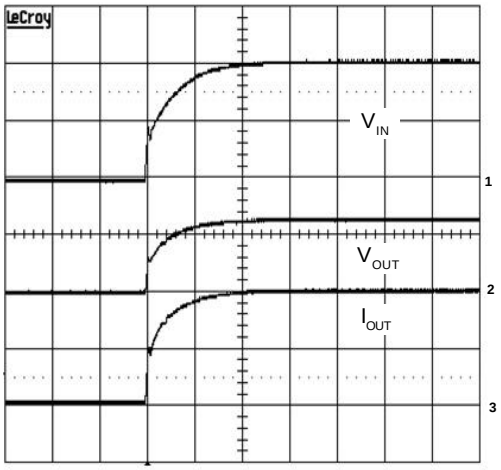


Ch1 : V_{OUT}, 1V/Div, DC
Ch2 : I_{OUT}, 2A/Div
Time : 50ms/Div

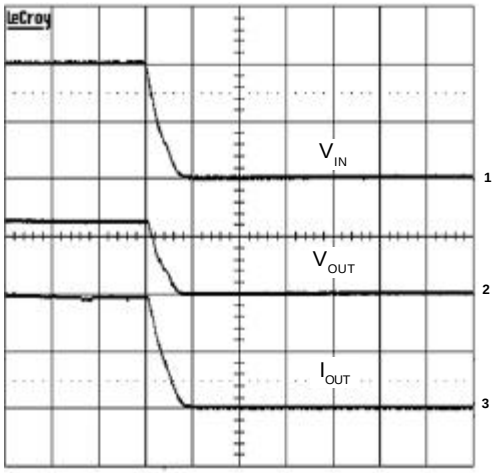
Operating Waveforms (Cont.)

3. Power on/off

- V_{IN} = 2V, V_{CNTL} = 3.3V, V_{OUT} = 1.2V



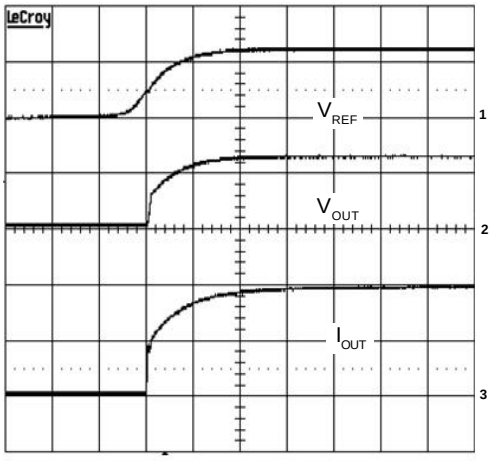
Ch1 : V_{IN}, 1V/Div, DC
Ch2 : V_{OUT}, 1V/Div, DC
Ch3 : I_{OUT}, 1A/Div
Time : 1ms/Div



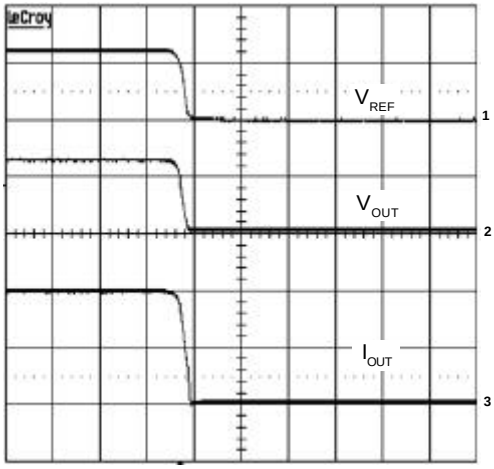
Ch1 : V_{IN}, 1V/Div, DC
Ch2 : V_{OUT}, 1V/Div, DC
Ch3 : I_{OUT}, 1A/Div
Time : 10ms/Div

4. Enable/Shutdown

- V_{IN} = 2V, V_{CNTL} = 3.3V, V_{OUT} = 1.2V



Ch1 : V_{REF}, 1V/Div, DC
Ch2 : V_{OUT}, 1V/Div, DC
Ch3 : I_{OUT}, 1A/Div
Time : 2ms/Div



Ch1 : V_{REF}, 1V/Div, DC
Ch2 : V_{OUT}, 1V/Div, DC
Ch3 : I_{OUT}, 1A/Div
Time : 2ms/Div

Application Information

General

The APL5330 is a linear regulator and is capable of providing output current up to 2A. The APL5330 is designed with the fast transient response, accurate output voltage, active-low shutdown control and fault protections (current-limit, thermal shutdown). The APL5330 is available in two packages to meet wide range of power dissipation requirements in various applications.

Output Voltage Regulation

The output voltage on VOUT pin tracks the reference voltage on VREF pin. A bypass NPN transistor controlled by a high bandwidth error amplifier regulates the output voltage by providing output current from VIN pin to the output. The base current of the pass transistor is provided by the VCNTL pin. An internal kelvin sensing scheme is used at the VOUT pin for perfect load regulation. Since the APL5330 exhibits very fast load transient response, lesser amount of capacitors can be used.

Current Limit

The APL5330 monitors the output current, and limits the maximum output current to prevent damages during overload or short-circuit conditions. To increase the input voltage on VIN or VCNTL will get higher current-limit points.

Shutdown and Soft-Start

The VREF pin is a dual-function input pin, acting as reference input and shutdown control input. Applying and holding a voltage below 0.35V(typ.) to VREF pin shuts down the output of the regulator. An NPN transistor or N-channel MOSFET is normaly used to pull down the VREF voltage while applying a “high” signal to turn on the transistor. When release the VREF pin, the current through the resistor divider charges the soft-start capacitor to initiate a soft-start process. The output voltage tracks the VREF voltage rises. The soft start function limits the input current.

Thermal Shutdown

A thermal shutdown circuit limits the junction temperature of the APL5330. When the junction temperature exceeds T_J= +170°C, a thermal sensor turns off the bypass transistor, allowing the device to cool down. The regulator starts to regulate again after the junction temperature reduces by 30°C, resulting in a pulsed output during continuous thermal overload conditions. The thermal limit designed with a 30°C hysteresis lowers the average T_J during continuous thermal overload conditions to extend life time of the APL5330.

Power Inputs

Input power sequencing is not necessary for VIN and VCNTL voltage supplies. However, do not apply a voltage to VOUT when there is no VCNTL voltage. This is because the internal parasitic diodes connected from VOUT to VIN or VCNTL is forward bias. The APL5330 can supply few current to load when the input voltage on VIN is not present.

Reference Voltage

The reference voltage is applied to the VREF pin connected with a resistor divider. Normally the bias current of the VREF pin flows out of the IC and is about 150nA (typ.), creating a voltage offset to the resistor divider and affecting the output voltage accuracy. The recommended resistors are <5kΩ to maintain the accurate output voltage. An external bypass capacitor is also connected to VREF. The capacitor (>0.1μF) and the resistor divider form a low-pass filter to reduce the inherent reference noise. Connect the capacitor as close to VREF as possible for optimal effect. More capacitance and large resistor divider will increase the soft-start interval. Do not place any additional loading on this reference input pin.

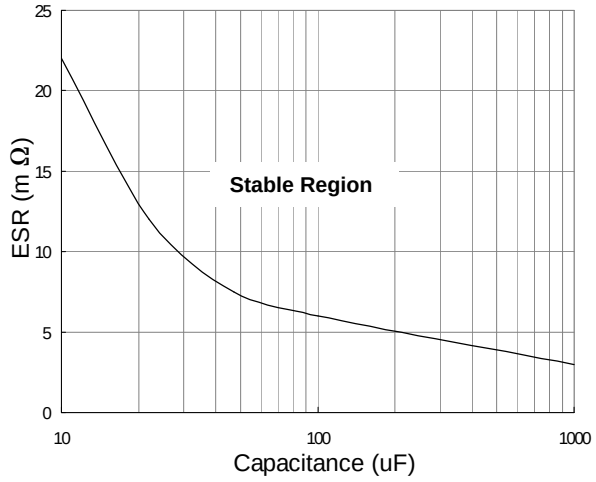
Application Information (Cont.)

Output Capacitor

The APL5330 requires a proper output capacitor to maintain stability and improve transient response.

The APL5330 can work stably with wide range of capacitance and ESR (equivalent series resistance). A low-ESR solid tantalum, aluminum electrolytic or ceramic output capacitor works extremely well and provides good transient response and stability over temperature.

The output capacitors also reduce the slew rate of load current and help the APL5330 to minimize variations of the output voltage. For this purpose, the low-ESR capacitors which depend on the step size and slew rate of load current are recommended.



Input Capacitor

The input capacitors of VCNTL and VIN pins are not required for stability but for supplying surge current during large load transients. This will prevent the input rail from dropping and improve the performance of the APL5330. The parasitic inductors between voltage sources or bulk capacitors and the power input pins will limit the slew rate of the surge currents during large load transients, resulting in voltage drop at VIN and VCNTL pins.

For VCNTL pin, a capacitor of 1μF (ceramic chip capacitor) or greater (aluminum electrolytic capacitor) is recommended. For VIN pin, an aluminum electrolytic capacitor (>47μF) is recommended. It is not necessary to use low-ESR capacitors.

Layout and Thermal Consideration

The input capacitors for VIN and VCNTL pins are normally placed near each pin for good performances. Ceramic decoupling capacitors of output must be placed as close to the load to reduce the parasitic inductance of traces. It is also recommended to place the APL5330 and output capacitors near the load for good load regulation and load transient response. Please connect the negative pins of the input and output capacitors and the GND pin of the APL5330 to the power ground plane of the load.

See figure 1. The SOP-8-P utilizes a bottom thermal pad to minimize the thermal resistance of the package and make the package suitable for high current applications. The thermal pad is soldered to the top ground pad connected to the internal or bottom ground plane by several vias. The printed circuit board (PCB) forms a heat sink and dissipates most of the heat into ambient air. It is recommended that the vias have proper size to retain solder and help heat conduction.

Thermal resistance consists of two main elements, θ_{JC} (junction-to-case thermal resistance) and θ_{CA} (case-to-ambient thermal resistance). θ_{JC} is specified from the IC junction to the bottom of the thermal pad directly below the die. θ_{CA} is the resistance from the bottom of thermal pad to the ambient air and it includes θ_{CS} (case-to-sink thermal resistance) and θ_{SA} (sink-to-ambient thermal resistance). The specified path for heat flow is the lowest resistance path and it dissipates majority of the heat to the ambient air. Typically, θ_{CA} is the dominant thermal resistance. Therefore, enlarging

Application Information (Cont.)

Layout and Thermal Consideration (Cont.)

the internal or bottom ground plane reduces the resistance θ_{CA}. The relationship between power dissipation and temperatures is the following equation:

$$P_D = (T_J - T_A) / \leq \theta_{JA}$$

where,

P_D : Power dissipation

T_J : Junction Temperature

T_A : Ambient Temperature

θ_{JA} : Junction-to-Ambient Thermal Resistance

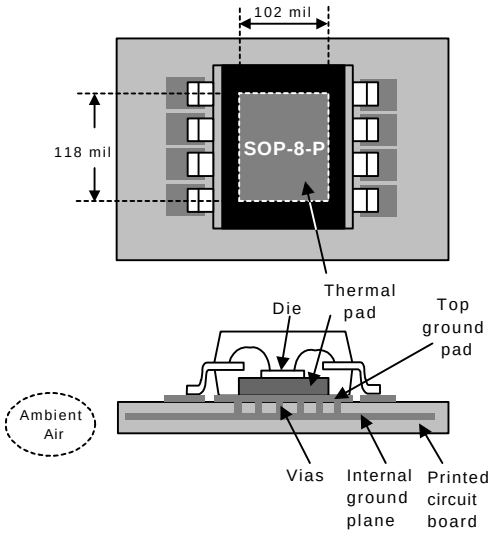
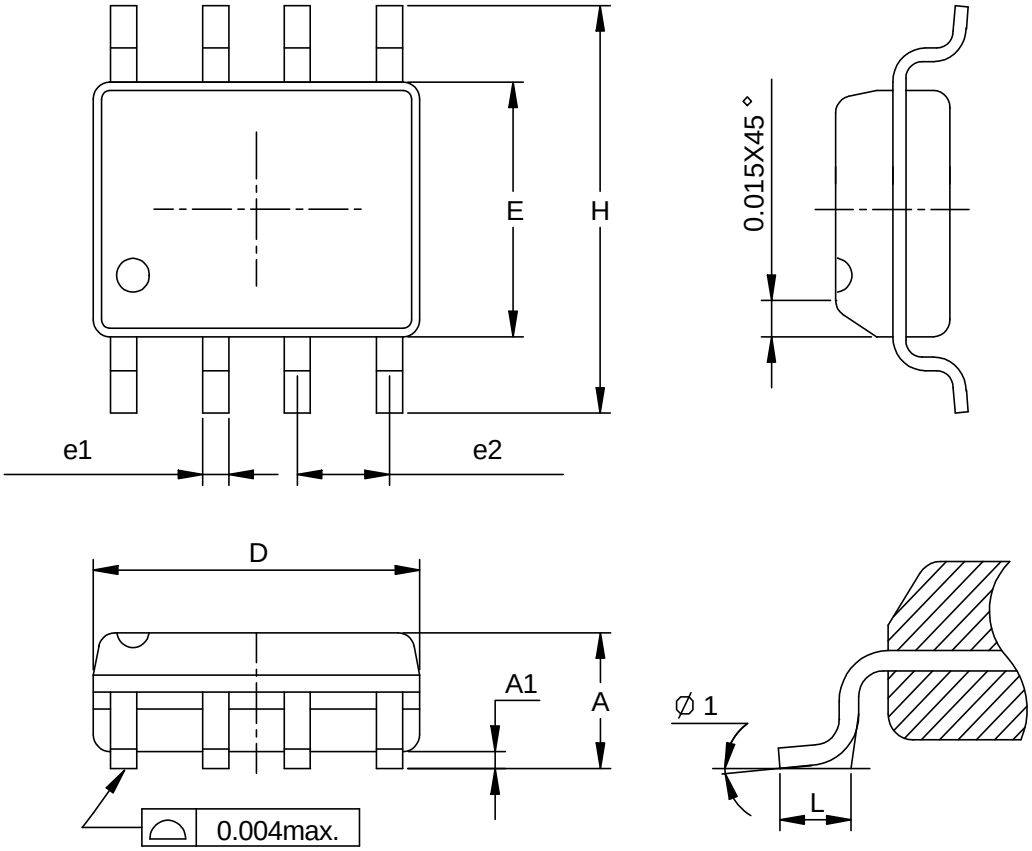


Figure 1 Top and side view of layout around the APL5330

Packaging Information

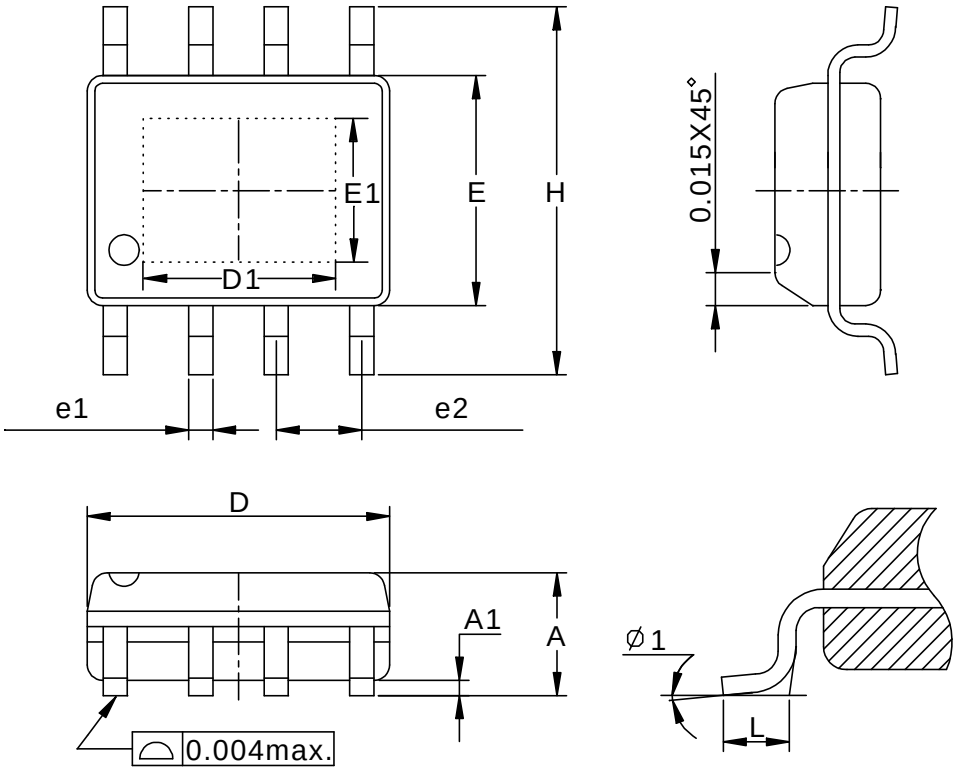
SOP-8 pin (Reference JEDEC Registration MS-012)



Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	4.80	5.00	0.189	0.197
E	3.80	4.00	0.150	0.157
H	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
e1	0.33	0.51	0.013	0.020
e2	1.27BSC		0.50BSC	
ϕ 1	0°	8°	0°	8°

Packaging Information

SOP-8-P pin (Reference JEDEC Registration MS-012)

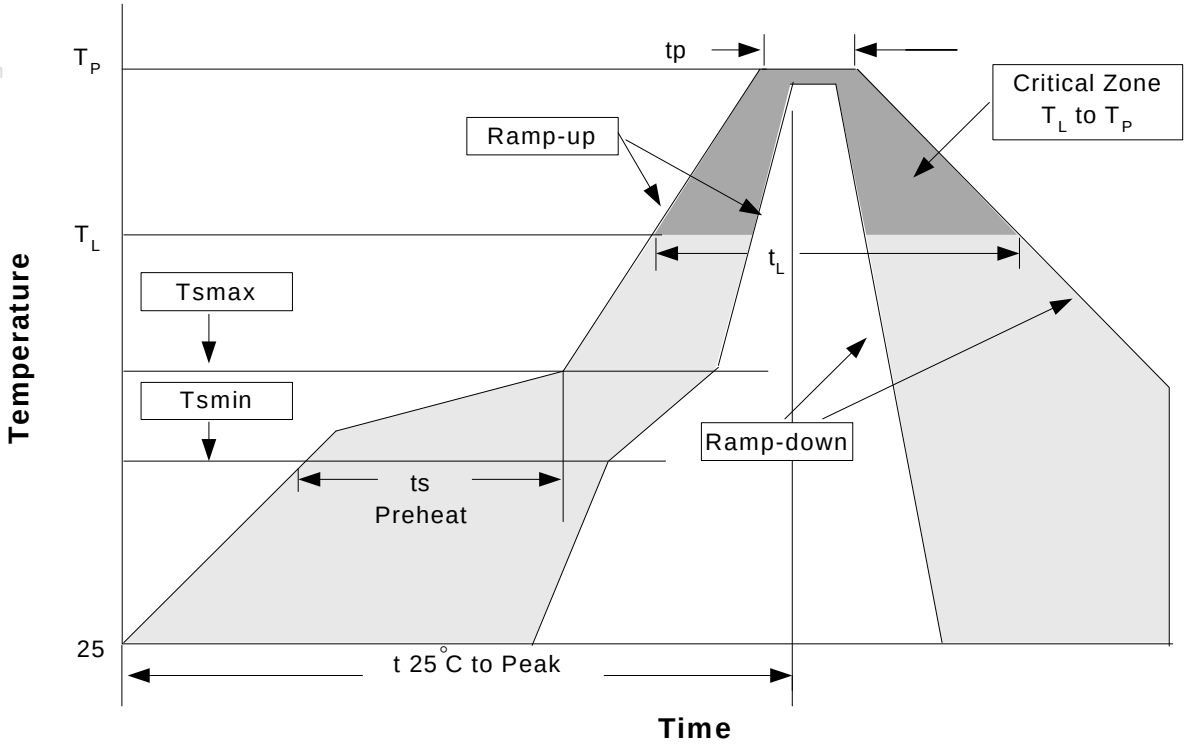


Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.35	1.75	0.053	0.069
A1	0	0.15	0	0.006
D	4.80	5.00	0.189	0.197
D1	3.00REF		0.118REF	
E	3.80	4.00	0.150	0.157
E1	2.60REF		0.102REF	
H	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
e1	0.33	0.51	0.013	0.020
e2	1.27BSC		0.50BSC	
ϕ1	8°		8°	

Physical Specifications

Terminal Material	Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb), 100%Sn
Lead Solderability	Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.

Reflow Condition (IR/Convection or VPR Reflow)



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak/Classificatioon Temperature (Tp)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Notes: All temperatures refer to topside of the package .Measured on the body surface.

Classification Reflow Profiles(Cont.)

Table 1. SnPb Entectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

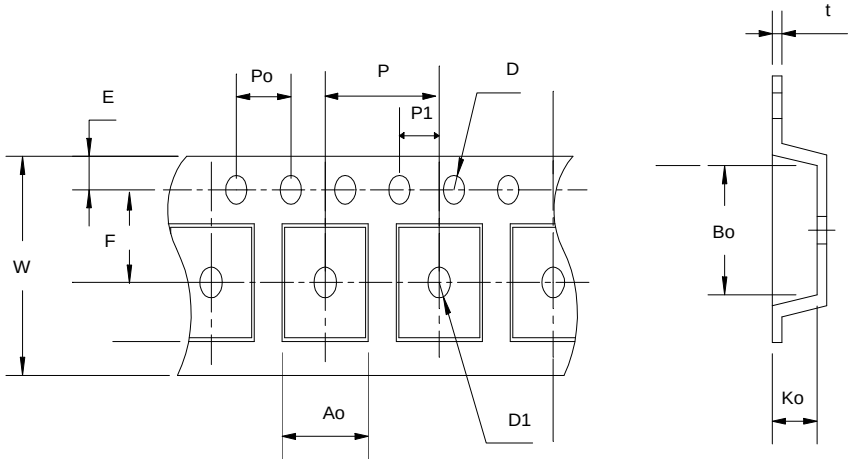
Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*
*Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.			

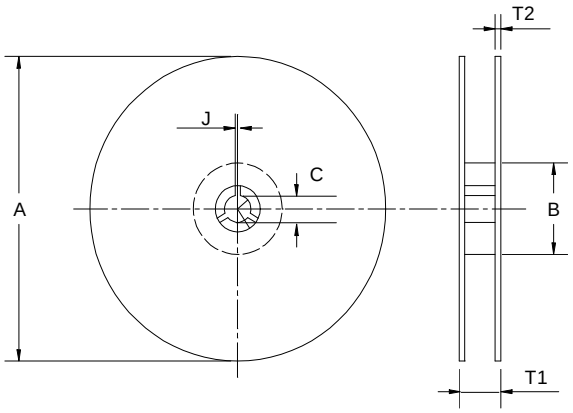
Reliability Test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 SEC
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @125°C
PCT	JESD-22-B,A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms, 1_{tr} > 100mA

Carrier Tape



Carrier Tape(Cont.)



Application	A	B	C	J	T1	T2	W	P	E
SOP- 8/ SOP-8-P	330 ± 1	62 +1.5	12.75+ 0.15	2 ± 0.5	12.4 ± 0.2	2 ± 0.2	12± 0. 3	8± 0.1	1.75±0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	5.5± 1	1.55 +0.1	1.55+ 0.25	4.0 ± 0.1	2.0 ± 0.1	6.4 ± 0.1	5.2± 0. 1	2.1± 0.1	0.3±0.013

(mm)

Cover Tape Dimensions

Application	Carrier Width	Cover Tape Width	Devices Per Reel
SOP- 8 / SOP-8-P	12	9.3	2500

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