3A Bus Termination Regulator

Features

- Sourcing and Sinking Current up to 3A
- Wide Input Voltage Range: 1.2V to 3.6V
- VTT and VTTREF Voltage Tracks at Half the VREF Voltage
- VTT and VTTREF Voltage with ±20mV Accuracy
- Excellent Load Transient Response
  - Droop Compensation
  - Fast Loop Response
- Stable with 20mF Ceramic Output Capacitors
- Current Limit Protection
- Thermal Shutdown Protection
- Power-On-Reset Function on VCNTL
- S3, S5 Input Signals for ACPI States
- Available in a Thermal Enhanced MSOP-10P Package
- Lead Free Available (RoHS Compliant)

Applications

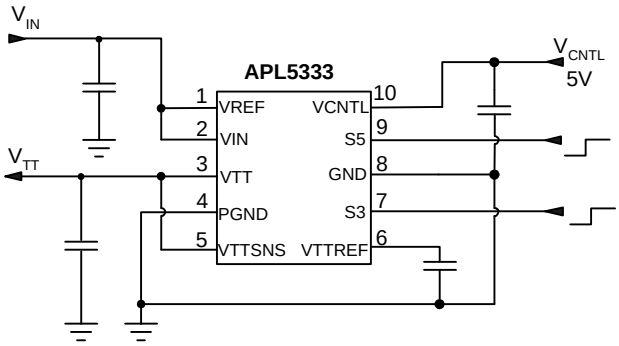
- DDR 1/2/3 Memory Termination
- SSTL-2, STL-18 and HSTL Termination

General Description

The APL5333 linear regulator is designed to provide a regulated voltage with bi-directional output current for DDR-SDRAM termination. The APL5333 integrates two power transistors to source or sink current up to 3A. It also incorporate current-limit, thermal shutdown into a single chip.

The output voltage of APL5333 tracks the voltage at VREF pin. An internal resistor divider is used to provide a half voltage of VREF for VTTREF and VTT Voltage. The VTT output voltage is only requiring 20µF of ceramic output capacitance for stability and fast transient response. The S3 and S5 pins provide the sleep state for VTT (S3 state) and suspend state (S4/S5 state) for device, when S5 and S3 are both pulled low the device provides the soft-off for VTT and VTTREF. The MSOP-10P package with a copper pad is available which provides excellent thermal impedance.

Simplified Application Circuit



Ordering and Marking Information

APL5333 □□□-□□□

- Lead Free Code
- Handling Code
- Temperature Range
- Package Code

Package Code
XA : MSOP-10P
Temperature Range
I : - 40 to 85 °C
Handling Code
TR : Tape & Reel
Lead Free Code
L : Lead Free Device

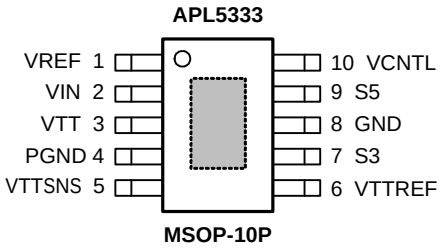
APL5333 XA : L5333 XXX XX

X - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte in plate termination finish; which are fully compliant with RoHS and compatible with both SnPb and lead-free soldering operations. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J STD-020C for MSL classification at lead-free peak reflow temperature.

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Pin Configuration



MSOP-10P

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{CNTL}	VCNTL Supply Voltage (VCNTL to GND)	-0.3~6	V
V_{IN}	VIN Supply Voltage (VIN to GND)	-0.3~6	V
V_{TT}	VTT Output Voltage (VTT to GND)	-0.3~6	V
V_{TTREF}	VTTREF Output Voltage (VTTREF to GND)	-0.3~6	V
	VTTSNS, VREF, S3 and S5 Voltage	-0.3~6	V
	PGND to GND Voltage	-0.3~0.3	V
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-65 to 150	°C
T_{SDR}	Maximum Lead Soldering Temperature	260, 10 sec	°C

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute mximum rating conditions for extended periods may affect device reliability.

Thermal Characteristic (Note 2)

Symbol	Parameter	Rating	Unit
θ_{JA}	Junction to Ambient Resistance in Free Air	60	°C/W

Note 2 : θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{CNTL}	VCNTL to GND	4.5~5.5	V
V_{IN}	VIN to GND	1.2~3.6	V
V_{TT}	VTT to GND	0.6~1.8	V
V_{REF}	VREF to GND	1.2~3.6	V
I_{VTT}	VTT Output Current (Note 4)	-3~+3	A
C_{IN}	VIN Input Capacitor	4.7~100	µF
C_{OUT}	Capacitance of VTT Output Multi-layer Ceramic Capacitor (MLCC)	4.7~47	µF
T_A	Ambient Temperature	-40~+80	°C
T_J	Junction Temperature	-40~+125	°C

Note 3 : Refer to the typical application circuit

Note 4 : If the VTT output current is “+3A”, then VTT source would be 3A current, and vice versa.

Electrical Characteristics

V_{CNTL}=5V, V_{IN}=V_{REF}=1.8V, T_A = -40 to 85°C, unless otherwise specified. Typical values refer to T_A =25°C.

Symbol	Parameter	Test Conditions	APL5333			Unit
			Min	Typ	Max	
SUPPLY CURRENT						
I_{VCNTL}	VCNTL Supply Current	T_A =25°C, V_{S3}=V_{S5}=5V, no load	0.3	0.7	2	mA
	VCNTL Standby Current	T_A =25°C, V_{S3}=0V, V_{S5}=5V, no load	20	40	80	µA
	VCNTL Shutdown Current	T_A =25°C, V_{S3}=V_{S5}=0V, no load V_{IN}=V_{REF}=0V	-	0.04	1.0	
I_{VIN}	VIN Supply Current	T_A =25°C, V_{S3}=V_{S5}=5V, no load	0.7	2	4	mA
	VIN Standby Current	T_A =25°C, V_{S3}=0V, V_{S5}=5V, no load	-	6	10	µA
	VIN Shutdown Current	T_A =25°C, V_{S3}=V_{S5}=0V, no load	-	0.3	1.0	
INPUT CURRENT						
I_{VREF}	VREF Input Current	V_{S3}=V_{S5}=5V	1	3	5	µA
I_{VTTSNS}	VTTSNS Input Current	V_{S3}=V_{S5}=5V	-1.00	-	1.00	
POWER-ON-RESET						
	VCNTL POR Threshold	V_{CNTL} Rising	3.6	3.8	4.0	V
	VCNTL POR Hysteresis		0.1	0.2	0.3	V
VTT OUTPUT						
V_{TT}	VTT Output Voltage	V_{IN}=V_{REF}=2.5V	-	1.25	-	V
		V_{IN}=V_{REF}=1.8V	-	0.9	-	
		V_{IN}=V_{REF}=1.5V	-	0.75	-	
	VTT Output Voltage Tolerance	V_{IN}=V_{REF}=2.5V, I_{VTT}=0A	-20	-	20	mV
		V_{IN}=V_{REF}=2.5V, I_{VTT}=±1.5A	-30	-	30	
		V_{IN}=V_{REF}=2.5V, I_{VTT}=±3A	-40	-	40	
		V_{IN}=V_{REF}=1.8V, I_{VTT}=0A	-20	-	20	
		V_{IN}=V_{REF}=1.8V, I_{VTT}=±1A	-30	-	30	
		V_{IN}=V_{REF}=1.8V, I_{VTT}=±2A	-40	-	40	
		V_{IN}=V_{REF}=1.5V, I_{VTT}=0A	-20	-	20	
		V_{IN}=V_{REF}=1.5V, I_{VTT}=±1A	-30	-	30	
		V_{IN}=V_{REF}=1.5V, I_{VTT}=±2A	-40	-	40	
	VTT Current Limit	V_{TT} < 0.5 X V_{REF} X 1.05 and V_{TT} > 0.5 X V_{REF} X 0.95	3.3	3.8	4.5	A
	VTT Short Circuit Current Limit	V_{TT} > 0.5 X V_{REF} X 1.1 or V_{TT} < 0.5 X V_{REF} X 0.9	1	1.7	2.3	
$R_{DS(ON)}$	Internal Power MOSFETs $R_{DS(ON)}$	Upper MOSFET	-	230	330	mΩ
		Lower MOSFET	-	230	330	
	VTT Leakage Current	V_{TT}=1.25V, V_{S3}=0V, V_{S5}=5V, T_A =25°C	-	2.5	4.0	µA
	VTTSNS Leakage Current	V_{TT}=1.25V, T_A =25°C	-1.00	-	1.00	µA
	VTT Discharge Current	V_{TT}=0.5V, V_{S3}=V_{S5}=0V, T_A =25°C V_{REF}=0V	20	35	50	mA

Electrical Characteristics (Cont.)

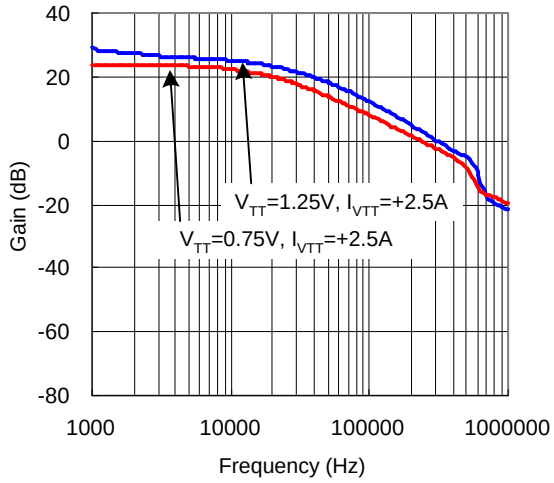
V_{CNTL}=5V, V_{IN}=V_{REF}=1.8V, T_A = -40 to 85°C, unless otherwise specified. Typical values refer to T_A =25°C.

Symbol	Parameter	Test Conditions	APL5333			Unit
			Min	Typ	Max	
VTTREF OUTPUT						
V_{TTREF}	VTTREF Output Voltage	V_{IN}=V_{REF} =2.5V	-	1.25	-	V
		V_{IN}=V_{REF} =1.8V	-	0.9	-	
		V_{IN}=V_{REF} =1.5V	-	0.75	-	
	VTTREF Output Voltage Tolerance	V_{IN}=V_{REF}, I_{VTTREF}<10mA	-20	-	+20	mV
I_{VTTREF}	VTTREF Source Current Limit	V_{TTREF}=0V	10	20	30	mA
$I_{VREFDIS}$	VTTREF Discharge Current	V_{TTREF}=2.5V, V_{S3}=V_{S5}=0V, T_A =25°C	1	2	3	mA
LOGIC THRESHOLD						
V_{IH}	High Threshold Voltage	V_{S3}, V_{S5} Rising	1.6	-	-	V
V_{IL}	Low Threshold Voltage	V_{S3}, V_{S5} Falling	-	-	0.3	V
	Leakage Current	S3, S5, T_A =25°C	-1	-	1	µA
THERMAL SHUTDOWN						
T_{SD}	Thermal Shutdown Temperature	T_J Rising	-	150	-	°C
	Thermal Shutdown Hysteresis		-	30	-	°C

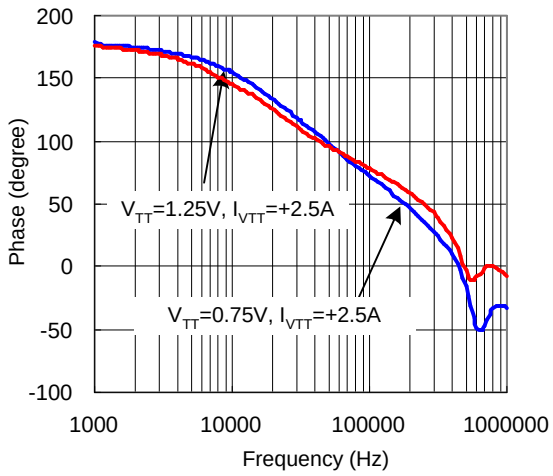
Typical Operating Characteristics

(Refer to the section "Typical Application Circuits", V_{CNTL}=5V, V_{IN}=V_{REF}=1.8V, V_{TT}=0.9V, T_A=25°C)

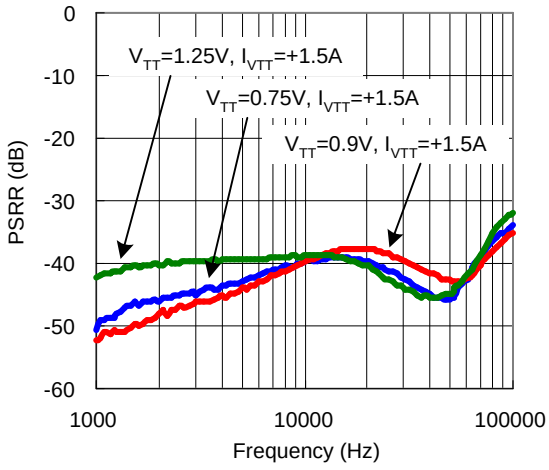
Frequency Response



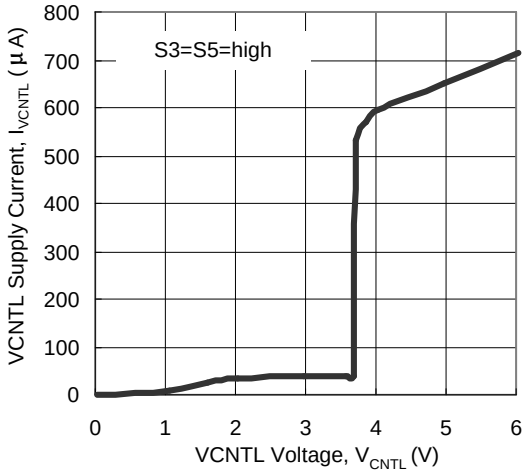
Frequency Response



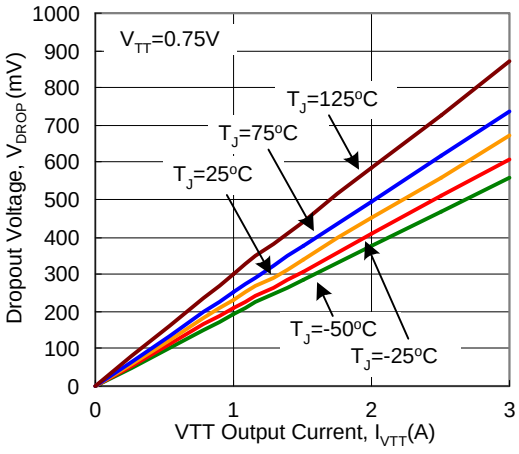
VCNTL PSRR



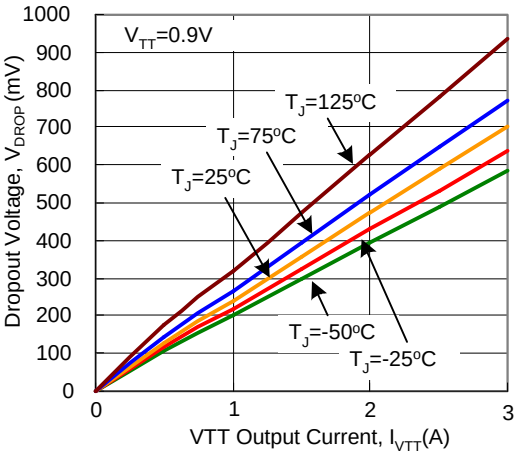
VCNTL Supply Current vs. VCNTL Voltage



Dropout Voltage vs. VTT Output Current



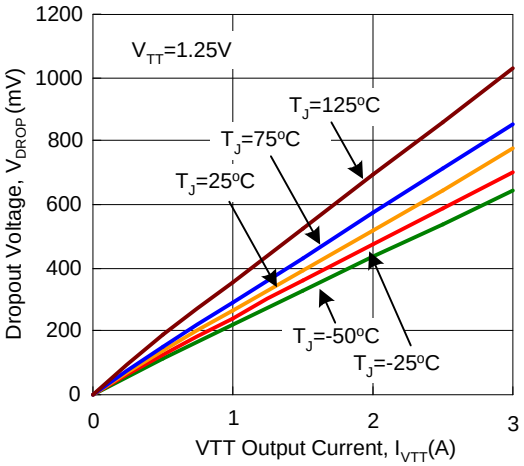
Dropout Voltage vs. VTT Output Current



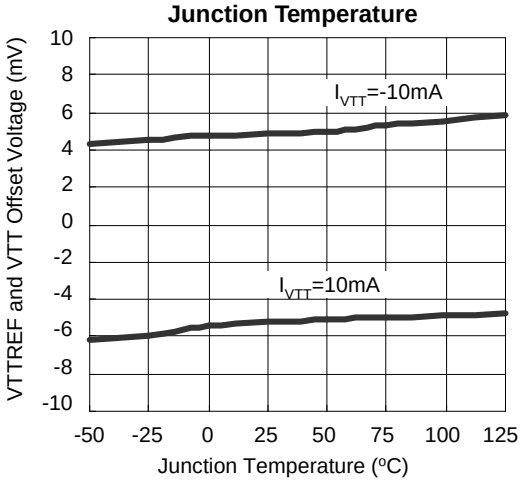
Typical Operating Characteristics (Cont.)

(Refer to the section "Typical Application Circuits", V_{CNTL}=5V, V_{IN}=V_{REF}=1.8V, V_{TT}=0.9V, T_A=25°C)

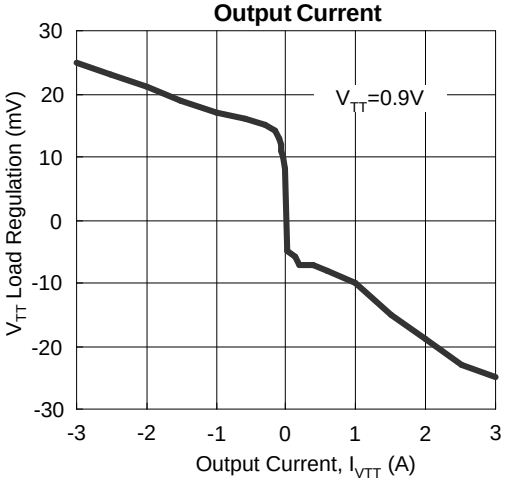
Dropout Voltage vs. VTT Output Current



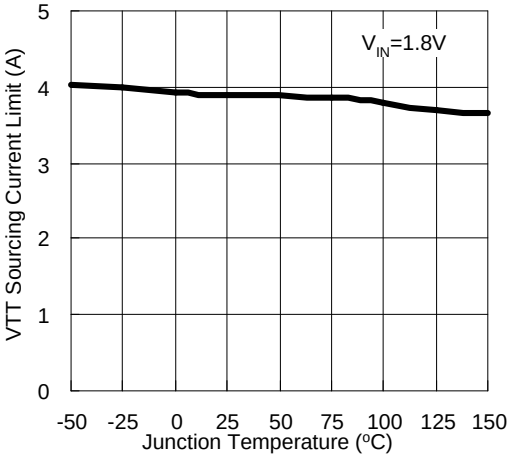
VTTREF and VTT Offset Voltage vs. Junction Temperature



V_{TT} Load Regulation vs. Output Current



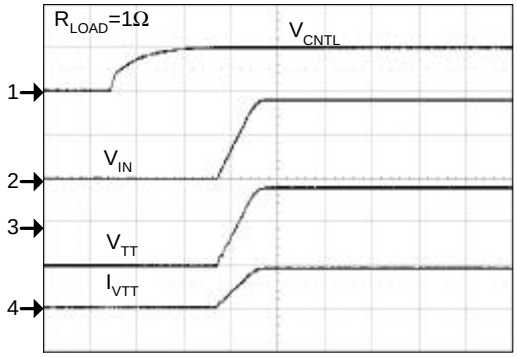
VTT Source Current Limit vs. Junction Temperature



Operating Waveforms

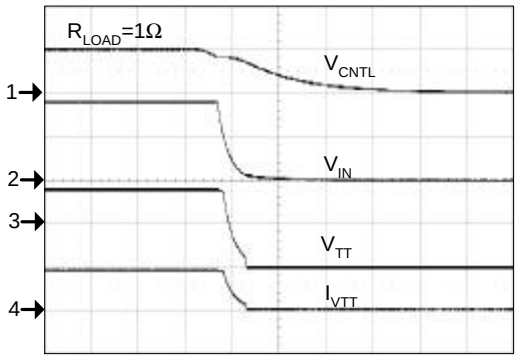
(Refer to the section "Typical Application Circuits", V_{CNTL}=5V, V_{IN}=V_{REF}=1.8V, V_{TT}=0.9V, T_A=25°C)

Power on



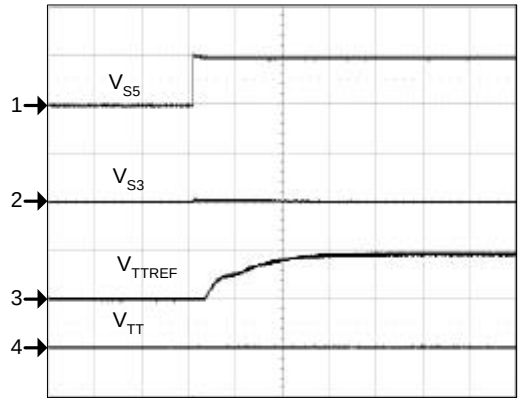
CH1 : V_{CNTL} , 5V/div
CH2 : V_{IN} , 1V/div
CH3 : V_{TT} , 500mV/div
CH4 : I_{VTT} , 1A/div
Time : 2ms/div

Power off



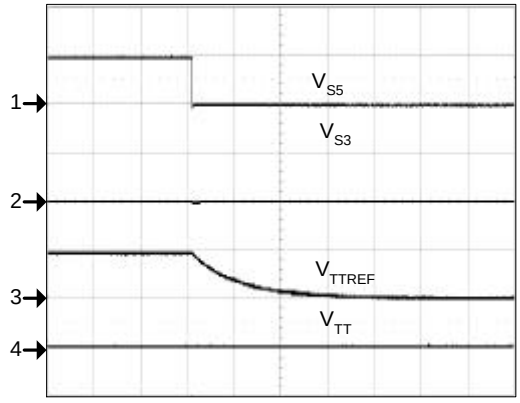
CH1 : V_{CNTL} , 5V/div
CH2 : V_{IN} , 1V/div
CH3 : V_{TT} , 500mV/div
CH4 : I_{VTT} , 1A/div
Time : 5ms/div

S5 Low to High



CH1 : V_{S5} , 5V/div
CH2 : V_{S3} , 5V/div
CH3 :V_{TTREF} , 1V/div
CH4 : V_{TT} , 1V/div
Time : 10µs/div

S5 High to Low

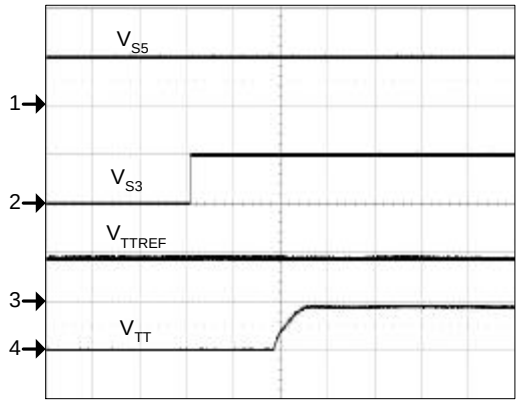


CH1 : V_{S5} , 5V/div
CH2 : V_{S3} , 5V/div
CH3 :V_{TTREF} , 1V/div
CH4 : V_{TT} , 1V/div
Time : 20µs/div

Operating Waveforms (Cont.)

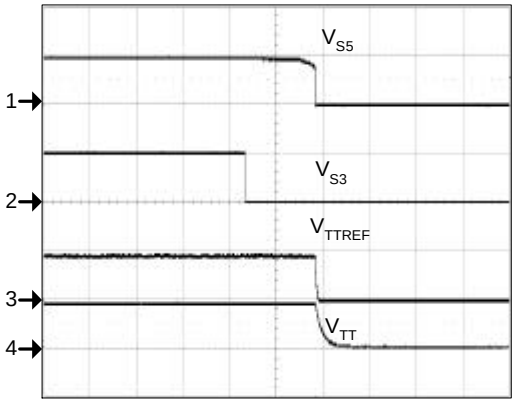
(Refer to the section "Typical Application Circuits", V_{CNTL}=5V, V_{IN}=V_{REF}=1.8V, V_{TT}=0.9V, T_A=25°C)

S3 Low to High



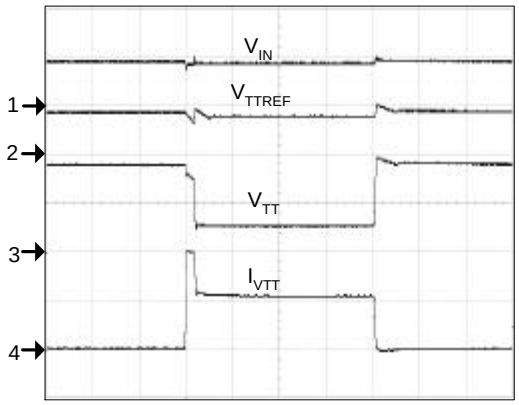
CH1 : V_{S5} , 5V/div
CH2 : V_{S3} , 5V/div
CH3 :V_{TTREF} , 1V/div
CH4 : V_{TT} , 1V/div
Time : 20µs/div

S3 and S5 High to Low



CH1 : V_{S5} , 5V/div
CH2 : V_{S3} , 5V/div
CH3 :V_{TTREF} , 1V/div
CH4 : V_{TT} , 1V/div
Time : 5ms/div

Current Limit and Short Circuit Current Limit

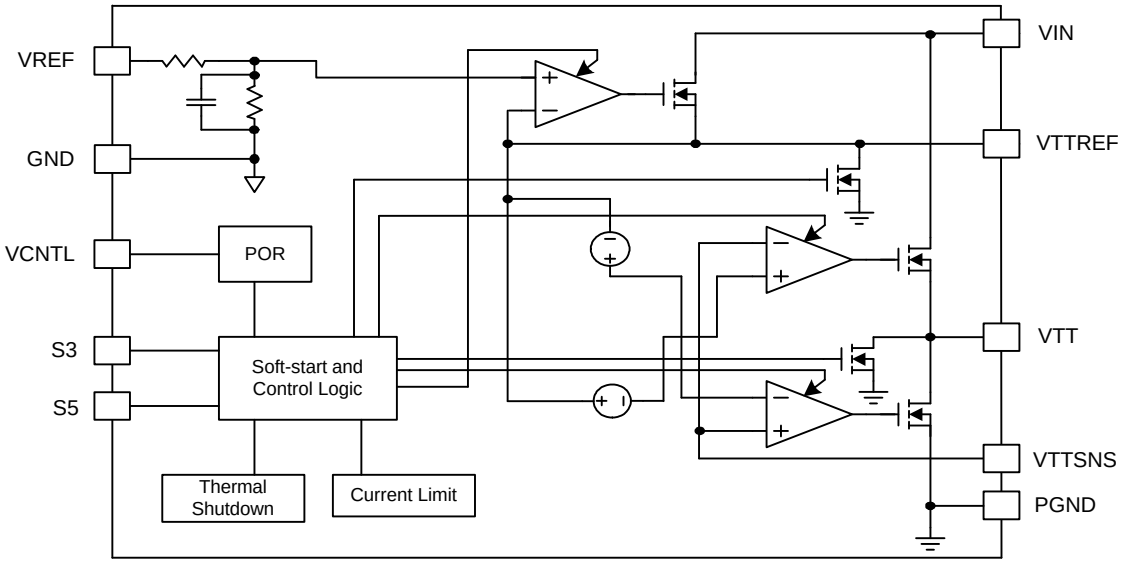


CH1 : V_{IN} , 2V/div
CH2 : V_{TTREF} , 1V/div
CH3 : V_{TT} , 500mV/div
CH4 : I_{VTT} , 2A/div
Time : 500µs/div

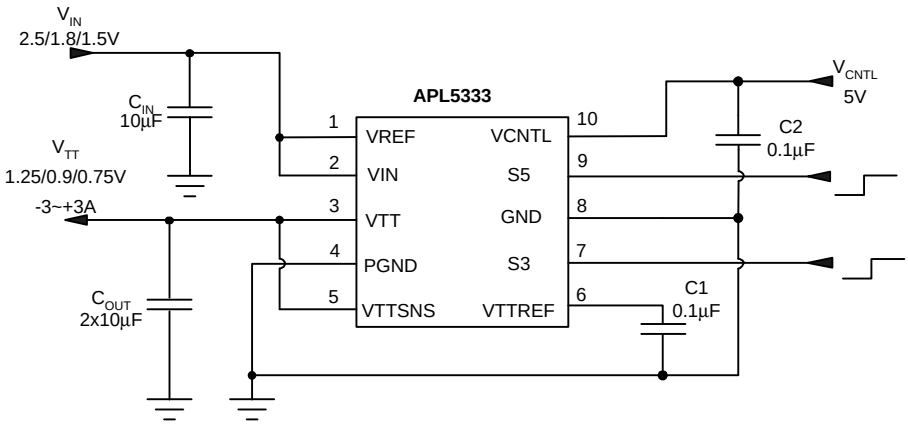
Pin Description

PIN NO.	PIN NAME	DESCRIPTION
1	VREF	Reference Voltage Input for VTT and VTTREF Regulator.
2	VIN	Power Input for VTT and VTTREF Pin. An input capacitor should be connected from VIN to PGND.
3	VTT	VTT Output Voltage Pin. Source and sink current up to 3A. To insure the stability issue, the output capacitor typical 20µF(10µF*2) should be connected from VTT to PGND.
4	PGND	Power Ground for VIN and VTT.
5	VTTSNS	Voltage Sense for VTT. Connect to the positive node of V_{TT} output capacitors.
6	VTTREF	VTT Reference Output Pin. A small capacitor 0.1µF should be connected from VTTREF to GND.
7	S3	S3 Signal Input.
8	GND	Signal Ground.
9	S5	S5 Signal Input
10	VCNTL	Power Input for Internal Control Circuitry. A bypass capacitor 0.1µF should be connected near the pin.

Block Diagram



Typical Application Circuit



Function Description

VTT Source/Sink Regulator

The APL5333 is a low dropout source/sink linear regulator with maximum 3A source/sink current. Two internal N-channel MOSFETs controlled by separate high bandwidth error amplifiers regulate the output voltage by sourcing current from VIN or sinking current to PGND. To prevent two pass elements from shoot-through, a voltage offset is created between two positive inputs of the error amplifiers. The APL5333 has a droop compensation for minimizing the amplitude of the peak-to-peak VTT voltage during load transient response. The droop voltage, added to the reference voltage applied to the positive inputs, is regulated by and proportional to the VTT sourcing and sinking output current. Therefore, the droop voltage is positive at sinking current and negative at sourcing current. Typical droop voltage is within ±40mV in all conditions.

Power-on-Reset (POR)

The APL5333 monitors the VCNTL pin voltage for power-on-reset function to prevent erroneous operation. The built-in POR circuit keeps the outputs shutoff until internal circuit is operating properly. Typical POR threshold is 3.8V with 0.2V hysteresis.

VTTREF Regulator

VTTREF voltage follows 1/2VREF voltage which is the reference of the VTT regulator. The VTTREF block consists of a resistor divider and a low pass filter. The regulator can source current up to 10mA. To insure the stability, a 0.1μF ceramic capacitor should be connected from VTTREF to GND.

Soft-start, Current Limit and Short Circuit Current Limit

The APL5333 provides a current limit protection to prevent the device from burnout. According to the voltage between VTT and VTTREF, current limit level is divided into two levels. When the VTT voltage is out of the 10% VTTREF voltage, the current limit is 1.7A (typical) and VTT voltage comes inside the 5% of VTTREF voltage, the current limit switches to 3.8A (typical). The APL5333 provides a soft-start function, using the constant current to charge the output capacitor that gives a rapid and linear output voltage rise. If the load current is above the current limit 1.7A at start-up, the VTT cannot start sucessfully.

STATE	S3	S5	VTTREF	VTT
S0	H	H	1	1
S3	L	H	1	0 (high-Z)
S4/5	L	L	0 (discharge)	0 (discharge)

Table1. The truth table of S3 and S5 pins

S3, S5 Control

The S3 and S5 signals control the VTT and VTTREF states and these pins should be connected to SLP_S3 and SLP_S5 signals respectively. The table1 shows the truth table of the S3 and S5 pins. When both S3 and S5 are above the logic threshold voltage, the VTT and VTTREF are turned on at S0 state. When S3 is low and S5 is high, the VTT voltage is disabled and left high impedance in S3 state. When both S3 and S5 are low, the VTT and VTTREF are turned off and discharged to the ground through internal MOSFETs during S4/S5 state. (Note that if the S3 is forced high and S5 is forced low, then VTTREF is discharged and VTT is at high-Z state. Such condition is not recommended.)

Thermal Shutdown

A thermal shutdown circuit limits the junction temperature of the APL5333. When the junction temperature exceeds +150°C, the device will turn off the MOSFETs, allowing the device to cool down. The regulator regulates the output again through initiation of a new soft-start cycle after the junction temperature cools by 30°C, resulting in a pulsed output during continuous thermal overload conditions. The thermal shutdown designed with a 30°C hysteresis lowers the average junction temperature during continuous thermal overload conditions, extending lifetime of the device. For normal operation, device power dissipation should be externally limited so that junction temperatures will not exceed +125°C.

Application Information

Input Capacitor

The APL5333 requires proper input capacitors to supply surge current during stepping load transients to prevent the input rail from dropping. Because the parasitic inductor from the voltage sources or other bulk capacitors to the VIN limits the slew rate of the surge current, it is necessary to place the input capacitors near VIN as close as possible. Input capacitors should be greater than 4.7µF. A capacitor of 0.47µF (MLCC) or above is recommended for VCNTL pin noise decoupling.

Output Capacitor

The APL5333 needs a proper output capacitor to maintain circuit stability and improve transient response over temperature and current. In order to insure the circuit stability, a 4.7µF MLCC (minimum) as an output capacitor must be placed near the VTT. With X5R and X7R dielectrics, 20µF is sufficient at all operating temperatures. Attaching two 10µF ceramic capacitors in parallel, the effects from ESR and ESL can be minimized.

Thermal Consideration

The APL5333 maximum power dissipation depends on the differences of the thermal resistance and temperature between junction and ambient air. The power dissipation P_D across the device is:

$$P_D = (T_J - T_A) / \theta_{JA}$$

where (T_J-T_A) is the temperature difference between the junction and ambient air. θ_{JA} is the thermal resistance between junction and ambient air. Assuming the T_A=25°C and maximum T_J=150°C (typical thermal limit threshold), the maximum power dissipation is calculated as:

$$P_{D(max)}=(150-25)/60$$
$$= 2.08(W)$$

For normal operation, do not exceed the maximum operating junction temperature of T_J = 125°C. The calculated power dissipation should be less than:

$$P_D=(125-25)/60$$
$$= 1.66(W)$$

The exposed pad provides an electrical connection to ground and channels heat away. Connect the exposed pad to ground by using a large ground plane.

Layout Consideration

Figure 1 illustrates the layout. Below is a checklist for your layout:

1. Please place the input capacitors close to the VIN.
2. Output capacitors for VTT must be close to the pin with short and wide track.
3. VTTSNS should be connected to the output capacitors of VTT separated from large current path to avoid effect of ESR and ESL. The ESR and ESL of ground track between VTT and GND should be minimized.
4. VREF should be connected to VIN by a separate track. VREF is the reference voltage of VTTREF, so avoid any noise to get into the VREF.
5. PGND is the ground of VIN and VTT. GND is the signal ground of VREF, VTTREF S3 and S5. GND and PGND should be isolated with a single point connection between them.
6. Soldering the exposed pad to ground is good for heatsinking. Numerous vias 0.33 mm in diameter connected from the thermal land to the internal/solder-side ground plane(s) should be used to enhance dissipation.

Large ground plane is good for heatsinking. Optimum performance can only be achieved when the device is mounted on a PC board according to the board layout diagrams which are shown as Figure 2.

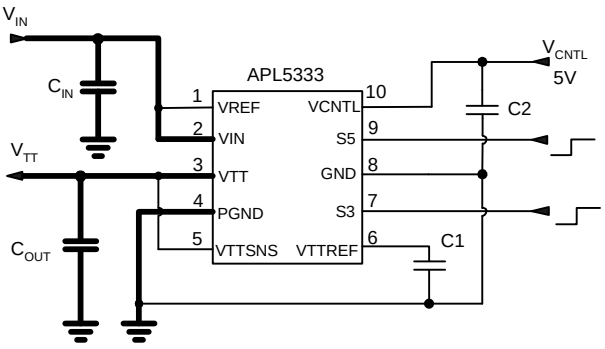


Figure 1

Application Information (Cont.)

Layout Consideration (Cont.)

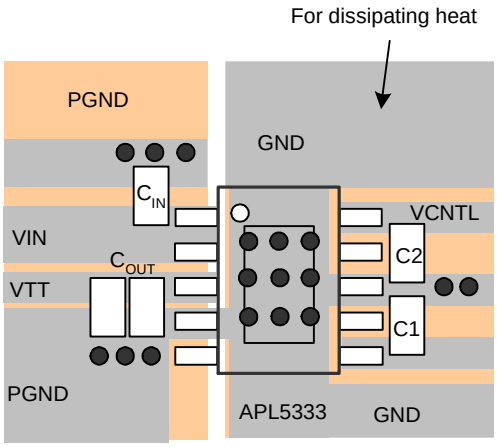
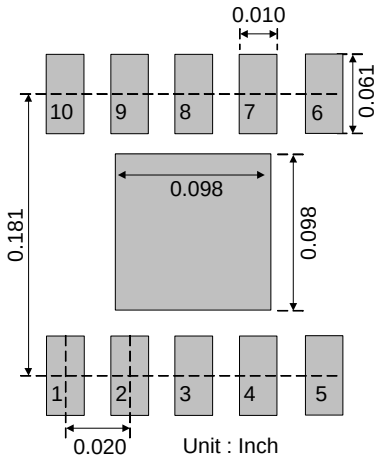


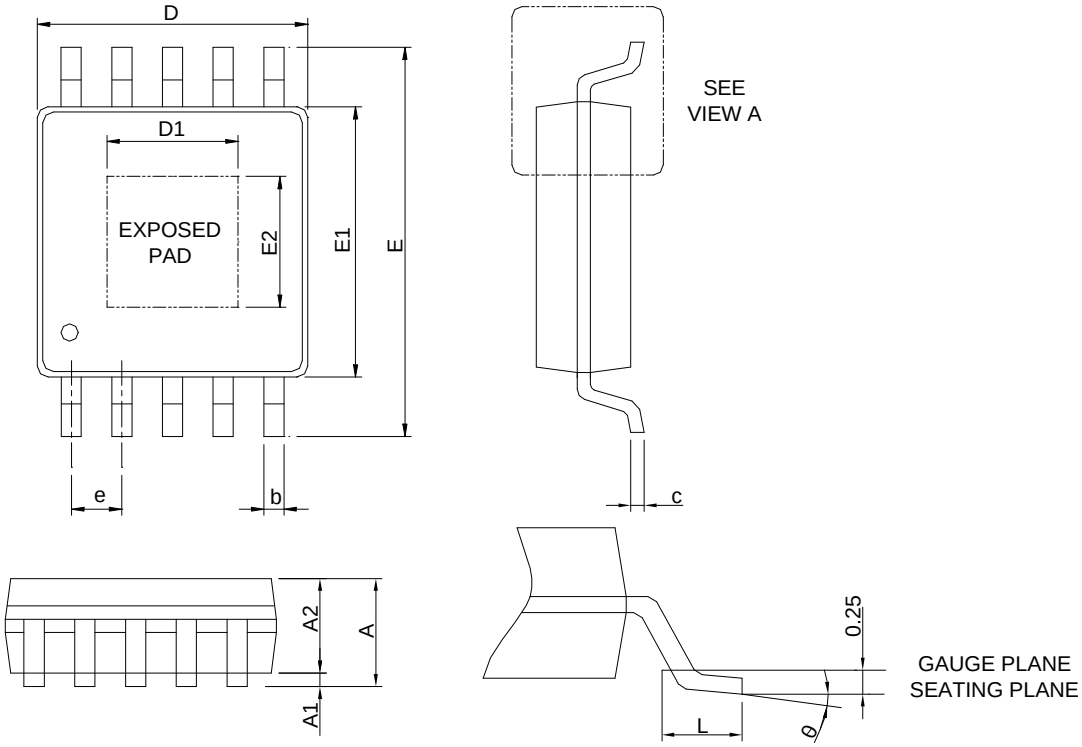
Figure 2 Recommended Layout

Recommended Minimum Footprint



Package Information

MSOP-10P

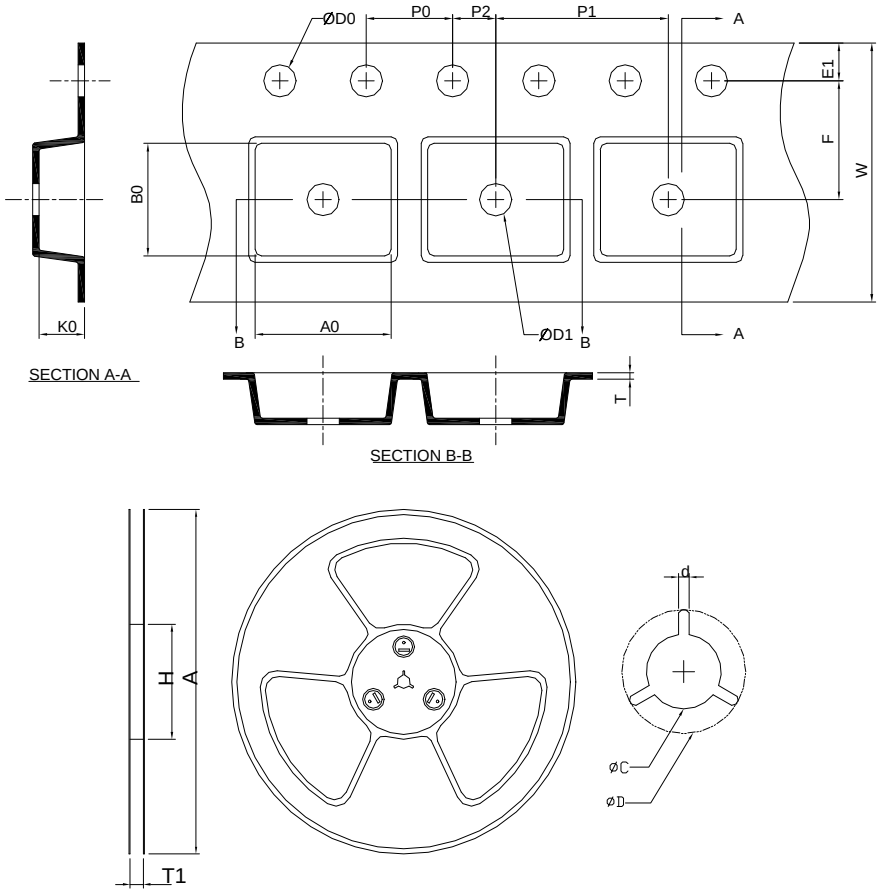


VIEW A

SYMBOL	MSOP-10P			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.10		0.043
A1	0.00	0.15	0.000	0.006
A2	0.75	0.95	0.030	0.037
b	0.17	0.33	0.007	0.013
c	0.08	0.23	0.003	0.009
D	2.90	3.10	0.114	0.122
D1	1.50	2.50	0.059	0.098
E	4.70	5.10	0.185	0.201
E1	2.90	3.10	0.114	0.122
E2	1.50	2.50	0.059	0.098
e	0.50 BSC		0.020 BSC	
L	0.40	0.80	0.016	0.031
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MO-187 BA-T.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not flash or protrusions.
3. Dimension "E1" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 6 mil per side.

Carrier Tape & Reel Dimensions



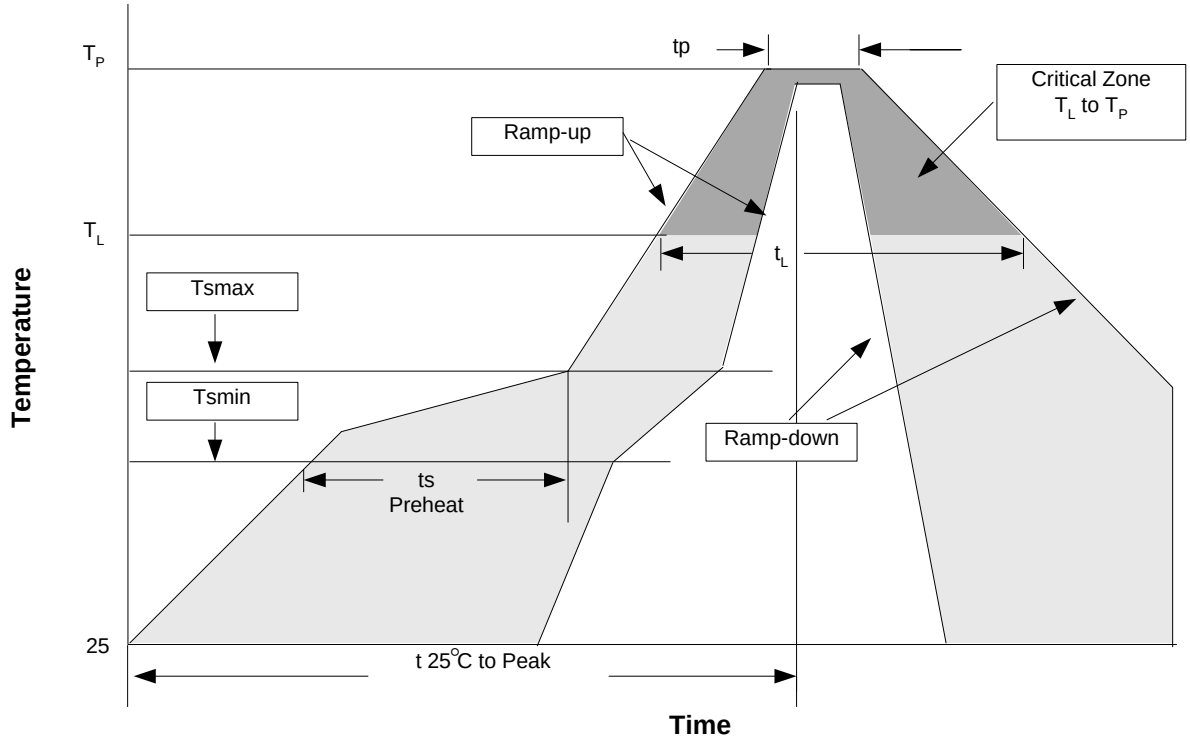
Application	A	H	T1	C	d	D	W	E1	F
MSOP-10P	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.00±0.10	8.00±0.10	2.00±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.70±0.20	3.30±0.20	1.40±0.20

(mm)

Devices Per Unit

Package Type	Unit	Quantity
MSOP- 10P	Tape & Reel	3000

Reflow Condition (IR/Convection or VPR Reflow)



Reliability Test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 sec
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @125°C
PCT	JESD-22-B,A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms, 1_{tr} > 100mA

Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak/Classification Temperature (Tp)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Note: All temperatures refer to topside of the package. Measured on the body surface.

Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*

* Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.

Customer Service

Anpec Electronics Corp.
Head Office :
No.6, Dusing 1st Road, SBIP,
Hsin-Chu, Taiwan, R.O.C.
Tel : 886-3-5642000
Fax : 886-3-5642050

Taipei Branch :
2F, No. 11, Lane 218, Sec 2 Jhongsing Rd.,
Sindian City, Taipei County 23146, Taiwan
Tel : 886-2-2910-3838
Fax : 886-2-2917-3838