0.8V Reference Ultra Low Dropout (0.2V@5A) Linear Regulator

Features

- **Ultra Low Dropout**
  - 0.2V (Typical) at 5A Output Current
- **Low ESR Output Capacitor (Multi-layer Chip Capacitors (MLCC)) Applicable**
- **0.8V Reference Voltage**
- **High Output Accuracy**
  - ±1.5% Over Line, Load and Temperature
- **Fast Transient Response**
- **Adjustable Output Voltage by External Resistors**
- **Power-On-Reset Monitoring on Both VCNTL and VIN Pins**
- **Internal Soft-Start**
- **Current-Limit Protection**
- **Under-Voltage Protection**
- **Thermal Shutdown with Hysteresis**
- **Power-OK Output with a Delay Time**
- **Shutdown for Standby or Suspend Mode**
- **Simple SOP-8P Package with Exposed Pad**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

- **Front Side Bus VTT (1.2V/5A)**
- **Note Book PC Applications**
- **Motherboard Applications**

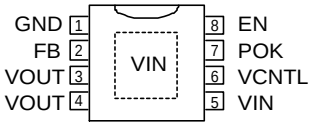
General Description

The APL5912 is a 5A ultra low dropout linear regulator. This product is specifically designed to provide well supply voltage for front-side-bus termination on motherboard and NB applications. The IC needs two supply voltages, a control voltage for the circuitry and a main supply voltage for power conversion, to reduce power dissipation and provide extremely low dropout.

The APL5912 integrates many functions. A Power-On-Reset (POR) circuit monitors both supply voltages to prevent wrong operations. A thermal shutdown and current-limit functions protect the device against thermal and current over-loads. A POK indicates the output status with time delay which is set internally. It can control other converter for power sequence. The APL5912 is enabled by other power system. Pulling and holding the EN pin below 0.3V shuts off the output.

The APL5912 is available in a SOP-8P package which features small size as SOP-8 and an Exposed Pad to reduce the junction-to-case resistance, being applicable in 2~2.5W applications.

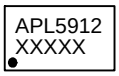
Pin Configuration



SOP-8P (Top View)

= Exposed Pad
(connected to the VIN plane for better heat dissipation)

Ordering and Marking Information

APL5912 □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code KA : SOP-8P Operating Ambient Temperature Range C : 0 to 70 °C Handing Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APL5912 KA : 	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{CNTL}	VCNTL Supply Voltage (VCNTL to GND)	-0.3 ~ 7	V
V_{IN}	VIN Supply Voltage (VIN to GND)	-0.3 ~ 3.3	V
$V_{I/O}$	EN and FB to GND	-0.3 ~ V_{CNTL}+0.3	V
V_{POK}	POK to GND	-0.3 ~ 7	V
P_D	Power Dissipation	3	W
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

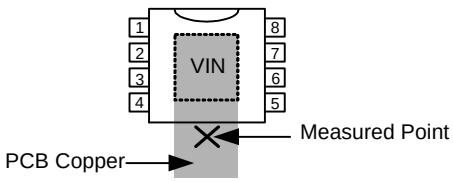
Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance in Free Air (Note 2) SOP-8P	40	°C/W
θ_{JC}	Junction-to-Case Thermal Resistance (Note 3) SOP-8P	17	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of SOP-8P is soldered directly on the PCB.

Note 3: The "Thermal Pad Temperature" is measured on the PCB copper area connected to the thermal pad of package.



Recommended Operating Conditions

Symbol	Parameter	Range	Unit
V_{CNTL}	VCNTL Supply Voltage	3.1 ~ 6	V
V_{IN}	VIN Supply Voltage	1.0 ~ 3.3	V
V_{OUT}	Output Voltage V_{CNTL}=3.3±5% V_{CNTL}=5.0±5%	 0.8 ~ 1.2 0.8 ~ V_{IN}-0.2	V
I_{OUT}	VOUT Output Current	0 ~ 6	A
T_J	Junction Temperature	-25 ~ 125	°C

Electrical Characteristics

Refer to "Typical Application Circuits". These specifications apply over, V_{CNTL}=5V, V_{IN}=1.5V, V_{OUT} = 1.2V and T_A=0 to 70°C, unless otherwise specified. Typical values refer to T_A=25°C.

Symbol	Parameter	Test Conditions	APL5912			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
I_{CNTL}	VCNTL Supply Current	EN = VCNTL, V_{FB} is well regulated	0.4	1	2	mA
I_{SD}	VCNTL Shutdown Current	EN = GND	-	180	380	µA
POWER-ON-RESET						
	VCNTL POR Threshold	V_{CNTL} Rising	2.7	2.9	3.1	V
	VCNTL POR Hysteresis		-	0.4	-	V
	VIN POR Threshold	V_{IN} Rising	0.8	0.9	0.99	V
	VIN POR Hysteresis		-	0.5	-	V
OUTPUT VOLTAGE						
V_{REF}	Reference Voltage	FB =VOUT	-	0.8	-	V
	Output Voltage Accuracy	I_{OUT}=0A ~ 5A, T_J= -25 ~125°C	-1.5	-	+1.5	%
	Line Regulation	V_{CNTL}=3.3 ~ 5.5V	-0.13	-	0.13	%/V
	Load Regulation	I_{OUT}=0A ~ 5A	-	0.06	0.15	%
DROPOUT VOLTAGE						
	Dropout Voltage	I_{OUT} = 5A, V_{CNTL}=5V, T_J= 25°C	-	0.15	0.2	V
		I_{OUT} = 5A, V_{CNTL}=5V, T_J= -25~125°C	-	-	0.25	V
PROTECTION						
I_{LIM}	Current Limit	V_{CNTL}=5V, T_J= 25°C	7	8	9	A
		V_{CNTL}=5V, T_J= -25 ~ 125°C	6	-	-	A
		V_{CNTL}=3.3V, T_J= 25°C	6.8	7.8	8.8	A
		V_{CNTL}=3.3V, T_J= -25 ~ 125°C	6	-	-	A
T_{SD}	Thermal Shutdown Temperature	T_J Rising	-	150	-	°C
	Thermal Shutdown Hysteresis		-	50	-	°C
	Under-Voltage Threshold	V_{FB} Falling	-	0.4	-	V

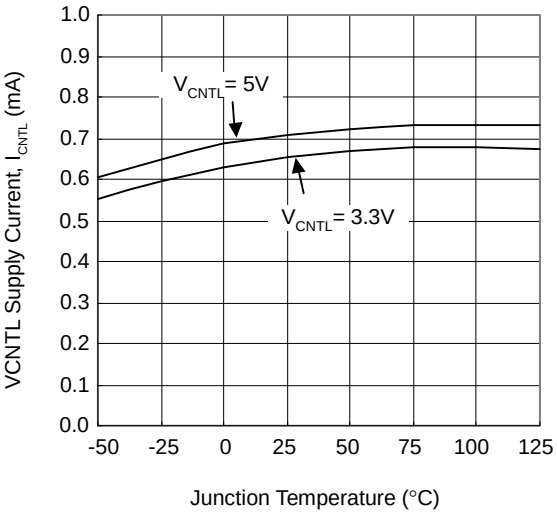
Electrical Characteristics (Cont.)

Refer to "Typical Application Circuits". These specifications apply over, V_{CNTL}=5V, V_{IN}=1.5V, V_{OUT} = 1.2V and T_A=0 to 70°C, unless otherwise specified. Typical values refer to T_A=25°C.

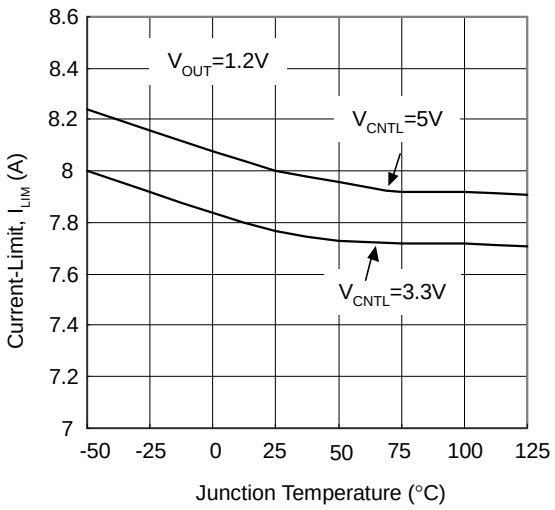
Symbol	Parameter	Test Conditions	APL5912			Unit
			Min.	Typ.	Max.	
ENABLE AND SOFT-START						
	EN Logic High Threshold Voltage	V_{EN} Rising	0.3	0.4	0.5	V
	EN Hysteresis		-	30	-	mV
	EN Pin Pull-Up Current	EN=GND	-	10	-	μA
T_{SS}	Soft-Start Interval		-	2	-	ms
POWER-OK AND DELAY						
V_{POK}	POK Threshold Voltage for Power OK	V_{FB} Rising	90%	92%	94%	V_{REF}
V_{PNOK}	POK Threshold Voltage for Power Not OK	V_{FB} Falling	79%	81%	83%	V_{REF}
	POK Low Voltage	POK sinks 5mA	-	0.25	0.4	V
T_{DELAY}	POK Delay Time		1	3	10	ms

Typical Operating Characteristics

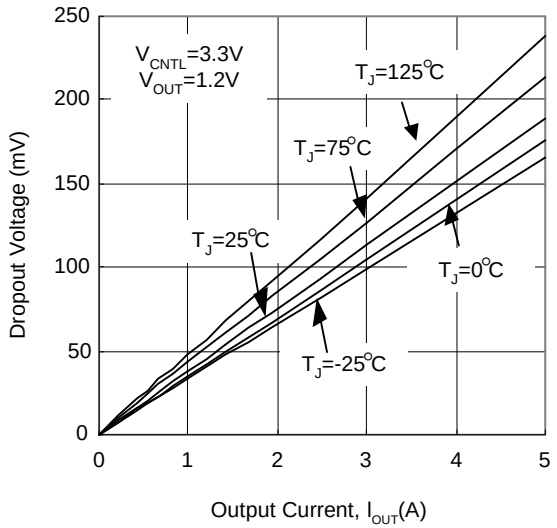
VCNTL Supply Current vs. Junction Temperature



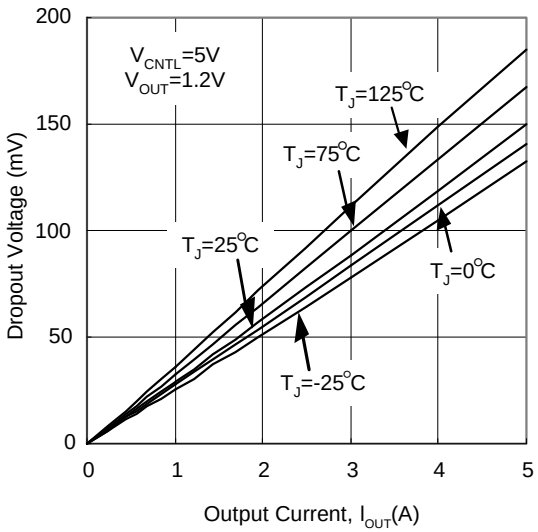
Current-Limit vs. Junction Temperature



Dropout Voltage vs. Output Current

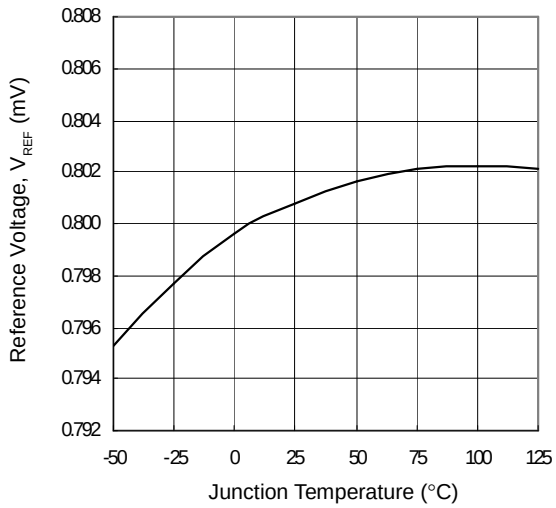


Dropout Voltage vs. Output Current

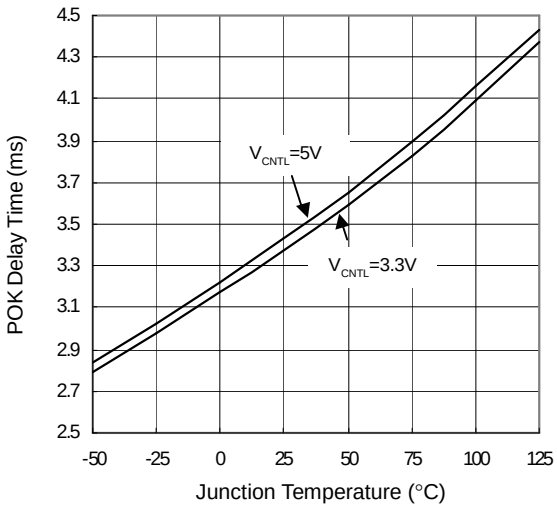


Typical Operating Characteristics

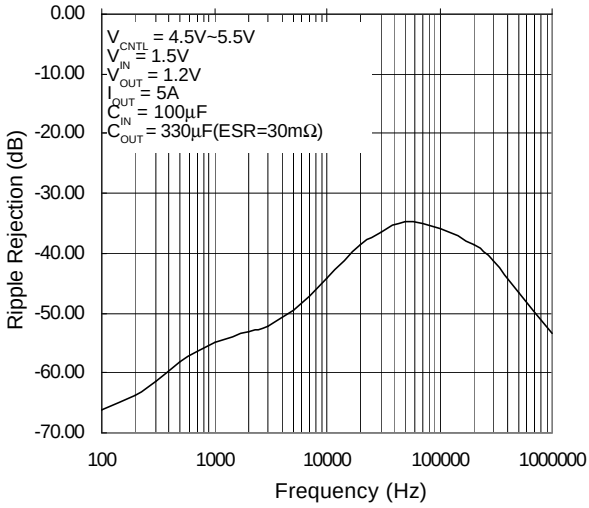
Reference Voltage vs. Junction Temperature



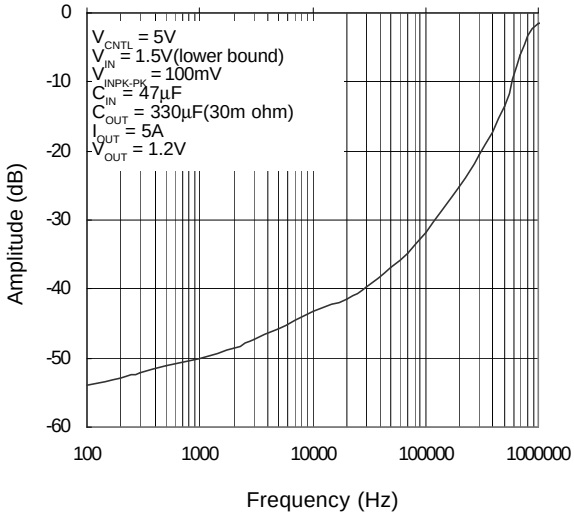
POK Delay Time vs. Junction Temperature



VCNTL PSRR

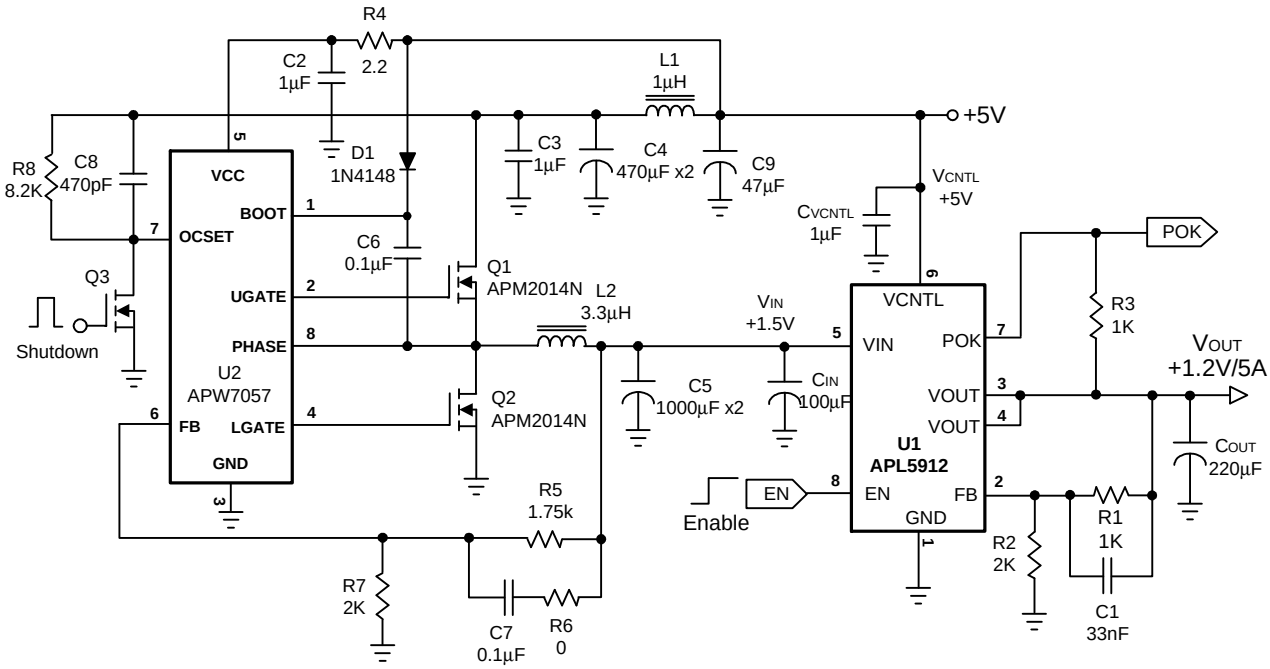


VIN PSRR



Operating Waveforms

Test Circuit

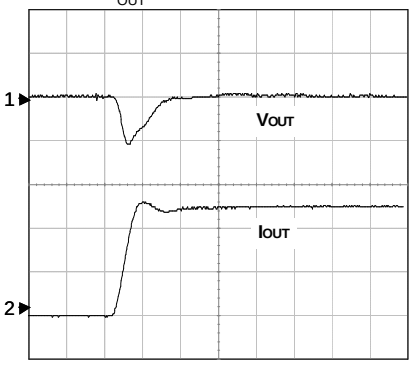


1. Load transient Response

1.1 Using an Output Capacitor with ESR≥18mΩ

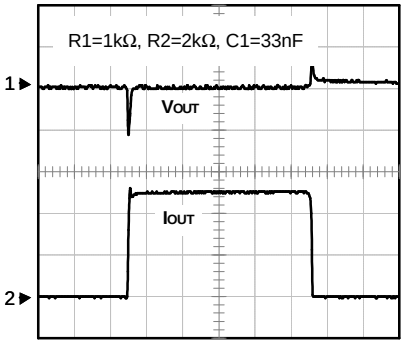
- C_{OUT} = 220µF/6.3V (ESR = 30mΩ), C_{IN} = 100µF/6.3V
- I_{OUT} = 10mA to 5A to 10mA, Rise time = Fall time = 1µs

I_{OUT} = 10mA ->5A



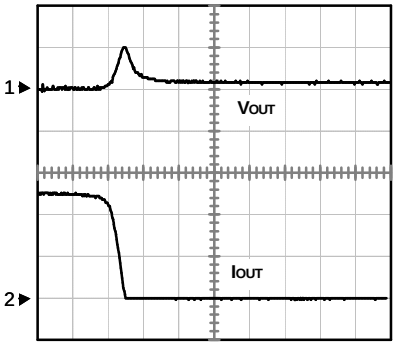
Ch1 : V_{OUT}, 50mV/Div
Ch2 : I_{OUT}, 2A/Div
Time : 2µs/Div

I_{OUT} = 10mA -> 5A ->10mA



Ch1 : V_{OUT}, 50mV/Div
Ch2 : I_{OUT}, 2A/Div
Time : 20µs/Div

I_{OUT} = 5A ->10mA



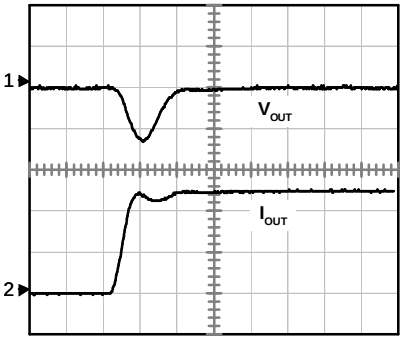
Ch1 : V_{OUT}, 50mV/Div
Ch2 : I_{OUT}, 2A/Div
Time : 2µs/Div

Operating Waveforms (Cont.)

1.2 Using an MLCC as the Output Capacitor

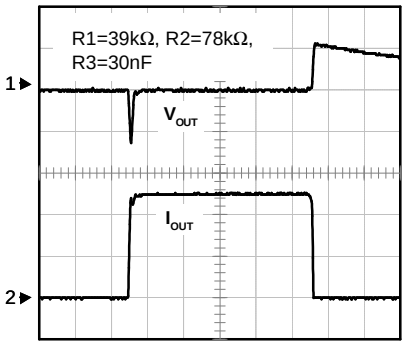
- C_{OUT} = 22µF/6.3V (ESR = 3mΩ), C_{IN} = 22µF/6.3V
- I_{OUT} = 10mA to 5A to 10mA, Rise time = Fall time = 1µs

I_{OUT} = 10mA -> 5A



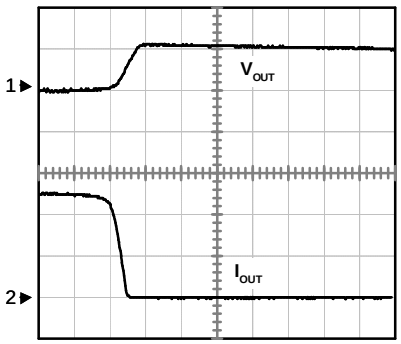
Ch1 : V_{OUT}, 100mV/Div
Ch2 : I_{OUT}, 2A/Div
Time : 2µs/Div

I_{OUT} = 10mA -> 5A ->10mA



Ch1 : V_{OUT}, 100mV/Div
Ch2 : I_{OUT}, 2A/Div
Time : 20µs/Div

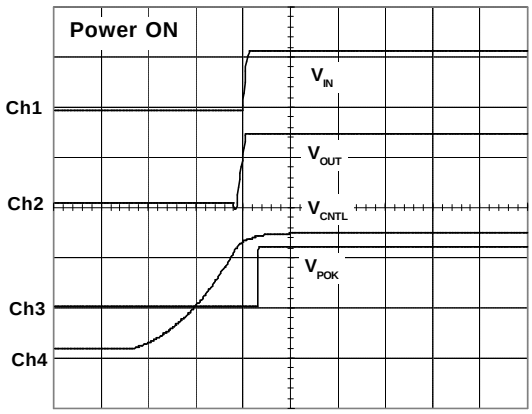
I_{OUT} = 5A ->10mA



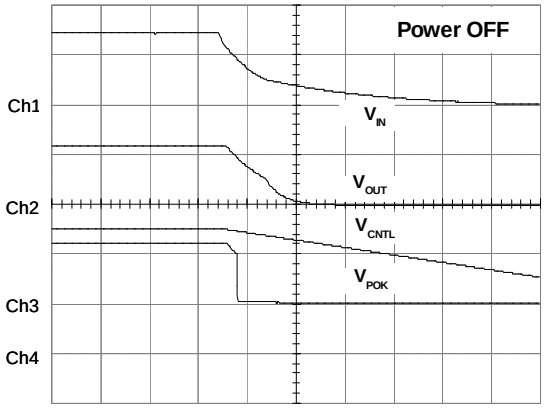
Ch1 : V_{OUT}, 100mV/Div
Ch2 : I_{OUT}, 2A/Div
Time : 2µs/Div

2. Power ON and Power OFF :

- V_{IN} = 1.5V, V_{CNTL} = 5V,V_{OUT} = 1.2V
- C_{OUT} = 220µF/6.3V (ESR = 30mΩ), C_{IN} = 100µF/6.3V, R_L = 1Ω



Ch1 : V_{IN}, 1V/div
Ch2 : V_{OUT},1V/div
Ch3 : V_{POK},1V/div
Ch4 : V_{CNTL},2V/div
Time : 10ms/div

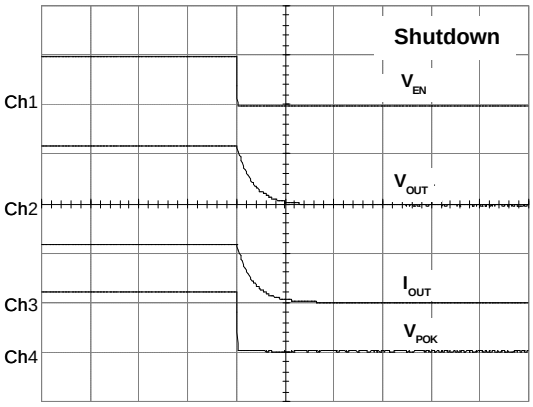


Ch1 : V_{IN}, 1V/div
Ch2 : V_{OUT}, 1V/div
Ch3 : V_{POK}, 1V/div
Ch4 : V_{CNTL}, 2V/div
Time : 10ms/div

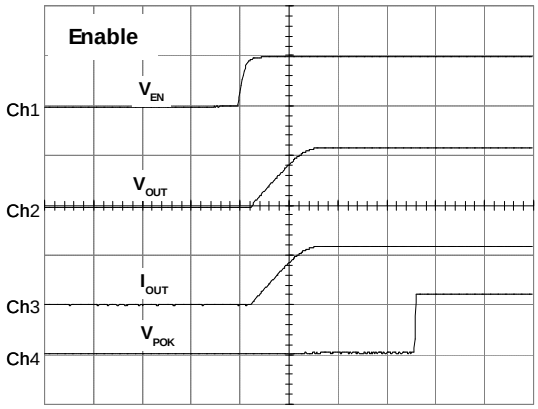
Operating Waveforms (Cont.)

3. Shutdown and Enable :

- V_{IN} = 1.5V, V_{CNTL} = 5V, V_{OUT} = 1.2V
- C_{OUT} = 220µF/6.3V (ESR = 30mΩ), C_{IN} = 100µF/6.3V, R_L = 1Ω



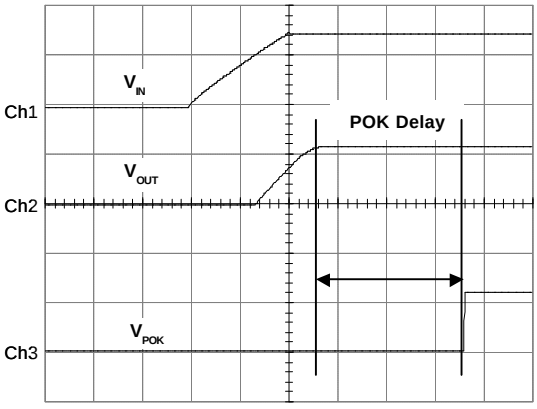
Ch1 : V_{EN}, 5V/div
Ch2 : V_{OUT}, 1V/div
Ch3 : I_{OUT}, 1A/div
Ch4 : V_{POK}, 1V/div
Time : 1ms/div



Ch1 : V_{EN}, 5V/div
Ch2 : V_{OUT}, 1V/div
Ch3 : I_{OUT}, 1A/div
Ch4 : V_{POK}, 1V/div
Time : 1ms/div

4. POK Delay :

- V_{IN} = 1.5V, V_{CNTL} = 5V, V_{OUT} = 1.2V
- C_{OUT} = 220µF/6.3V (ESR = 30mΩ), C_{IN} = 100µF/6.3V, R_L = 1Ω

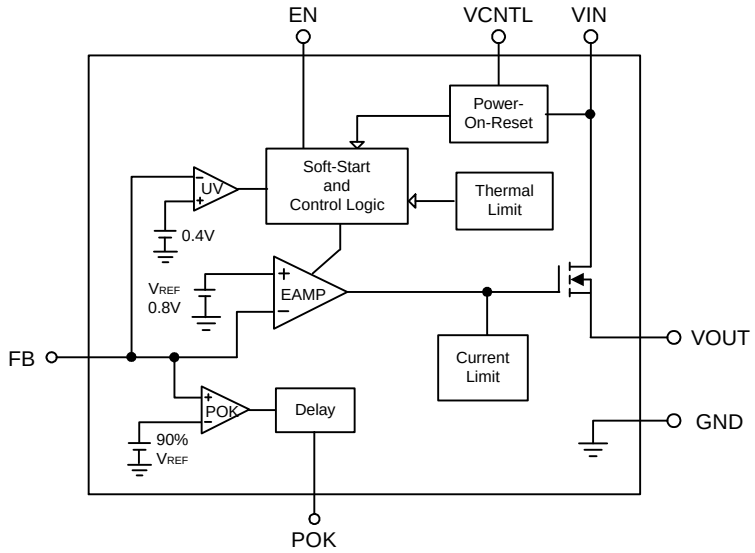


Ch1 : V_{IN}, 5V/div
Ch2 : V_{OUT}, 1V/div
Ch3 : V_{POK}, 1V/div
Time : 1ms/div

Pin Description

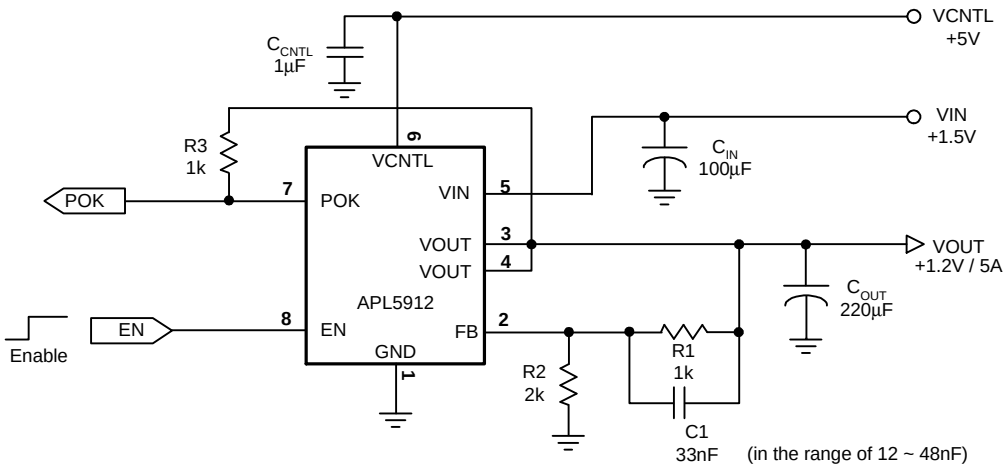
PIN		FUNCTION
NO.	NAME	
1	GND	Ground pin of the circuitry. All voltage levels are measured with respect to this pin.
2	FB	Connecting this pin to an external resistor divider receives the feedback voltage of the regulator. The output voltage set by the resistor divider is determined by : $V_{OUT} = 0.8 \cdot \left(1 + \frac{R1}{R2}\right)$ where R1 is connected from VOUT to FB with Kelvin sensing and R2 is connected from FB to GND. A bypass capacitor may be connected with R1 in parallel to improve load transient response.
3,4	VOUT	Output of the regulator. Please connect Pin 3 and 4 together using wide tracks. It is necessary to connect a output capacitor with this pin for closed-loop compensation and improve transient responses.
5	VIN	Main supply input pins for power conversions. The Exposed Pad provides a very low impedance input path for the main supply voltage. Please tie the Exposed Pad and VIN Pin (Pin 8) together to reduce the dropout voltage. The voltage at this pins is monitored for Power-On-Reset purpose.
6	VCNTL	Power input pin of the control circuitry. Connecting this pin to a +5V (recommended) supply voltage provides the bias for the control circuitry. The voltage at this pin is monitored for Power-On-Reset purpose.
7	POK	Power-OK signal output pin. This pin is an open-drain output used to indicate status of output voltage by sensing FB voltage. This pin is pulled low when the rising FB voltage is not above the V_{POK} threshold or the falling FB voltage is below the V_{PNOK} threshold, indicating the output is not OK.
8	EN	Enable control pin. Pulling and holding this pin below 0.3V shuts down the output. When re-enabled, the IC undergoes a new soft-start cycle. When leave this pin open, an internal current source 10μA pulls this pin up to VCNTL voltage, enabling the regulator.
-	Exposed Pad	Main supply input pins for power conversions. The Exposed Pad provides a very low impedance input path for the main supply voltage. Please tie the Exposed Pad and VIN Pin (Pin 8) together to reduce the dropout voltage. The voltage at this pins is monitored for Power-On-Reset purpose.

Block Diagram

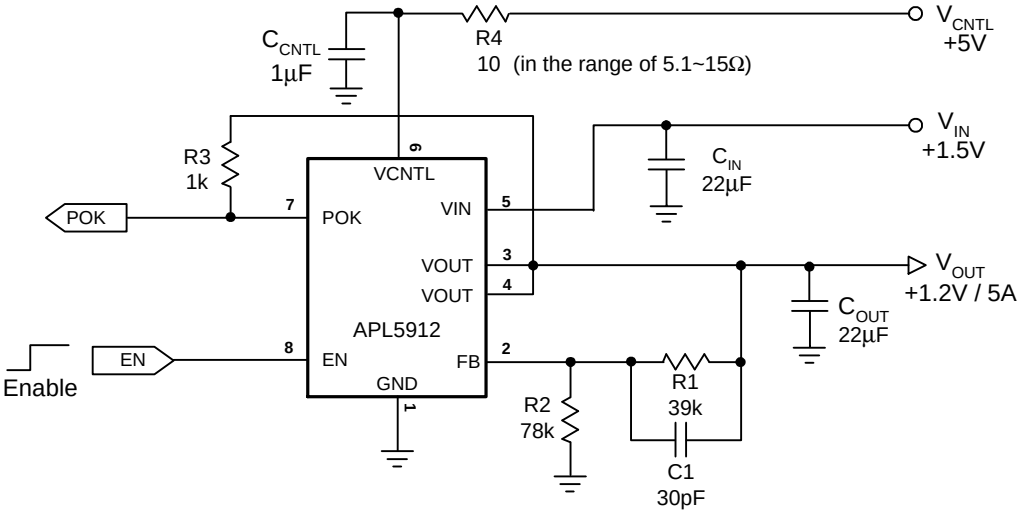


Typical Application Circuit

1. Using an Output Capacitor with ESR³18mW



2. Using an MLCC as the Output Capacitor



V_{OUT}(V)	R1 (kΩ)	R2 (kΩ)	C1 (pF)
1.05	43	137.6	27
1.5	27	30.86	36
1.8	15	12	68

Function Description

Power-On-Reset

A Power-On-Reset (POR) circuit monitors both input voltages at VCNTL and VIN pins to prevent wrong logic controls. The POR function initiates a soft-start process after the two supply voltages exceed their rising POR threshold voltages during powering on. The POR function also pulls low the POK pin regardless the output voltage when the VCNTL voltage falls below its falling POR threshold.

Internal Soft-Start

An internal soft-start function controls rising rate of the output voltage to limit the current surge at start-up. The typical soft-start interval is about 2ms.

Output Voltage Regulation

An error amplifier works with a temperature-compensated 0.8V reference and an output NMOS regulates output to the preset voltage. The error amplifier is designed with high bandwidth and DC gain provides very fast transient response and less load regulation. It compares the reference with the feedback voltage and amplifies the difference to drive the output NMOS which provides load current from VIN to VOUT.

Current-Limit

The APL5912 monitors the current via the output NMOS and limits the maximum current to prevent load and APL5912 from damages during overload or short-circuit conditions.

Under-Voltage Protection (UVP)

The APL5912 monitors the voltage on FB pin after soft-start process is finished. Therefore, the UVP is disable during soft-start. When the voltage on FB pin falls below the under-voltage threshold, the UVP circuit shuts off the output immediately. After a while, the APL5912 starts a new soft-start to regulate output.

Thermal Shutdown

A thermal shutdown circuit limits the junction temperature of APL5912. When the junction temperature exceeds +150°C, a thermal sensor turns off the output NMOS, allowing the device to cool down. The regulator regulates the output again through initiation of a new soft-start cycle after the junction temperature cools by 50°C, resulting in a pulsed output during continuous thermal overload conditions. The thermal shutdown is designed with a 50°C hysteresis to lower the average junction temperature during continuous thermal overload conditions, extending lifetime of the device.

For normal operation, device power dissipation should be externally limited so that junction temperatures will not exceed +125°C.

Enable Control

The APL5912 has a dedicated enable pin (EN). A logic low signal (V_{EN}< 0.3V) applied to this pin shuts down the output. Following a shutdown, a logic high signal re-enables the output through initiation of a new soft-start cycle. Left open, this pin is pulled up by an internal current source (10μA typical) to enable operation. It's not necessary to use an external transistor to save cost.

Power-OK and Delay

The APL5912 indicates the status of the output voltage by monitoring the feedback voltage (V_{FB}) on FB pin. As the V_{FB} rises and reaches the rising Power-OK threshold (V_{POK}), an internal delay function starts to perform a delay time. At the end of the delay time, the IC turns off the internal NMOS of the POK to indicate the output is OK. As the V_{FB} falls and reaches the falling Power-OK threshold (V_{PNOK}), the IC immediately turns on the NMOS of the POK to indicate the output is not OK without a delay time.

Application Information

Power Sequencing

The power sequencing of VIN and VCNTL is not necessary to be concerned. However, do not apply a voltage to VOUT for a long time when the main voltage applied at VIN is not present. The reason is the internal parasitic diode from VOUT to VIN conducts and dissipates power without protections due to the forward-voltage

Output Capacitor

The APL5912 requires a proper output capacitor to maintain stability and improve transient response over temperature and current. The output capacitor selection is to select proper ESR (equivalent series resistance) and capacitance of the output capacitor for good stability and load transient response.

The APL5912 is designed with a programmable feedback compensation adjusted by an external feedback network for the use of wide ranges of ESR and capacitance in all applications. Ultra-low-ESR capacitors (such as ceramic chip capacitors) and low-ESR bulk capacitors (such as solid tantalum, POSCap, and Aluminum electrolytic capacitors) can all be used as an output capacitor. The value of the output capacitors can be increased without limit.

During load transients, the output capacitors, depending on the stepping amplitude and slew rate of load current, are used to reduce the slew rate of the current seen by the APL5912 and help the device to minimize the variations of output voltage for good transient response. For the applications with large stepping load current, the low-ESR bulk capacitors are normally recommended.

Decoupling ceramic capacitors must be placed at the load and ground pins as close as possible and the impedance of the layout must be minimized.

Input Capacitor

The APL5912 requires proper input capacitors to supply current surge during stepping load transients to prevent the input rail from dropping. Because the parasitic inductor from the voltage sources or other bulk capacitors to the VIN pin limit the slew rate of the surge currents, more parasitic inductance needs more input capacitance.

Ultra-low-ESR capacitors (such as ceramic chip capacitors) and low-ESR bulk capacitors (such as solid tantalum, POSCap, and Aluminum electrolytic capacitors) can all be used as an input capacitor of VIN. For most applications, the recommended input capacitance of VIN is 10µF at least. If the drop of the input voltage is not cared, the input capacitance can be less than 10µF. More capacitance reduces the variations of the input voltage of VIN pin.

Feedback Network

Figure 1 shows the feedback network among VOUT, GND, and FB pins. It works with the internal error amplifier to provide proper frequency response for the linear regulator. The ESR is the equivalent series resistance of the output capacitor. The C_{OUT} is ideal capacitance in the output capacitor. The V_{OUT} is the setting of the output voltage.

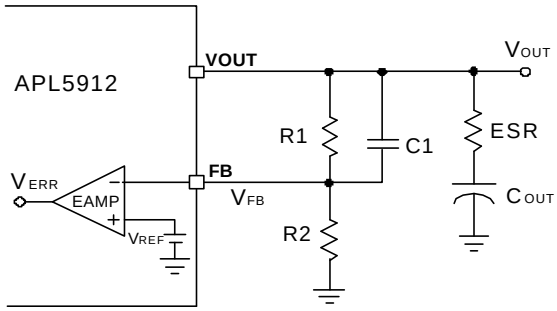


Figure 1

The feedback network selection, depending on the values of the ESR and C_{OUT}, has been classified into three conditions :

- **Condition 1 : Large ESR (≥18mΩ)**
  - Select the R1 in the range of 400Ω ~ 2.4kΩ
  - Calculate the R2 as the following:

$$R2(k\Omega) = R1(k\Omega) \cdot \frac{0.8(V)}{V_{OUT}(V) - 0.8(V)} \quad \text{..... (1)}$$

  - Calculate the C1 as the following:

$$10 \cdot \frac{V_{OUT}(V)}{R1(k\Omega)} \le C1(nF) \le 40 \cdot \frac{V_{OUT}(V)}{R1(k\Omega)} \quad \text{..... (2)}$$

- **Condition 2 : Middle ESR**
  - Calculate the R1 as the following:

$$R1(k\Omega) = \frac{1500}{ESR(m\Omega)} - 37.5 \cdot V_{OUT}(V) + 30 \quad \text{..... (3)}$$

Application Information (Cont.)

Feedback Network (Cont.)

Select a proper R1(selected) to be a little larger than the calculated R1.

- Calculate the C1 as the following:

$$C1(pF) = [ESR(m\Omega) + 50] \cdot \frac{C_{OUT}(\mu F)}{R1(k\Omega)} \quad \text{..... (4)}$$

Where $R1=R1_{(selected)}$

Select a proper $C1_{(selected)}$ to be a little smaller than the calculated C1.

- The C1 calculated from equation (4) must meet the following equation :

$$C1(pF) \geq 5.1 \cdot \left[1 + \frac{50}{ESR(m\Omega)}\right] \cdot \left[1 + \frac{37.5 \cdot V_{OUT}(V)}{R1(k\Omega)}\right] \text{..(5)}$$

Where R1=R1(calculated) from equation (3)

If the C1(calculated) can not meet the equation (5), please use the Condition 3.

- Use equation (2) to calculate the R2.

• Condition 3: Low ESR (eg. Ceramic Capacitors)

- Calculate the R1 as the following:

$$R1(k\Omega) = \sqrt{(5.9 \cdot ESR(m\Omega) + 294) \cdot C_{OUT}(\mu F)} - 37.5 \cdot V_{OUT}(V) \text{..(6)}$$

Select a proper R1(selected) to be a little larger than the calculated R1. ***The minimum selected R1 is equal to 1k*** *when the calculated R1 is smaller than 1k or negative.*

- Calculate the C1 as the following :

$$C1(pF) = \sqrt{(0.17 \cdot ESR(m\Omega) + 8.5) \cdot C_{OUT}(\mu F)} \cdot \left[1 + \frac{37.5 \cdot V_{OUT}(V)}{R1(k\Omega)}\right] \text{..(7)}$$

Where $R1=R1_{(selected)}$

Select a proper C1(selected) to be a little smaller than the calculated C1.

- The C1 calculated from equation (7) must meet the following equation :

$$C1(pF) \geq \left[0.033 + \frac{1.25 \cdot V_{OUT}(V)}{R1(k\Omega)}\right] \cdot ESR(m\Omega) \cdot C_{OUT}(\mu F) \text{..(8)}$$

Where R1=R1(calculated) from equation (6)

If the C1(calculated) can not meet the equation (8), please use the Condition 2.

- Use equation (2) to calculate the R2.

The reason to have three conditions described above is to optimize the load transient responses for all kinds of the output capacitor. For stability only, the Condition 2, regardless of equation (5), is enough for all kinds of output capacitor.

PCB Layout Consideration (See Figure 2)

1. Please solder the Exposed Pad and VIN together on the PCB. The main current flow is through the exposed pad.
2. Please place the input capacitors for VIN and VCNTL pins near pins as close as possible.
3. Ceramic decoupling capacitors for load must be placed near the load as close as possible.
4. To place APL5912 and output capacitors near the load is good for performance.
5. The negative pins of the input and output capacitors and the GND pin of the APL5912 are connected to the ground plane of the load.
6. Please connect PIN 3 and 4 together by a wide track or plane on the Top layer.
7. Large current paths must have wide tracks.
8. See the Typical Application
   - Connect the one pin of the R2 to the GND of APL5912.

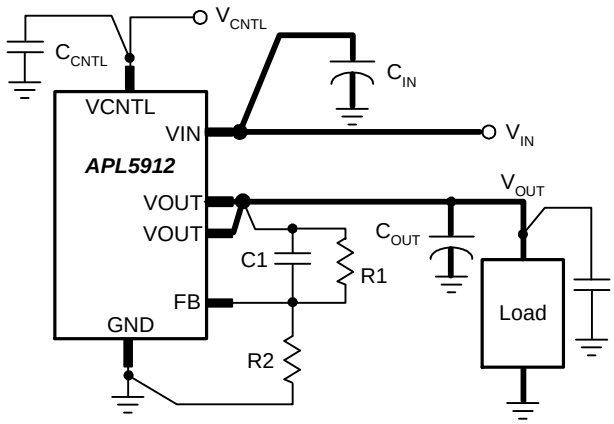


Figure 2

- Connect the one pin of R1 to the Pin 3 of APL5912
- Connect the one pin of C1 to the Pin 3 of APL5912

Application Information (Cont.)

Thermal Consideration

See Figure 3. The SOP-8P is a cost-effective package featuring a small size like a standard SOP-8 and a bottom exposed pad to minimize the thermal resistance of the package, being applicable to high current applications. The exposed pad must be soldered to the top V_{IN} plane. The copper of the V_{IN} plane on the Top layer conducts heat into the PCB and air. Please enlarge the area to reduce the case-to-ambient resistance (θ_{CA}).

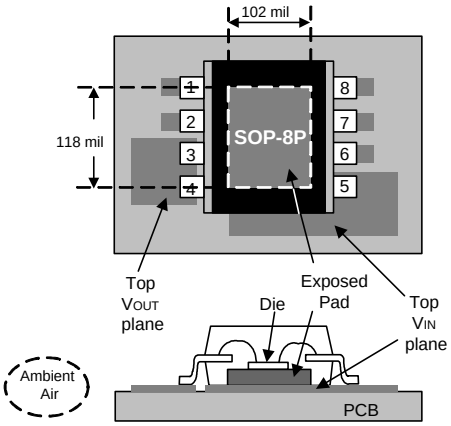
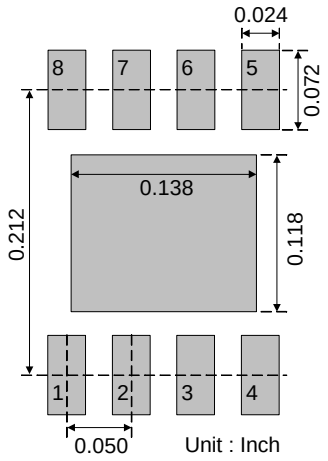


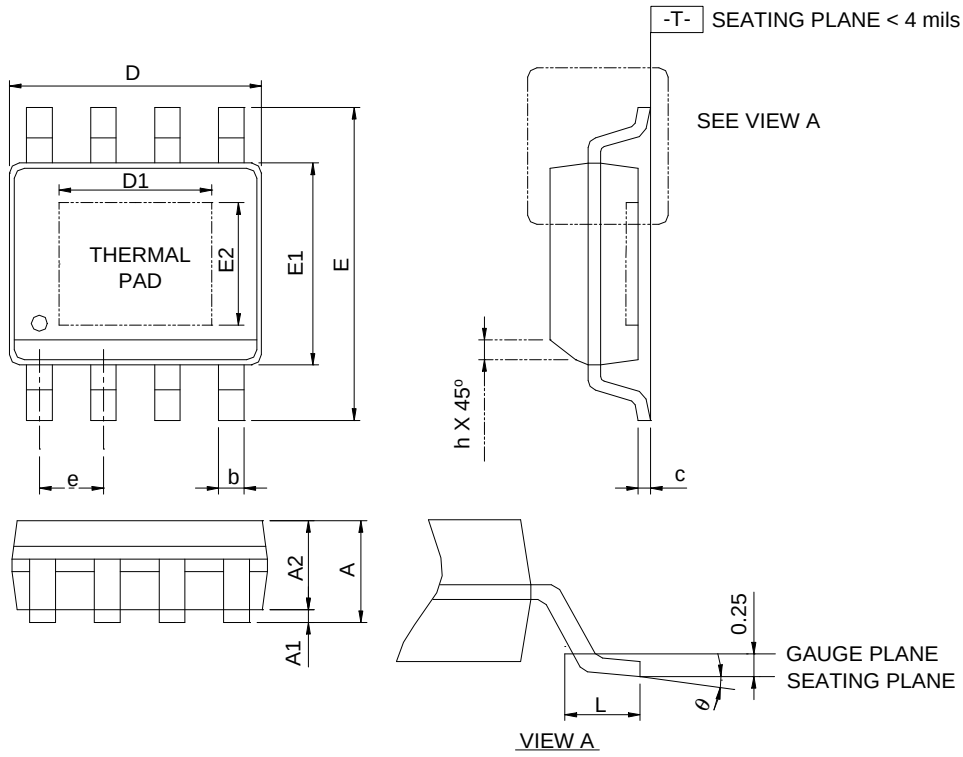
Figure 3

Recommended Minimum Footprint



Package Information

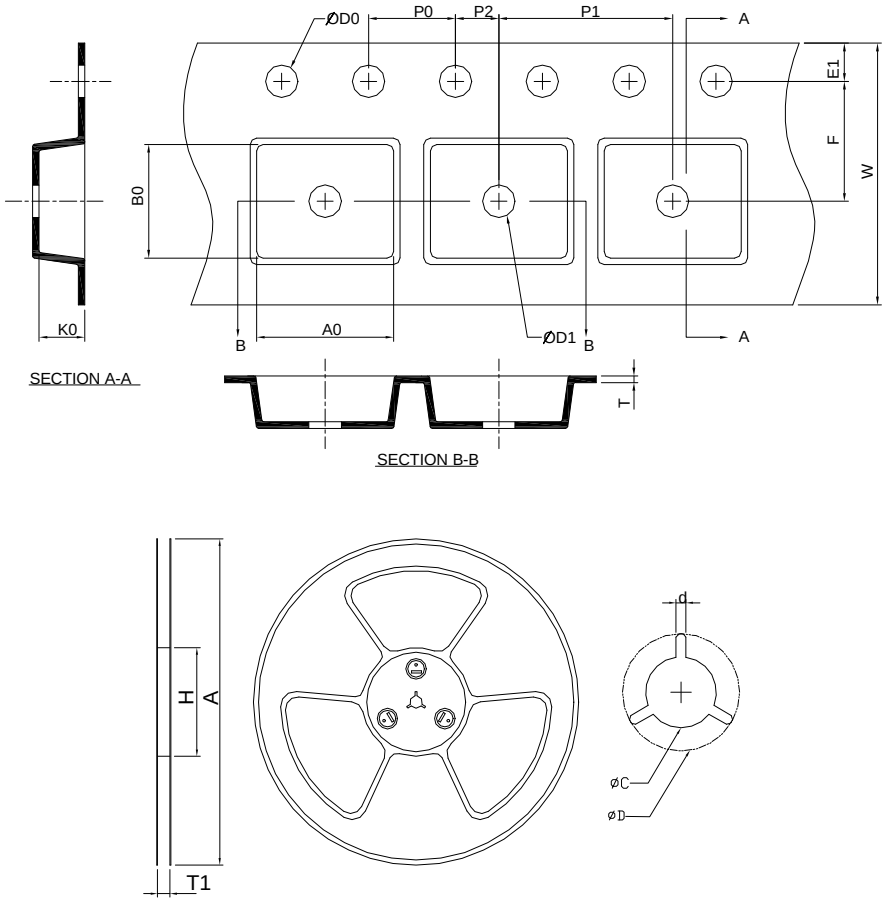
SOP-8P



SYMBOL	SOP-8P			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.60		0.063
A1	0.00	0.15	0.000	0.006
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
D1	2.50	3.50	0.098	0.138
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
E2	2.00	3.00	0.079	0.118
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°C	8°C	0°C	8°C

Note : 1. Followed from JEDEC MS-012 BA.
2. Dimension "D" does not include mold flash, protrusions or gate burrs.
Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .
3. Dimension "E" does not include inter-lead flash or protrusions.
Inter-lead flash and protrusions shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
SOP-8P	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	5.20±0.20	2.10±0.20

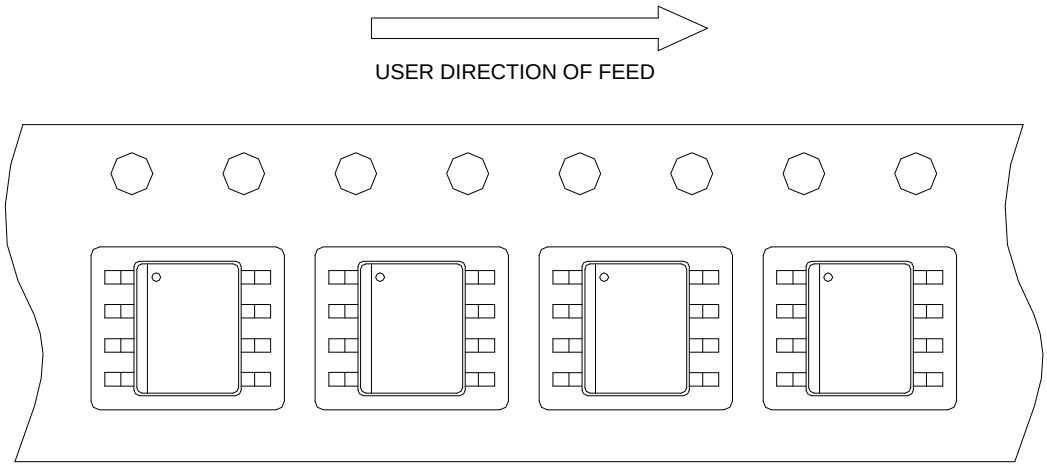
(mm)

Devices Per Unit

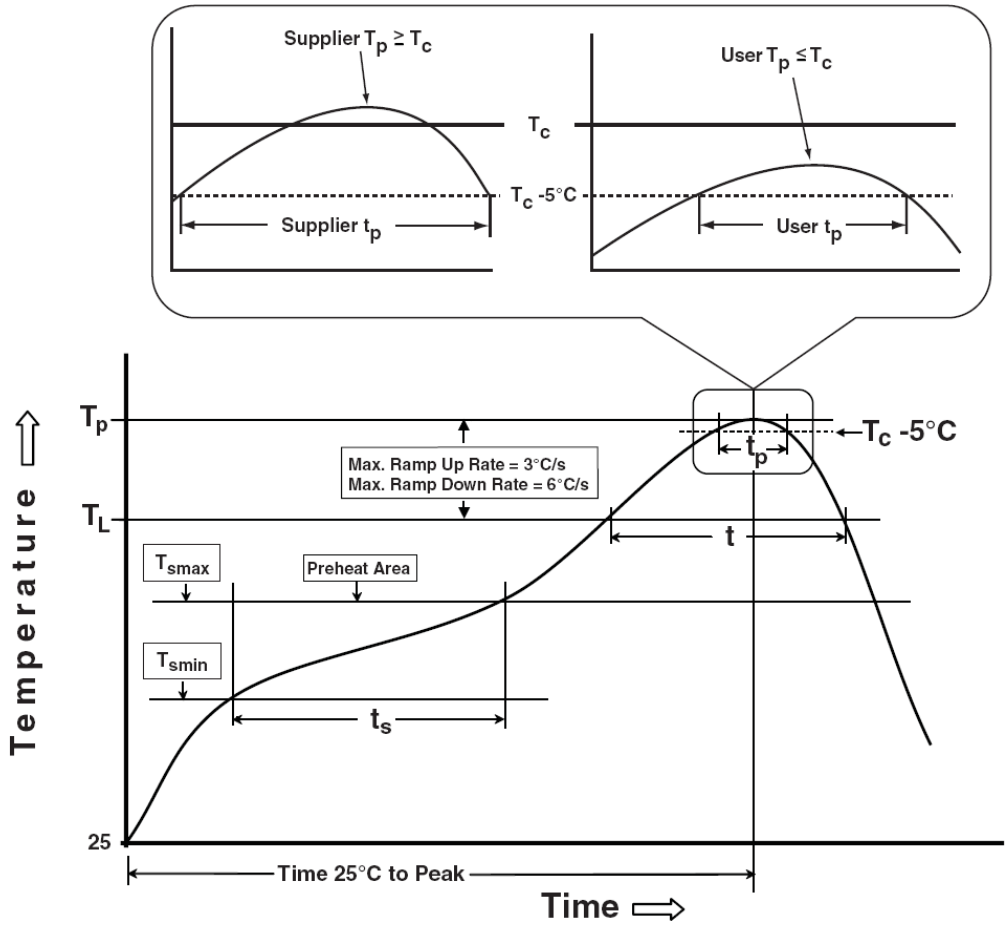
Package Type	Unit	Quantity
SOP- 8P	Tape & Reel	2500

Taping Direction Information

SOP-8P



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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